Triple video output amplifier

GENERAL DESCRIPTION

The ILA6107Q includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black-current control

FEATURES

- Typical bandwidth of 5.5 MHz for an output signal of 60 V (p-p)
- High slew rate of 900 V/μs
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 50
- Black-Current Stabilization (BCS) circuit
- Thermal protection.

BLOCK DIAGRAM

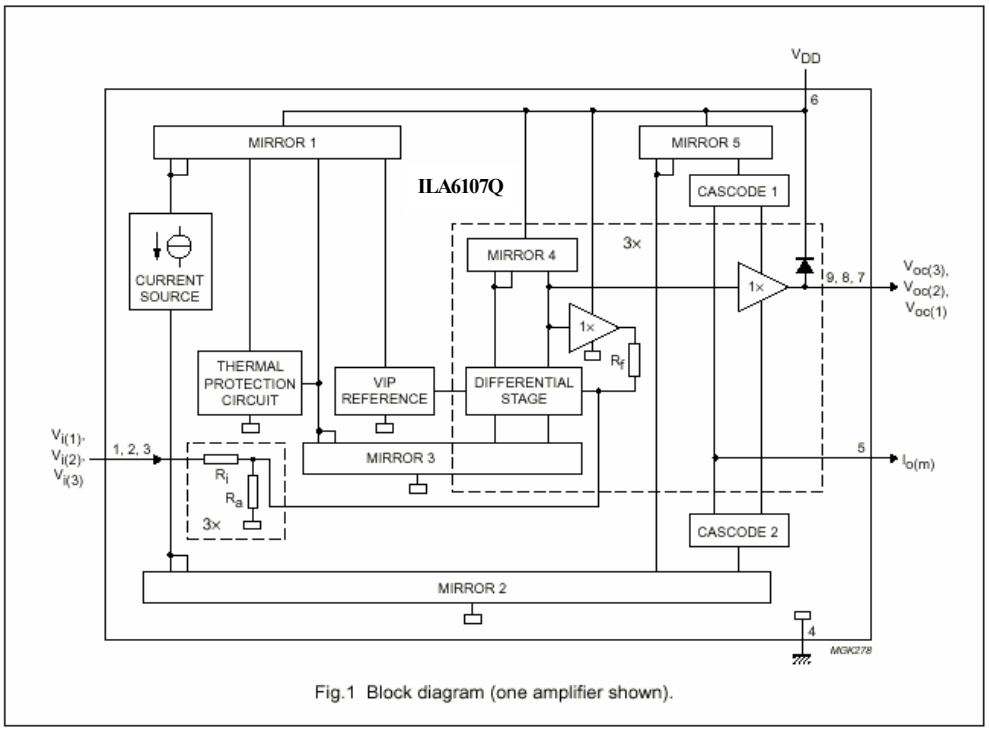
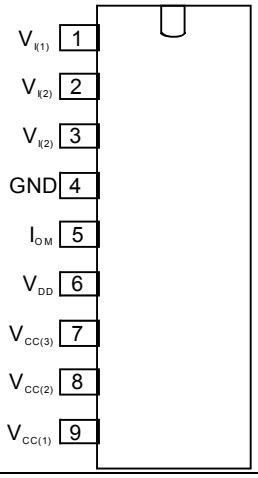


Fig.1 Block diagram (one amplifier shown).

INTEGRAL

PINNING

SIMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black-current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltage measured with respect to pin 4 (ground); currents as specified in Fig. 1; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	0	250	
V_i	supply voltage at pins 1 to 3	0	12	
$V_{o(m)}$	measurement output voltage	0	6	
$V_{o(c)}$	cathode output voltage	0	V_{DD}	
T_{stg}	storage temperature	-55	+150	°C
T_j	junction temperature	-20	+150	°C
V_{es}	electrostatic handling			
	Human Body Model (HBM)	-	2000	V
	Machine Model (MM)	-	300	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see "*Handling MOS Devices*").

QUALITY SPECIFICATION

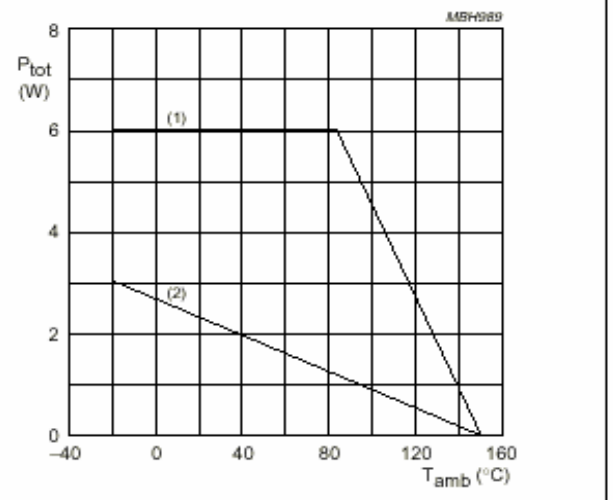
Quality specification "*SNW-FQ-611 part D* " is applicable and can be found in the "*Quality reference Handbook* ". The handbook can be ordered using the code (9397 750 00192.

THERMAL HARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient		56	K/W
$R_{th(j-fin)}$	thermal resistance from junction to fin	note 1	11	K/W
$R_{th(h-a)}$	thermal resistance from heatsink to ambient		18	K/W

Note

1. An external heatsink is necessary.



(1) Infinite heatsink.
(2) No heatsink.

Fig.3 Power derating curves.

Thermal protection

The internal thermal protection circuit gives a decrease of the slew rate at high temperatures: 10% decrease at 130 °C and 30% decrease at 145 °C (typical values on the spot of the thermal protection circuit).

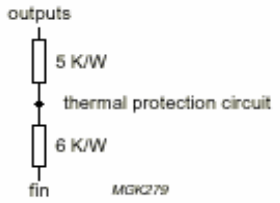


Fig.4 Equivalent thermal resistance network.

INTEGRAL

CHARACTERISTICS

Operating range: T_j = -20 to +150 °C; V_{DD} = 180 to 210 V. Test conditions: T_{amb} = 25 °C; V_{DD} = 200 V ; $V_{o(c1)} = V_{o(c2)} = V_{o(c3)}$ = ½ V_{DD}; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th(h-a)}$ = 18 K/W; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_q	quiescent supply current		5.9	6.9	7.9	mA
$V_{ref(int)}$	internal reference voltage		-	2.5	-	V
R_j	input resistance		-	3.6	-	kΩ
G	amplifier		47.5	51.0	55.0	
ΔG	gain difference		-2.5	0	+2.5	
$V_{o(c)}$	nominal output voltage at pins 7, 8 and 9 (DC value)	I_i = 0 μA	116	129	142	V
$\Delta V_{o(c)(offset)}$	differential nominal output offset voltage between pins 7 and 8, 8 and 9 and 9 and 7 (DC value)	I_i = 0 μA	-	0	5	V
$\Delta V_{o(c)(T)}$	output voltage temperature drift at pins 7, 8 and 9		-	-10	-	mV/K
$\Delta V_{o(c)(T)(offset)}$	differential output offset voltage temperature drift between pins 7 and 8, 8 and 9 and 7 and 9		-	0	-	mV/K
$I_{o(m)(offset)}$	offset current of measurement output	$I_{o(c)}$ = 0 μA 1.5 V < V_i <5.5 V 3 V < $V_{o(m)}$ < 6 V	-50	-	+50	μA
$\Delta I_{o(m)} / \Delta I_{o(c)}$	linearity of current transfer	-100 μA < $I_{o(c)}$ < 100 μA 1.5 V < V_i <5.5 V 3 V < $V_{o(m)}$ < 6 V	0.9	1.0	1.1	
		at CRT discharge; $I_{o(c)}$ = 1 mA 1.5 V < V_i <5.5 V 3 V < $V_{o(m)}$ < 5.4 V	-	1.0	-	
$I_{o(c)(max)}$	maximum peak output current (pins 7, 8 and 9)	50 V < $V_{o(c)}$ < V_{DD} – 50 V	-	20	-	mA
$V_{o(c)(min)}$	minimum output voltage (pins 7, 8 and 9)	V_i = 7.0 V	-	-	10	V
$V_{o(c)(max)}$	maximum output voltage (pins 7, 8 and 9)	V_i = 1.0 V	V_{DD} – 15	-	-	V
B_S	small signal bandwidth (pins 7, 8 and 9)	$V_{o(c)}$ = 60 V (p-p)	-	5.5	-	MHz
B_L	large signal bandwidth (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p)	-	4.5	-	MHz
t_{Pco}	cathode output propagation time 50% input to 50% output (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3);	-	60	-	ns
Δt_{Pco}	difference in cathode output propagation time 50% input to 50% output (pins 7and 8, 7 and 9 and 8	$V_{o(c)}$ = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3);	- 10	0	+ 10	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	and 9)					
$t_{o(r)}$	cathode output rise time 10% output to 90% output (pins 7, 8 and 9)	$V_{o(c)}$ = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3);	67	91	113	ns
$t_{o(f)}$	cathode output fall time 90% output to 10% output (pins 7, 8 and 9)	$V_{o(c)}$ = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3);	67	91	113	ns
t_{st}	Setting time 50% input to 99% < output < 101% (pins 7, 8 and 9)	$V_{o(c)}$ = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3);	-	-	350	ns
SR	slew rate between 50 V to (V_{DD} – 50 V) (pins 7, 8 and 9)	V_i = 4 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3);	-	900	-	V/μs
O_v	cathode output voltage overshoot (pins 7, 8 and 9)	V_i = 100 V (p-p) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3);	-	2	-	%
PSRR	Power supply rejection ratio	f < 50 kHz; note 1	-	55	-	dB
$\alpha_{ct(DC)}$	DC crosstalk between channels		-	50	-	dB

Notes

1. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.