IA16450 Preliminary Data Sheet

Universal Asynchronous Receiver/Transmitter

FEATURES

- **Form, Fit, and Function Compatible with the National® NS16450**
- **Packaging options available: 40 Pin Plastic or 44 Pin Plastic Leaded Chip Carrier**
- **Programmable Word Length, Stop Bits, and Parity**
- **Full Duplex Operation**
- **Programmable Baud Rate Generator**
  - **Division of any input clock by 1 to (2^{16} –1)**
  - **Generates Internal 16 x clock**
- **Programmable Serial-Interface**
  - **5-, 6-, 7- or 8-bit characters**
  - **Even, Odd, or No-Parity Bit Generation and Detection**
  - **1-, 1 ½-, or 2-Stop Bit Generation**
  - **Baud Generation of DC to 56k**
- **Prioritized Interrupt Control**
- **Internal Diagnostic/Loopback Capabilities**

The IA16450 uses **innovASIC**'s innovative new ***f*³ Program** to provide industry with parts that other vendors have declared obsolete. By specifying parts through this program a customer is assured of never having a component become obsolete again. This advanced information sheet assumes the original part has been designed in, and so provides a summary of capabilities only. For new designs contact **innovASIC** for more detailed information.

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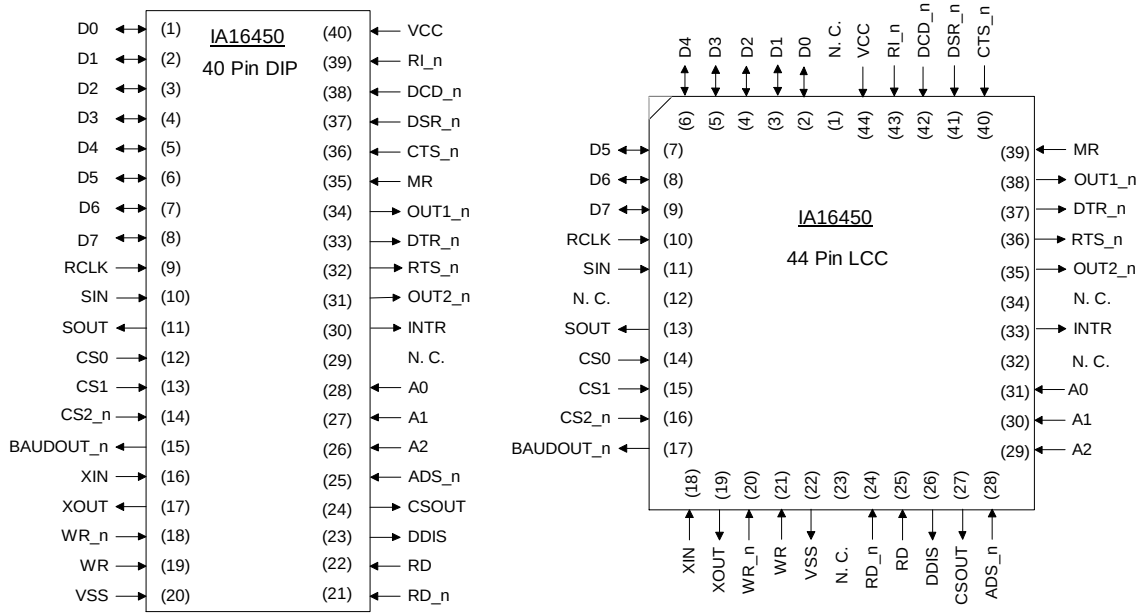
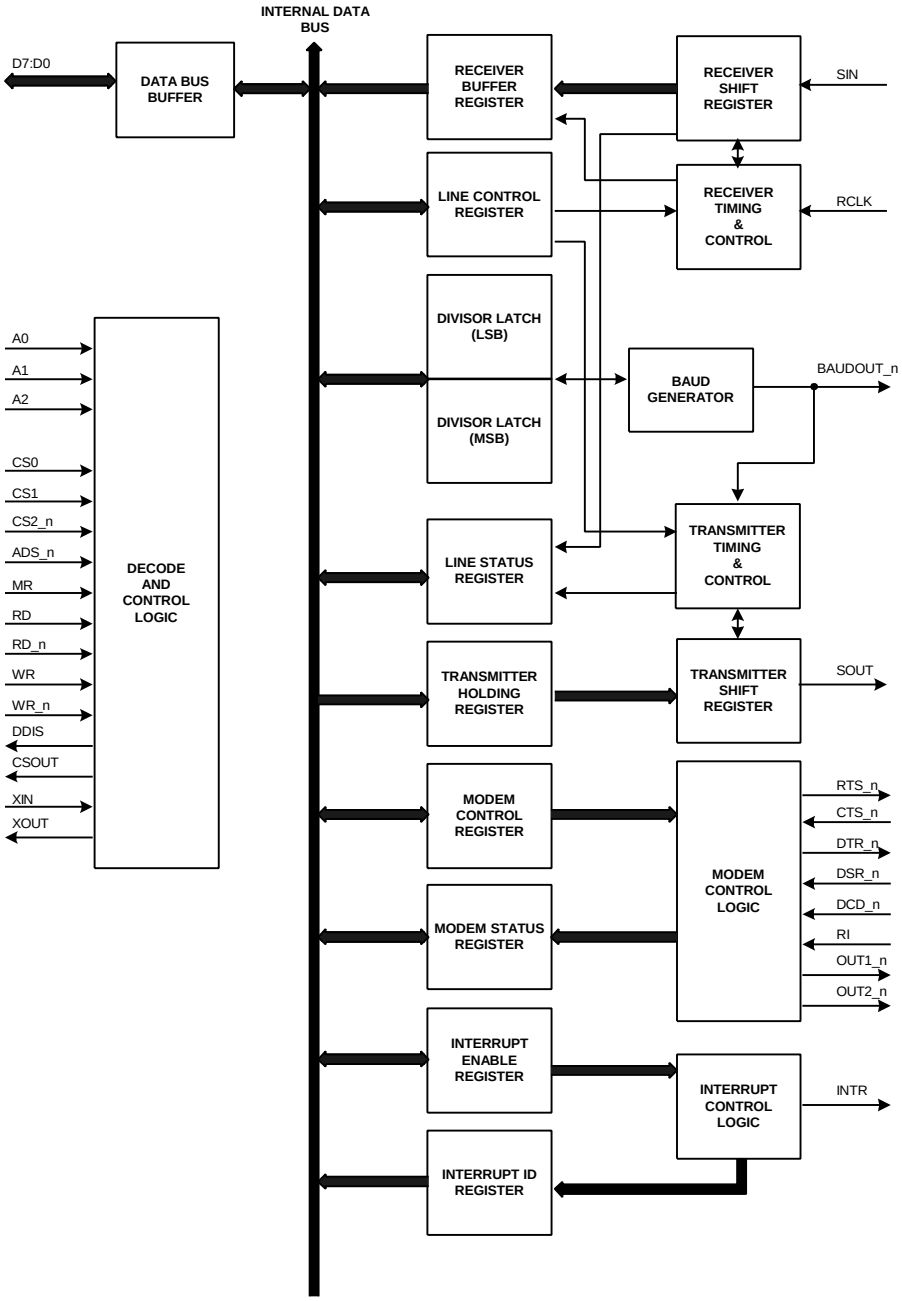
Package Pinout



IA16450 Preliminary Data Sheet
Universal Asynchronous Receiver/Transmitter

The IA16450 is a form, fit and function compatible part to the National NS16450 Univeral Asynchronous Receiver/Transmitter. The IA16450 function receives and transmits data in a variety of configurations including 5, 6, 7 or 8 bit data words, odd, even or no parity, and 1, 1.5, and 2 stop bits. This megafunction includes an internal Baud Rate Generator and Interrupt Control. A block diagram is shown in Figure 1.

Functional Block Diagram
Figure 1



I/O Signal Description

Table 1 below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provided**.** Table 2 refers to the address register map. Table 3 refers to the Preliminary A. C. Characteristics. Figure 2 illustrates the Preliminary Timing Waveforms for this device. Environmental/Qualification Levels are listed in Table 4.

Table 1

Name	Type	Description
MR	I	Master Reset - Active high - Clears all registers (except the receiver buffer, transmitter holding and divisor latches) to their initial state. Resets internal control logic to its initial state
A(2:0)	I	Register Address - Active high - This bus selects one of the internal UART registers (refer to table 1). Note the state of the divisor latch access bit (DLAB - the msb of the line control register) must be set high to access the divisor latches and low to access the receiver buffer or the interrupt enable register.
DIN(7:0)	I	Data Input Bus - Active high - Serves as input data when writing to internal UART registers.
CS0	I	Chip Select 0 - Active high - When CS0, CS1 and CS2 are active the megafunction is selected. Read and write transactions to internal UART registers are then possible.
CS1	I	Chip Select 1 - Active high - When CS0, CS1 and CS2 are active the megafunction is selected. Read and write transactions to internal UART registers are then possible.
CS2_n	I	Chip Select 2 - Active low - When CS0, CS1 and CS2 are active the megafunction is selected. Read and write transactions to internal UART registers are then possible.
ADS_n	I	Address Strobe - Active low - Gating signal to the Address input latch. The positive edge of ADS_n latches the state of the register address bus into the Address input latch. If address signals are guaranteed to be stable for the duration of a read or write cycle, ADS_n may be tied low thus forcing the Address input latch to be transparent.
RD	I	Read Control - Active High - when RD is high or RD_n is low and the UART is selected, read transactions from internal UART registers are possible.

Name	Type	Description
RD_n	I	Read Control - Active low - when RD is high or RD_n is low and the UART is selected, read transactions from internal UART registers are possible.
WR	I	Write Control - Active High - when WR is high or WR_n is low and the UART is selected, write transactions to internal UART registers are possible.
WR_n	I	Write Control - Active low - when WR is high or WR_n is low and the UART is selected, write transactions to internal UART registers are possible.
SIN	I	Serial Data Input - Active High - Receive data to the UART
RCLK	I	Receive Clock - The 16x baud rate clock used by the receiver section of the UART.
CTS_n	I	Clear To Send - Active Low - Active state indicates that the MODEM or data set is ready to exchange data. A change in state of this input is recorded in the DCTS bit (bit 0) of the MODEM Status register. Whenever CTS_n changes state, an interrupt is generated if the MODEM Status interrupt is enabled. The complement of this input is recorded in the CTS (bit 4) bit of the MODEM Status register
DSR_n	I	Data Set Ready - Active Low - Active state indicates that the MODEM or data set is ready to establish the communications link with the UART. A change in state of this input is recorded in the DDSR bit (bit 1) of the MODEM Status register. Whenever DSR_n changes state, an interrupt is generated if the MODEM Status interrupt is enabled. The complement of this input is recorded in the DSR (bit 5) bit of the MODEM Status register
DCD_n	I	Data Carrier Detect - Active Low - Active state indicates that the data carrier has been detected by the MODEM or data set. A change in state of this input is recorded in the DDCD bit (bit 3) of the MODEM Status register. Whenever DCD_n changes state, an interrupt is generated if the MODEM Status interrupt is enabled. The complement of this input is recorded in the DCD (bit 7) bit of the MODEM Status register

Name	Type	Description
RI_n	I	Ring Indicator - Active Low - Active state indicates that the ring signal has been detected by the MODEM or data set. A change in state of this input is recorded in the TERI bit (bit 2) of the MODEM Status register. Whenever DSR_n changes state, an interrupt is generated if the MODEM Status interrupt is enabled. The complement of this input is recorded in the RI (bit 6) bit of the MODEM Status register
DOUT(7:0)	O	Data Output Bus - Active high - Serves as output data when reading from internal UART registers.
DDIS	O	Driver Disable - Active High - Active State indicates that the CPU is reading data from the UART. This output is intended as a disable or direction control between the UART and CPU.
CSOUT	O	Chip Select Output - Active High - Active State indicates that the megafunction has been selected by use of the CS0, CS1 and CS2_n inputs.
SOUT	O	Serial Data Out - Active High - Serial (transmit) data out. This signal is set to the marking (logic 1) state upon master reset.
BAUDOUT_n	O	Baud Out - Active Low - The 16x baud rate clock used by the transmitter section of the UART. This output is controlled by the programmable baud rate generator.
RTS_n	O	Request to Send - Active Low - This output indicates that the UART is ready to exchange data. This output is controlled by writing to the RTS (bit 1) bit of the control register.
DTR_n	O	Data Terminal Ready - Active Low - This output indicates that the UART is ready to establish a communications link. This output is controlled by writing to the DTR (bit 0) bit of the control register.
OUT1_n	O	Discrete Output - Active Low - One of two user-programmable discrete outputs. This output is controlled by writing to the OUT1 (bit 2) bit of the control register.
OUT2_n	O	Discrete Output - Active Low - One of two user-programmable discrete outputs. This output is controlled by writing to the OUT2 (bit 3) bit of the control register.
INTR	O	Interrupt - Active High - Indicates that an enabled interrupt has had its interrupt condition met.

Name	Type	Description
XIN	I	External Crystal Input. This signal iniput is used in conjuction with XOUT to form a feedback circuit for the baud rate generator's oscillator. If a clock signal will be generated off-chip, then it should drive the baud rate generator through this pin
XOUT	O	External Crystal Output. This signal output is used in conjuction with XIN to form a feedback circuit for the baud rate generator's oscillator. If the clock signal will be generated off-chip, then this pin is unused.
VSS	P	Ground.
VCC	P	+5V power.

IA16450 Register Address Map

Table 2

DLAB	A2	A1	A0	REGISTER DESCRIPTION
0	0	0	0	Receiver Buffer - Read Only Transmitter Holding Register - Write Only
1	0	0	0	Divisor Latch (LSB)
0	0	0	1	Interrupt Enable Register
1	0	0	1	Divisor Latch (MSB)
X	0	1	0	Interrupt ID Register
X	0	1	1	Line Control Register
X	1	0	0	MODEM Control Register
X	1	0	1	Line Status Register
X	1	1	0	MODEM Status Register
X	1	1	1	Scratch

AC Electrical Characteristics

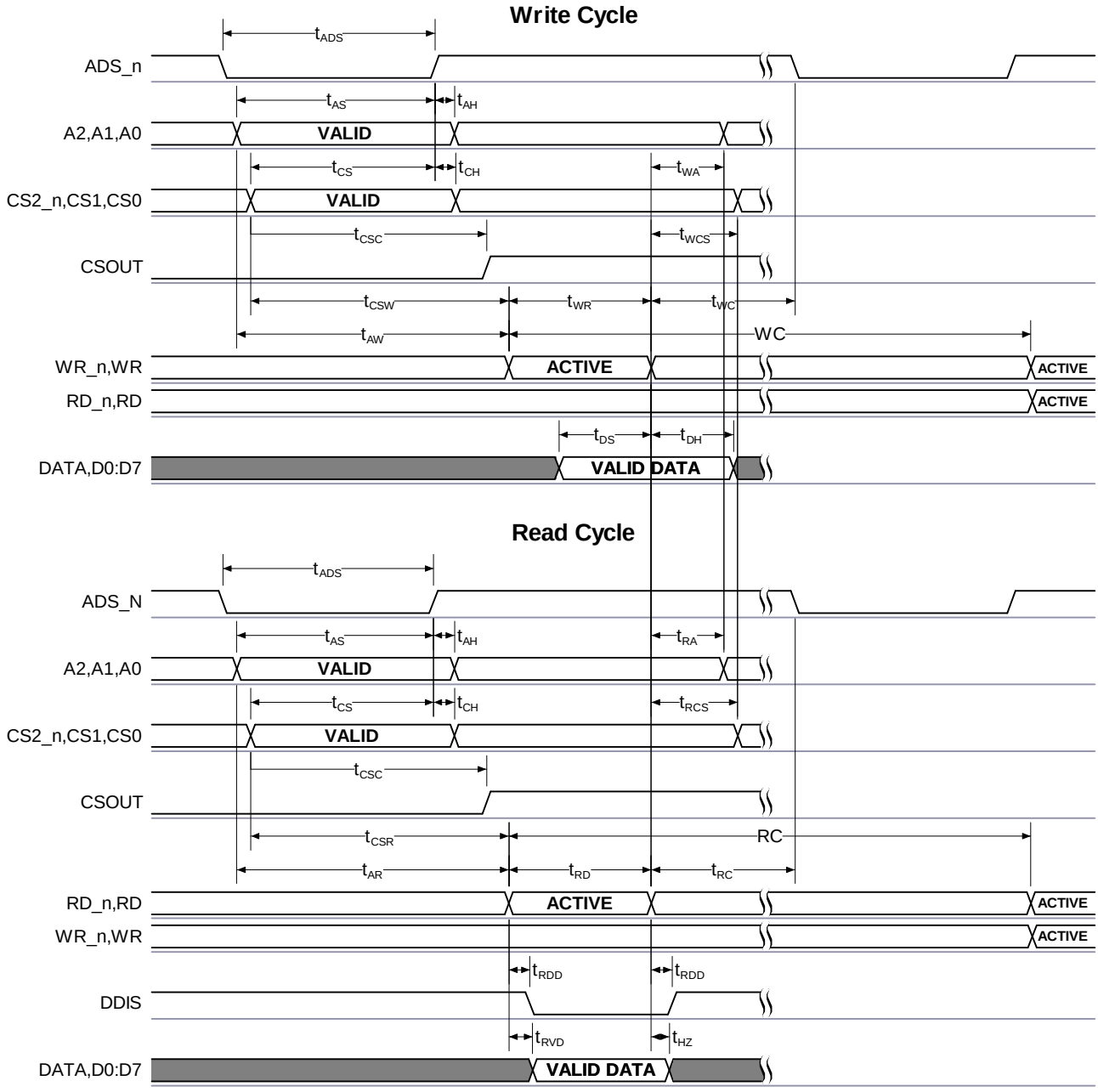
Table 3

Symbol	Parameter	Min	Max
t_{ADS}	Address Strobe Width	25	
t_{AH}	Address Hold Time	0	
t_{AR}	RD, RD_n Delay from Address (Note 1)	20	
t_{AS}	Address Setup Time	25	
t_{AW}	WR, WR_n Delay from Address (Note 1)	20	
t_{CH}	Chip Select Hold Time	0	
t_{CS}	Chip Select Setup Time	25	
t_{CSC}	Chip Select Output Delay from Select (Note 1)		33
t_{CSR}	RD, RD_n Delay fron Select (Note 1)	20	
t_{CSW}	WR, WR_n Delay fron Select (Note 1)	20	
t_{DH}	Data Hold Time	10	
t_{DS}	Data Setup Time	20	
t_{HZ}	RD, RD_n to Floating Data Delay	0	25
t_{RA}	Address Hold Time from RD, RD_n (Note 1)	0	
t_{RC}	Read Cycle Delay	36	
t_{RCS}	Chip Select Hold Time from RD, RD_n (Note 1)	0	
t_{RD}	RD, RD_n Strobe Width	60	
t_{RDD}	RD, RD_n to Driver Disable Delay		20
t_{RVD}	Delay from RD, RD_n to Data		31
t_{WA}	Address Hold Time from WR, WR_n	0	
t_{WC}	Write Cycle Delay	36	
t_{WCS}	Chip Select Hold Time from WR, WR_n (Note 1)	0	
t_{WR}	WR, WR_n Strobe Width	60	
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$	115	
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$	115	

Note 1: Applicable only when ADS_n is tied low.

Timing Waveforms

Figure 2

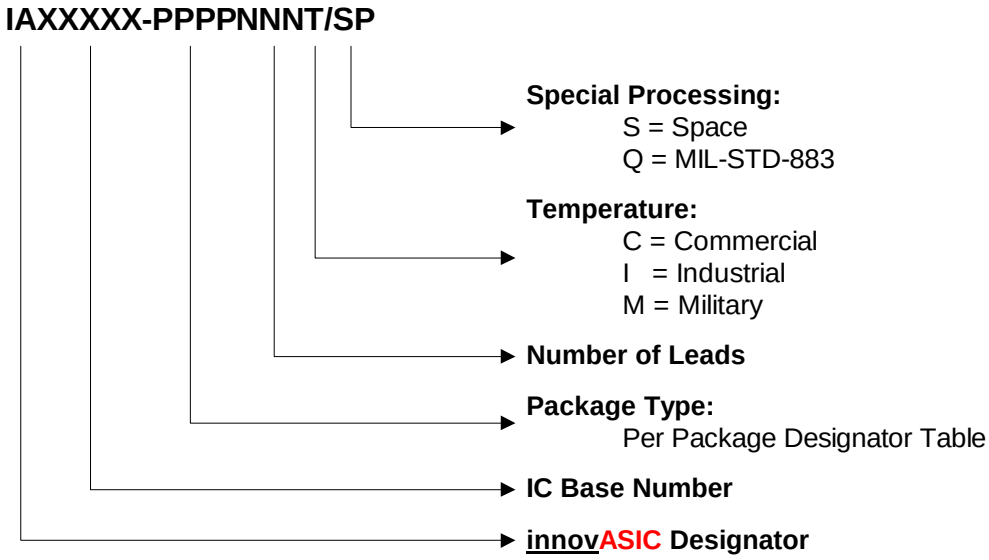


Qualification Levels

Table 4

Part Number	Environmental / Qual Level
IA16450-PDW40C	Commercial
IA16450-PLC44C	Commercial
IA16450-PDW40I	Industrial
IA16450-PLC44I	Industrial

The following diagram depicts the **innovASIC** Product Identification Number.



Package Designator Table

Package Type	innovASIC Designator
Ceramic side brazed Dual In-line	CDB
Cerdip with window	CDW
Ceramic leaded chip carrier	CLC
Cerdip without window	CD
Ceramic leadless chip carrier	CLL
PLCC	PLC
Plastic DIP standard (300 mil)	PD
Plastic DIP standard (600 mil)	PDW
Plastic metric quad flat pack	PQF
Plastic thin quad flat pack	PTQ
Skinny Cerdip	CDS
Small outline plastic gull-wing(150 mil body)	PSO
Small outline medium plastic gull-wing (207 mil body)	PSM
Small outline narrow plastic gull wing (150 mil body)	PSN
Small outline wide plastic gull wing (300 mil body)	PSW
Skinny Plastic Dip	PDS
Shrink small outline plastic (5.3mm .208 body)	PS
Thin shrink small outline plastic	PTS
Small outline large plastic gull wing (330 mil body)	PSL
Thin small outline plastic gull-wing (8 x 20mm) [TSOP]	PST
PGA	CPGA
BGA	CBGA

Contact **innovASIC** for other package and processing options.