40MHz, 32-Channel Serial to Parallel Converter with Push-Pull Outputs

Ordering Information

	Package Options		
Device	**64 Pin Plastic Gullwing**	**80-Lead Ceramic Gullwing**	**Die in Wafer Form**
HV76	HV7620PG	HV7620DG	HV7620XW

Features

- ❑ Processed with HVCMOS® technology
- ❑ 5V CMOS logic and 12V supply rail
- ❑ Output voltage up to 200V
- ❑ Low power level shifting
- ❑ Source/sink current minimum 50mA
- ❑ 40MHz equivalent data rate
- ❑ Chip select
- ❑ Polarity function
- ❑ Forward and reverse shifting options (DIR pin)
- ❑ Latched outputs

General Description

The HV76 is a low-voltage serial to high-voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for color AC plasma displays.

The device has 4 parallel 8-bit shift registers permitting data rate 4 times the speed of one. The data are clocked in simultaneously on all four data inputs with a single clock. Data are shifted in on a low to high transition of the clock. The latches and control logic perform the output enable function.

The DIR pin causes clockwise (CW) shifting of the data when connected to V_{DD1}, and counterclockwise (CCW) shifting when connected to GND. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable) input. Transfer of data from the shift registers to the latches occurs when the $\overline{LE}$ input is high. Data is stored in the latches when $\overline{LE}$ is low. The current source on the logic inputs provides active pull up when the input pins are open.

Absolute Maximum Ratings

Supply voltage[1], V_{DD1}		-0.5V to +15V
Supply voltage[1], V_{DD2}		-0.5V to +15V
Supply voltage[1], V_{PP}		-0.5V to +225V
Logic input levels[1]		-2.0V to V_{DD1}+2.0V
Continuous total power dissipation[2]	Plastic	1200mW
	Ceramic	1900mW
Operating temperature range	Plastic	-40°C to +85°C
	Ceramic	-55°C to 125°C
Storage temperature range		-65°C to +150°C

Notes:

1. All voltages are referenced to GND.
2. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 19mW/°C for ceramic.

02/96/022

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics (V_{DD1} = 5V, V_{DD2} = 12V, V_{PP} = 200V and T_A = 25°C)

Symbol	Parameters	Min	Max	Units	Condition
I_{DD1}	V_{DD1} supply current		5	mA	f_{CLK} =10MHz
I_{DD2}	V_{DD2} supply current		20	mA	V_{DD2} = V_{DD2} max f_{CLK} = 10 MHz
I_{PP}	High voltage supply current		2	mA	All output high or low
I_{DD1Q}	Quiescent V_{DD1} supply current		100	μA	All input = V_{DD1}
I_{DD2Q}	Quiescent V_{DD2} supply current		100	μA	All input = V_{DD1}
V_{OH}	High-level output	185		V	I_O = -50mA
V_{OL}	Low-level output		20	V	I_O = 50mA
I_{IH}	High-level logic input current		1.0	μA	V_{IN} = V_{DD1}
I_{IL}	Low-level logic input current		-10	μA	V_{IN} = 0V
V_{GG}	HVGND to LVGND voltage difference	-1.0	1.0	V	

AC Characteristics (Logic signal inputs and data inputs have t_r, t_f ≤ 5ns. V_{DD1} = 5V or 12V, V_{DD2} = 12V, V_{PP} = 200V)

Symbol	Parameters		Min	Max	Units	Condition
f_{CLK}	Clock frequency	V_{DD1} = 5V		10	MHz	Per register C_L = 15pF
		V_{DD1} = 12V		5	MHz	Per register C_L = 15pF
t_{WL}, t_{WH}	Clock width high or low		40		ns	
t_{SU}	Data set-up time		20		ns	
t_H	Data hold time		20		ns	
t_{ON}, t_{OFF}	Time from $\overline{LE}$ to HV_{OUT}			275	ns	C_L = 15pF
t_{WLE}	Width of $\overline{LE}$ pulse		25		ns	
t_{DLE}	Delay time clock to $\overline{LE}$ low to high		50		ns	
t_{SLE}	$\overline{LE}$ setup time before clock rises		20		ns	
t_{DLF}, t_{DLN}	$\overline{BL}$ or CS low to high to HV_{OUT}			250	ns	
t_{COF}, t_{CON}	Clock to HV_{OUT}			275	ns	
t_{DLH}	Delay time clock to data low to high			100	ns	C_L = 15pF
t_{DHL}	Delay time clock to data high to low			100	ns	C_L = 15pF

Recommended Operating Conditions

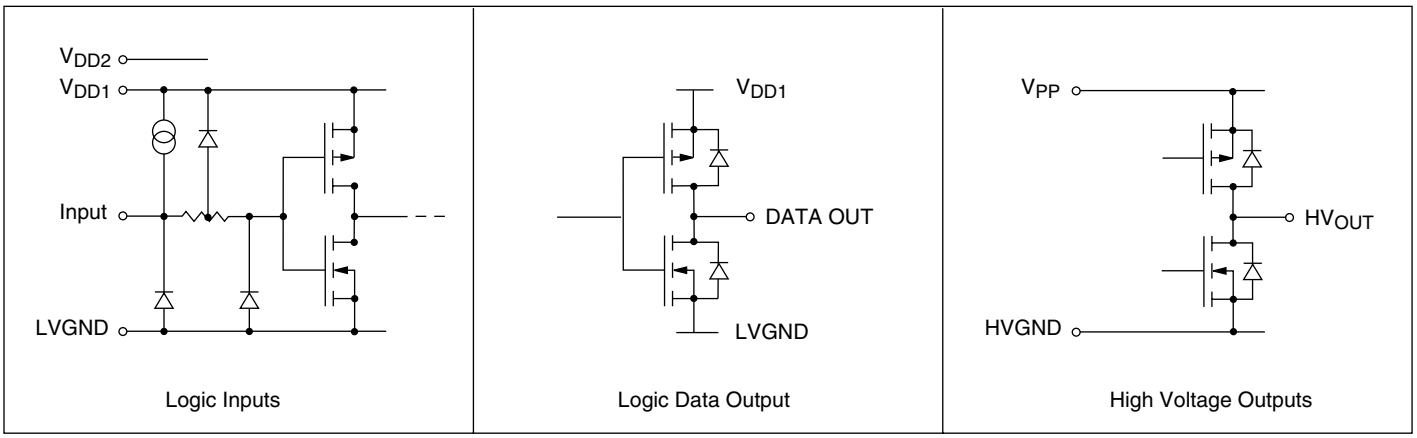
Symbol	Parameters		Min	Max	Unit
V_{DD1}	Logic supply voltage		4.5	V_{DD2}	V
V_{DD2}	12V supply voltage		10.8	13.2	V
V_{PP}	High voltage supply voltage		50	200	V
V_{IH}	High-level input voltage		V_{DD1}-0.5V	V_{DD1}	V
V_{IL}	Low-level input voltage		0	0.5	V
f_{CLK}	Clock frequency	V_{DD1} = 5V		10	MHz
		V_{DD1} = 12V		5	MHz
T_A	Operating free-air temperature	Plastic	-40	+85	°C
		Ceramic	-55	+125	°C
I_{OD}	Allowable pulsed current through ouptut diodes[1]			500	mA
$I_{GND(Vpp)}$	Allowable pulsed V_{PP} or HVGND current[1]			16	A
$V_{PP(SLEW)}$[2]	Slew rate of V_{PP}			340	V/μs

Notes:

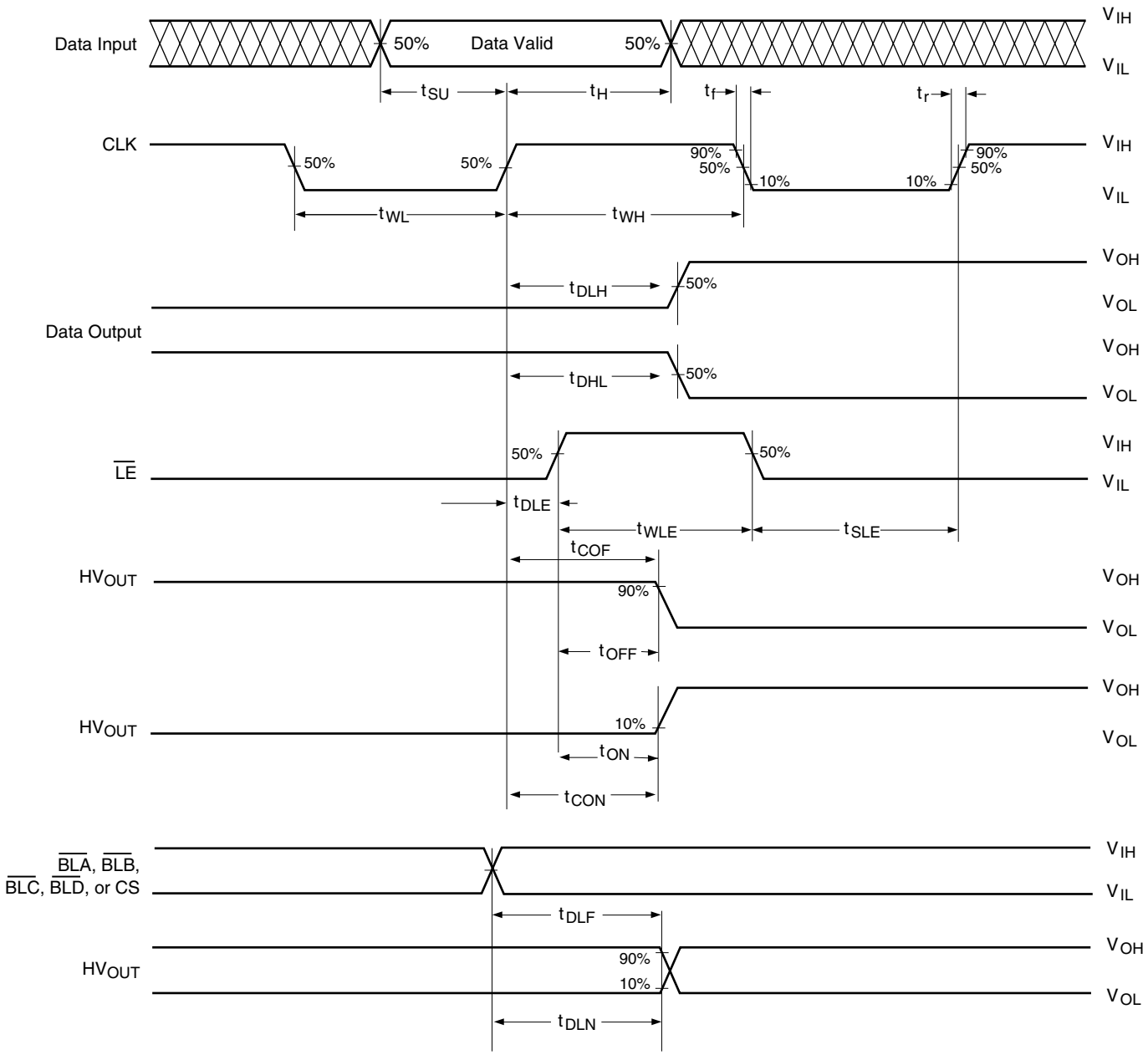
1.The current pulse width = 500ns, duty cycle = 5%.

2.This device cannot be hot-switched for output frequency greater than 500Hz. For output frequency greater than 500Hz, V_{PP} must be ramped.

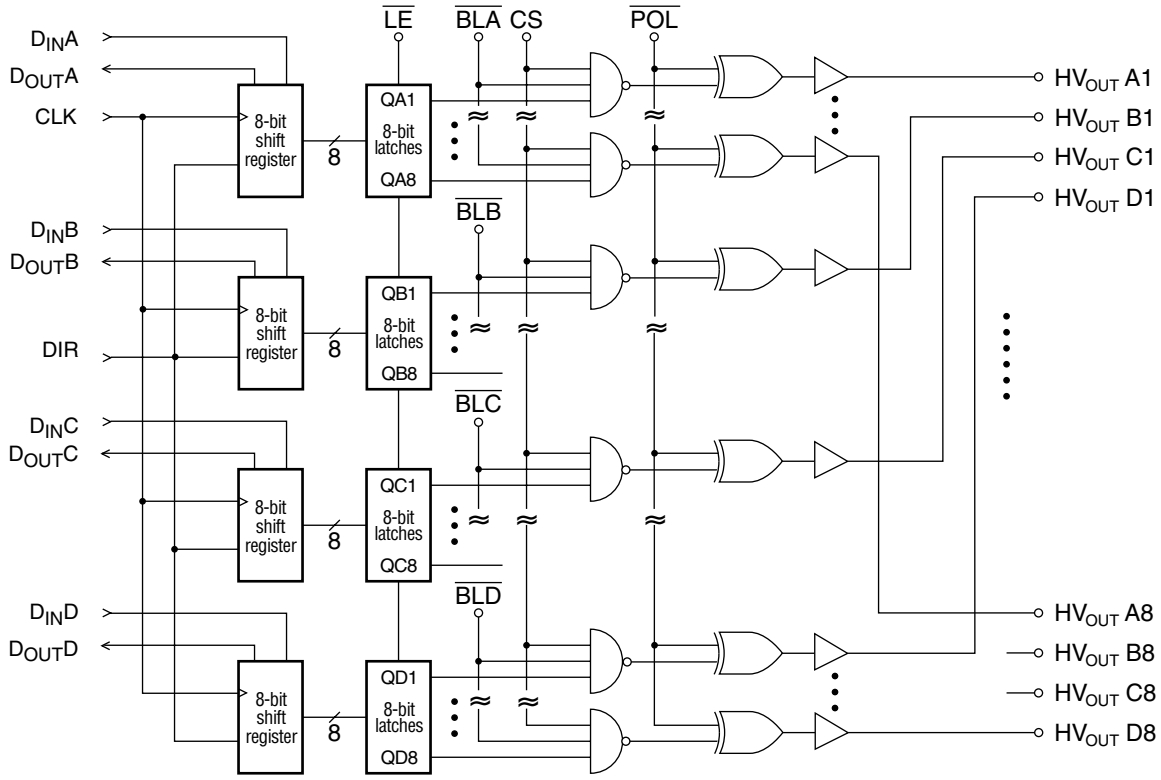
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs													HV Outputs			
	$D_{IN}A$	$D_{IN}B$	$D_{IN}C$	$D_{IN}D$	CLK	$\overline{LE}$	DIR	$\overline{BLA}$	$\overline{BLB}$	$\overline{BLC}$	$\overline{BLD}$	CS	$\overline{POL}$	A	B	C	D
All O/P High	X	X	X	X	X	X	X	X	X	X	X	L	L	H	H	H	H
All O/P Low	X	X	X	X	X	X	X	X	X	X	X	L	H	L	L	L	L
"A" Outputs Low	X	X	X	X	X	X	X	L	X	X	X	X	H	L	*	*	*
Normal Polarity	X	X	X	X	X	X	X	H	H	H	H	H	H	No Inversion			
Outputs Inverted	X	X	X	X	X	X	X	H	H	H	H	H	L	Inversion			
Transparent Mode	H	L	L	L	↑	H	X	H	H	H	H	H	H	H	L	L	L
Data Stored	X	X	X	X	X	L	X	H	H	H	H	H	H	Stored Data			
Shift CW	X	X	X	X	↑	H	H	H	H	H	H	H	X	A_N $\vec{A}_{N+1}$	B_N $\vec{B}_{N+1}$	C_N $\vec{C}_{N+1}$	D_N $\vec{D}_{N+1}$
Shift CCW	X	X	X	X	↑	H	L	H	H	H	H	H	X	A_N $\vec{A}_{N-1}$	B_N $\vec{B}_{N-1}$	C_N $\vec{C}_{N-1}$	D_N $\vec{D}_{N-1}$

Notes:

H = High level, L = Low level, X = Irrelevant, ↑ = Low to high transition.

* = Dependent on previous stage's state before the last CLK ↑ for last $\overline{LE}$ high.

Power-up sequence:

GND (HV, LV)
V_{DD2}
V_{DD1}
Logic Input Signals
V_{PP}

To power down reverse the sequence above.

The V_{PP} should not drop below V_{DD} or float during operation.

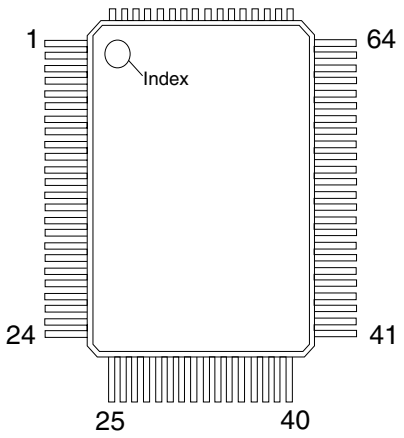
Pin Configurations

HV76

Pin	Function	Pin	Function
1	HVGND	33	CS
2	V_{PP}	34	$D_{OUT}B$
3	$HV_{OUT}D8$	35	$D_{IN}B$
4	$HV_{OUT}C8$	36	$D_{IN}A$
5	$HV_{OUT}B8$	37	$D_{OUT}A$
6	$HV_{OUT}A8$	38	$\overline{CLK}$
7	$HV_{OUT}D7$	39	$\overline{BLA}$
8	$HV_{OUT}C7$	40	$\overline{BLB}$
9	$HV_{OUT}B7$	41	V_{DD1}
10	$HV_{OUT}A7$	42	LVGND
11	$HV_{OUT}D6$	43	N/C
12	$HV_{OUT}C6$	44	HVGND
13	$HV_{OUT}B6$	45	HVGND
14	$HV_{OUT}A6$	46	V_{PP}
15	$HV_{OUT}D5$	47	$HV_{OUT}D4$
16	$HV_{OUT}C5$	48	$HV_{OUT}C4$
17	$HV_{OUT}B5$	49	$HV_{OUT}B4$
18	$HV_{OUT}A5$	50	$HV_{OUT}A4$
19	V_{PP}	51	$HV_{OUT}D3$
20	HVGND	52	$HV_{OUT}C3$
21	HVGND	53	$HV_{OUT}B3$
22	V_{DD2}	54	$HV_{OUT}A3$
23	$\overline{BLC}$	55	$HV_{OUT}D2$
24	$\overline{BLD}$	56	$HV_{OUT}C2$
25	$\overline{LE}$	57	$HV_{OUT}B2$
26	$D_{OUT}D$	58	$HV_{OUT}A2$
27	$D_{IN}D$	59	$HV_{OUT}D1$
28	$D_{IN}C$	60	$HV_{OUT}C1$
29	$D_{OUT}C$	61	$HV_{OUT}B1$
30	$\overline{POL}$	62	$HV_{OUT}A1$
31	LVGND	63	V_{PP}
32	DIR	64	HVGND

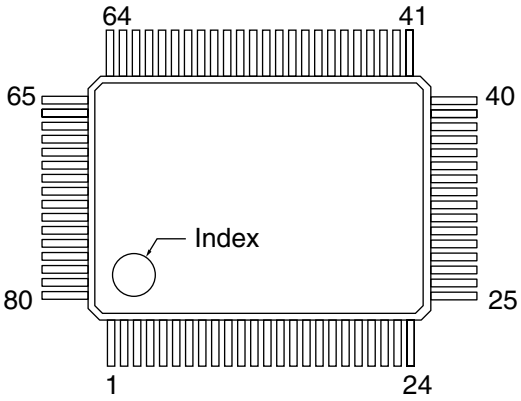
*Pins 65 to 80 are N/C (ceramic only)

Package Outline



top view

3-sided Plastic 64-pin Gullwing Package



top view

80-pin Ceramic Gullwing Package

Supertex inc.

1235 Bordeaux Drive, Sunnyvale, CA 94089
TEL: (408) 744-0100 • FAX: (408) 222-4895
www.supertex.com