

4.7A, 30V, 0.031 Ohm, N-Channel, Logic Level UltraFET Power MOSFET



This N-Channel power MOSFET is manufactured using the innovative UltraFET process. This advanced process technology achieves the

lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA76113.

Ordering Information

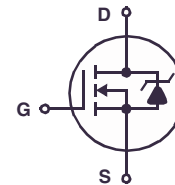
PART NUMBER	PACKAGE	BRAND
HUF76113T3ST	SOT-223	76113

NOTE: HUF76113T3ST is available only in tape and reel.

Features

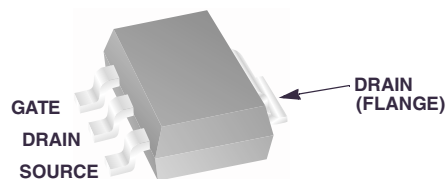
- Logic Level Gate Drive
- 4.7A, 30V
- Ultra Low On-Resistance, $r_{DS(ON)} = 0.031\Omega$
- Temperature Compensating PSpice® Model
- Temperature Compensating SABER™ Model
- Thermal Impedance SPICE Model
- Thermal Impedance SABER Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

SOT-223



HUF76113T3ST

Absolute Maximum Ratings $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

	HUF76113T3ST	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	30 V
Drain to Gate Voltage ($R_{\text{GS}} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	30 V
Gate to Source Voltage	V_{GS}	± 20 V
Drain Current		
Continuous ($T_A = 25^{\circ}\text{C}$, $V_{\text{GS}} = 10\text{V}$) (Figure 2) (Note 2)	I_{D}	4.7 A
Continuous ($T_A = 100^{\circ}\text{C}$, $V_{\text{GS}} = 5\text{V}$) (Note 2)	I_{D}	2.7 A
Continuous ($T_A = 100^{\circ}\text{C}$, $V_{\text{GS}} = 4.5\text{V}$) (Note 2)	I_{D}	2.6 A
Pulsed Drain Current	I_{DM}	Figure 4
Pulsed Avalanche Rating	E_{AS}	Figure 6
Power Dissipation (Note 2)	P_{D}	1.1 W
Derate Above 25°C		0.0091 $\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature	$T_{\text{J}}, T_{\text{STG}}$	-55 to 150 $^{\circ}\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_{L}	300 $^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_{\text{J}} = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_A = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS						
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25V, V _{GS} = 0V	-	-	1	μA
		V _{DS} = 25V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA
ON STATE SPECIFICATIONS						
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V
Drain to Source On Resistance	r _{DS(ON)}	I _D = 4.7A, V _{GS} = 10V (Figure 9, 10)	-	0.027	0.031	Ω
		I _D = 2.7A, V _{GS} = 5V (Figure 9)	-	0.033	0.038	Ω
		I _D = 2.6A, V _{GS} = 4.5V (Figure 9)	-	0.035	0.040	Ω
THERMAL SPECIFICATIONS						
Thermal Resistance Junction to Ambient	R _{θJA}	Pad Area = 0.173 in ² (Note 2)	-	-	110	°C/W
		Pad Area = 0.068 in ² (See TB377)	-	-	133	°C/W
		Pad Area = 0.026 in ² (See TB377)	-	-	157	°C/W
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)						
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≅ 2.6A, R _L = 5.8Ω, V _{GS} = 4.5V, R _{GS} = 18Ω (Figure 15)	-	-	90	ns
Turn-On Delay Time	t _{d(ON)}		-	12	-	ns
Rise Time	t _r		-	46	-	ns
Turn-Off Delay Time	t _{d(OFF)}		-	31	-	ns
Fall Time	t _f		-	31	-	ns
Turn-Off Time	t _{OFF}		-	-	95	ns

HUF76113T3ST

Electrical Specifications $T_A = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 15V, I _D ≡ 4.7A, R _L = 3.2Ω, V _{GS} = 10V, R _{GS} = 9.1Ω (Figure 16)	-	-	40	ns	
Turn-On Delay Time	t _{d(ON)}		-	4	-	ns	
Rise Time	t _r		-	21	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	31	-	ns	
Fall Time	t _f		-	25	-	ns	
Turn-Off Time	t _{OFF}		-	-	85	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 15V, I _D ≡ 2.7A, R _L = 5.5Ω I _{g(REF)} = 1.0mA (Figure 14)	-	17.0	20.5	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	9.5	11.5	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	0.73	0.90	nC
Gate to Source Gate Charge	Q _{gs}			-	1.50	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	4.30	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	625	-	pF	
Output Capacitance	C _{OSS}		-	310	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	60	-	pF	

NOTES:

- Rated with $R_{\theta JA} = 110^\circ\text{C/W}$ measured using FR-4 board with 0.173 in² copper at 1000 seconds.

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 4.7\text{A}$	-	-	1.25	V
		$I_{SD} = 2.7\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 2.7\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	44	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 2.7\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	46	nC

Typical Performance Curves

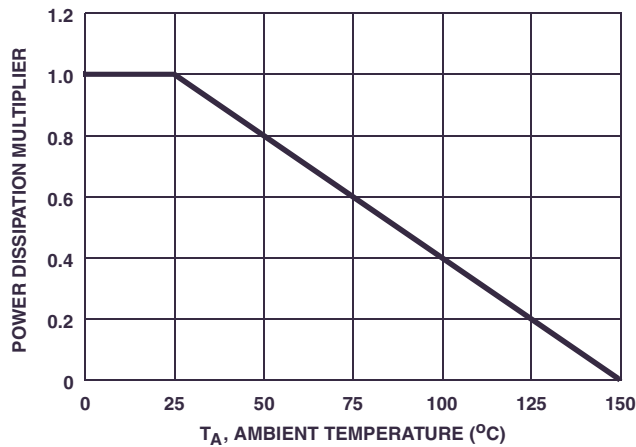


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

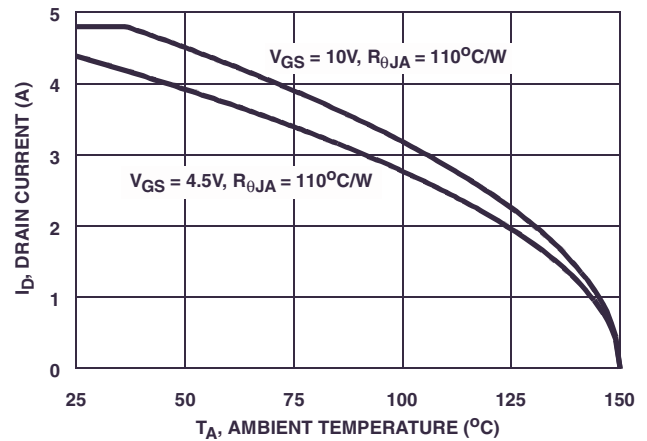
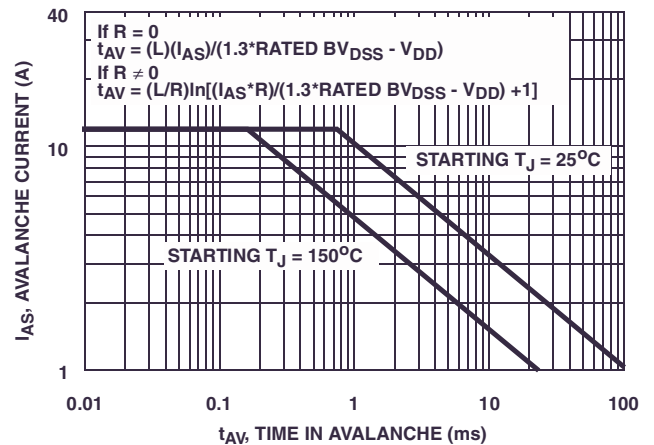
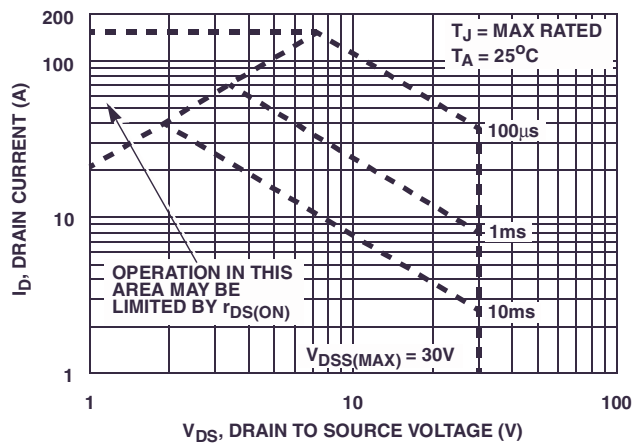
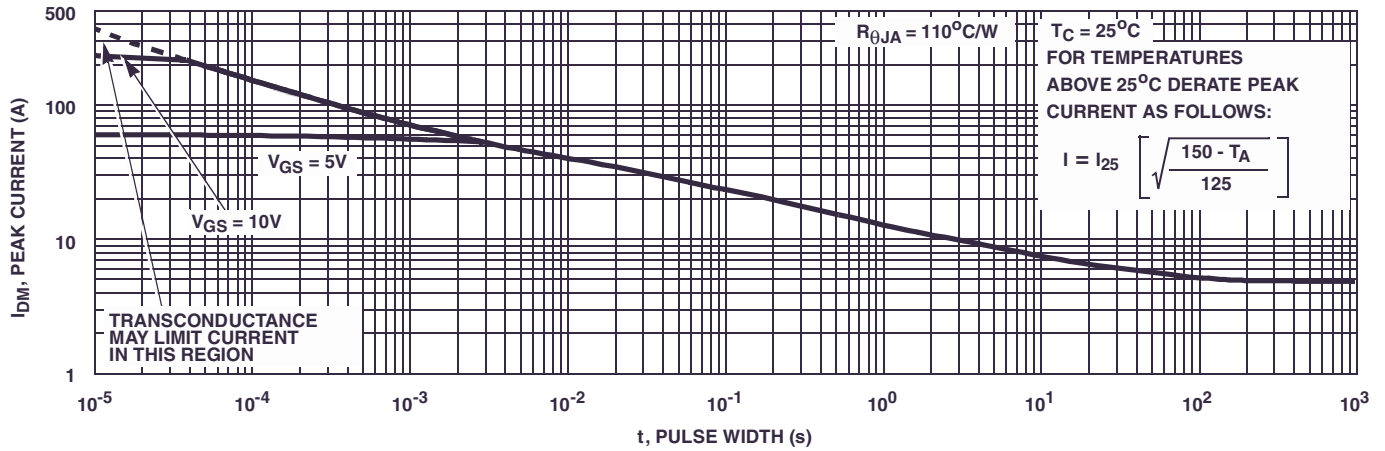
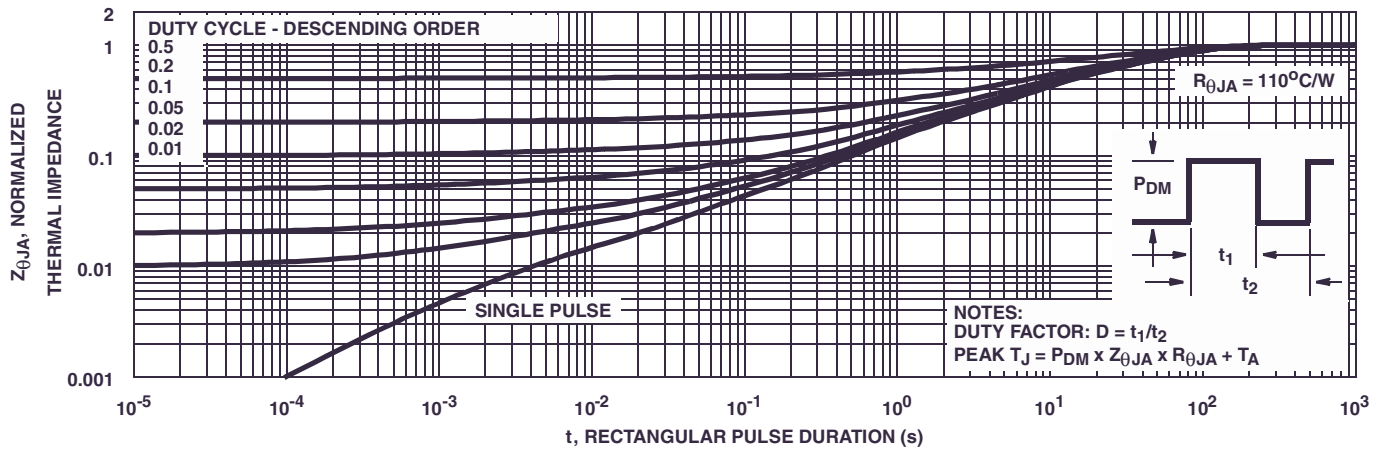


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

Typical Performance Curves (Continued)

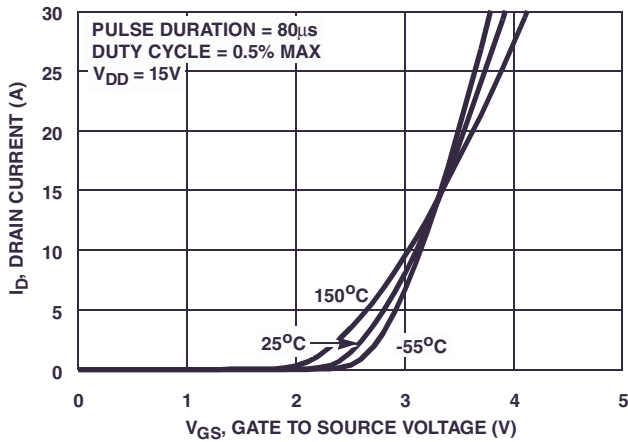


FIGURE 7. TRANSFER CHARACTERISTICS

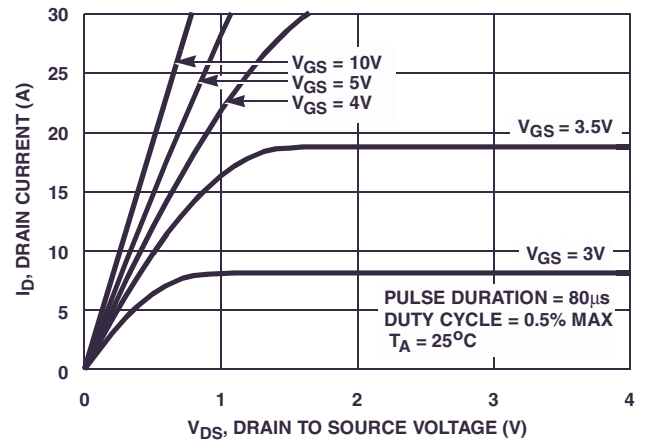


FIGURE 8. SATURATION CHARACTERISTICS

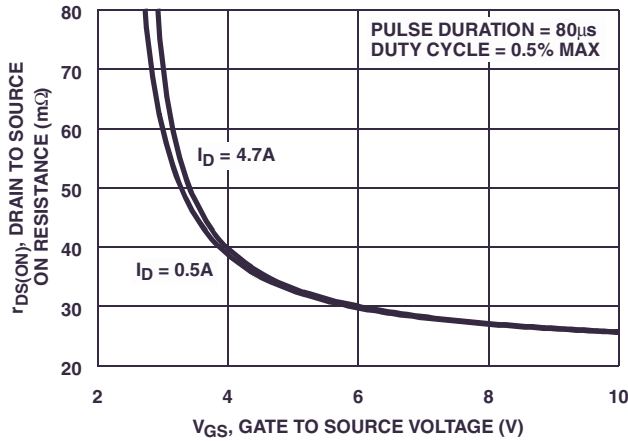


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

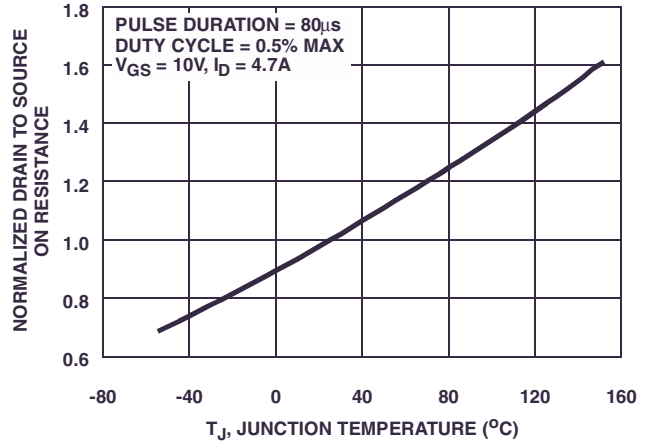


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

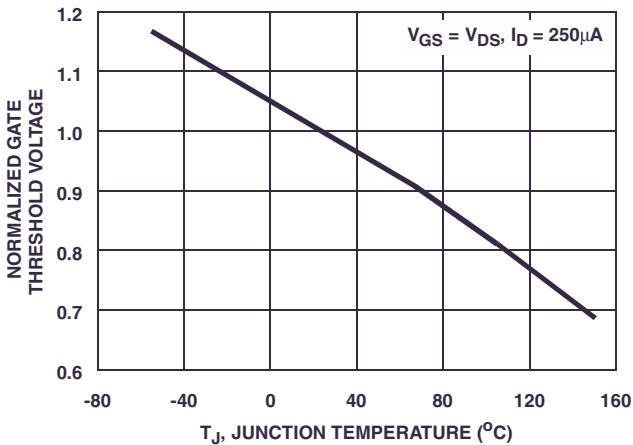


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

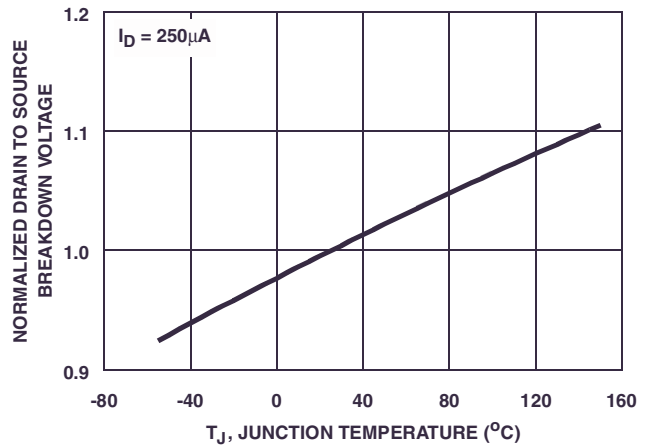


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

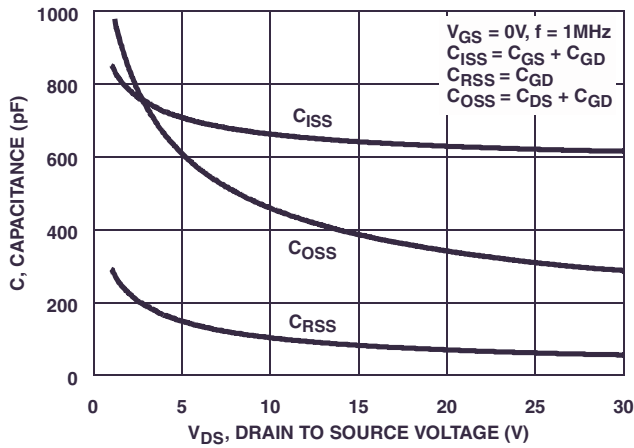
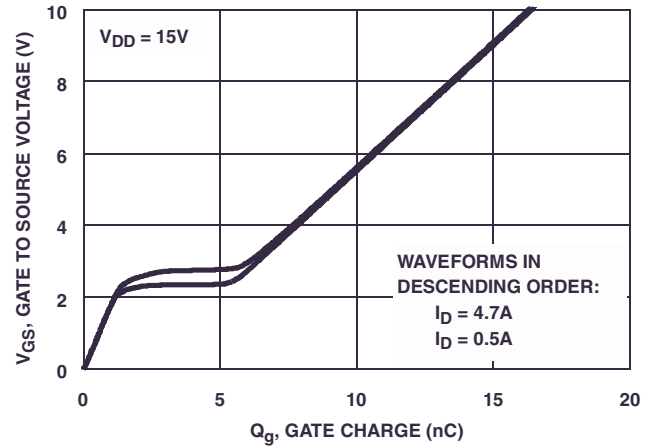


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

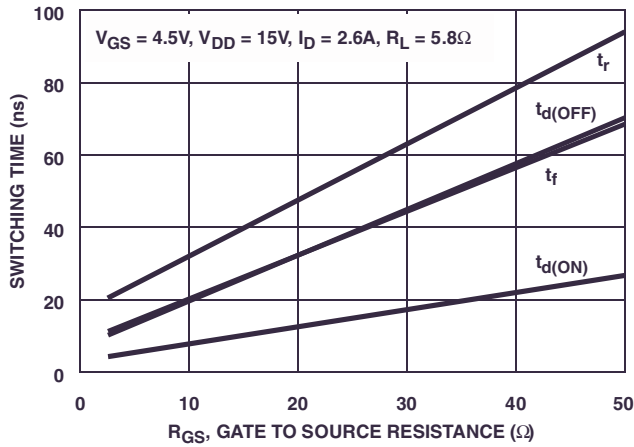


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

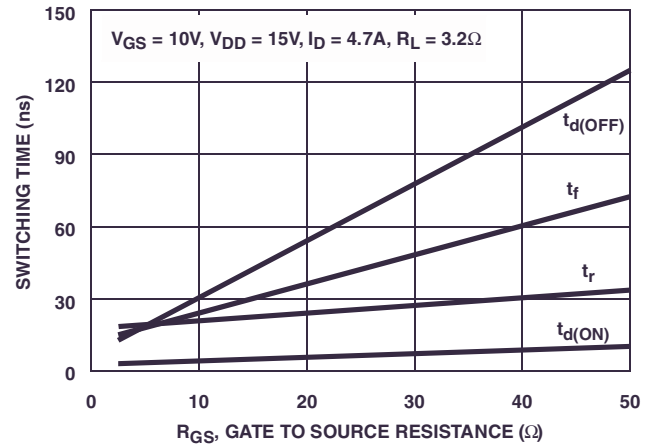


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

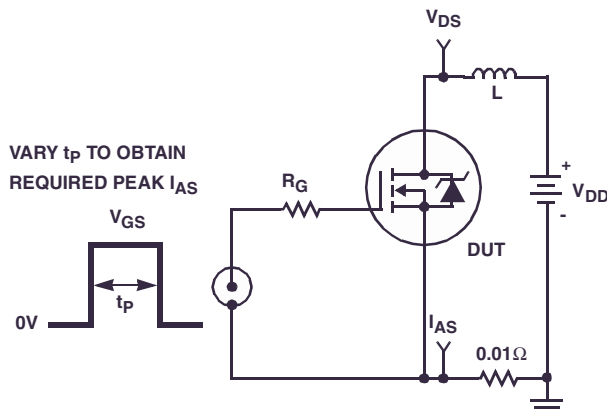


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

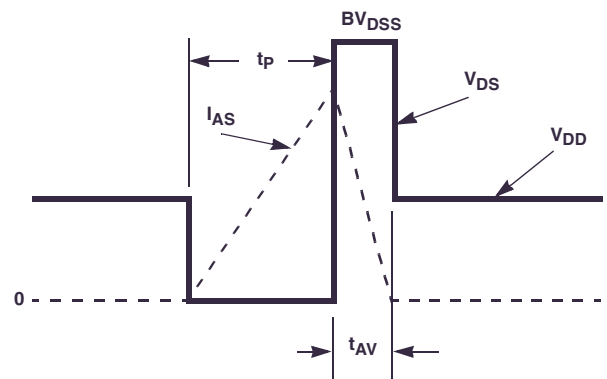


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

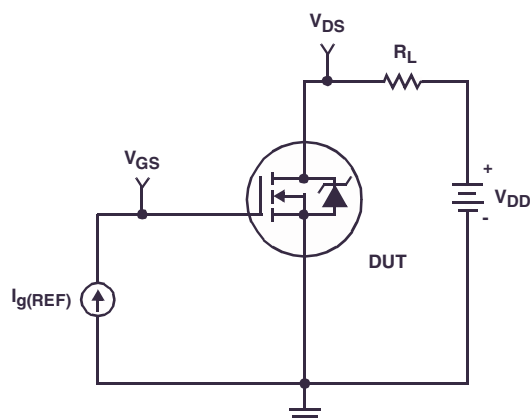


FIGURE 19. GATE CHARGE TEST CIRCUIT

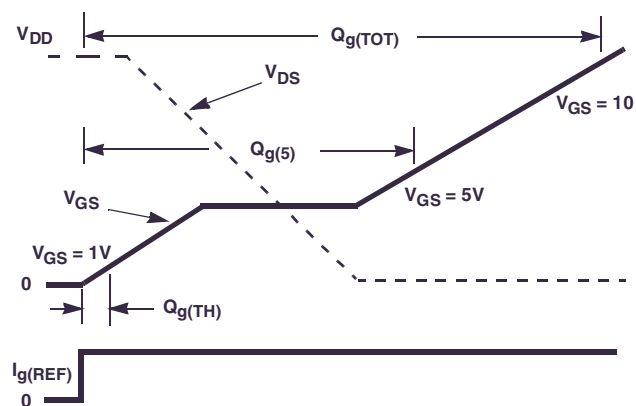


FIGURE 20. GATE CHARGE WAVEFORMS

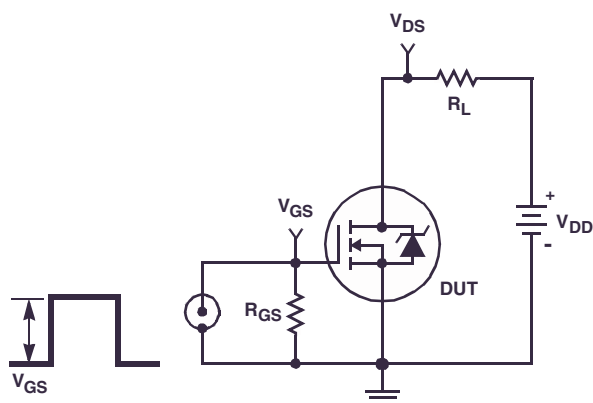


FIGURE 21. SWITCHING TIME TEST CIRCUIT

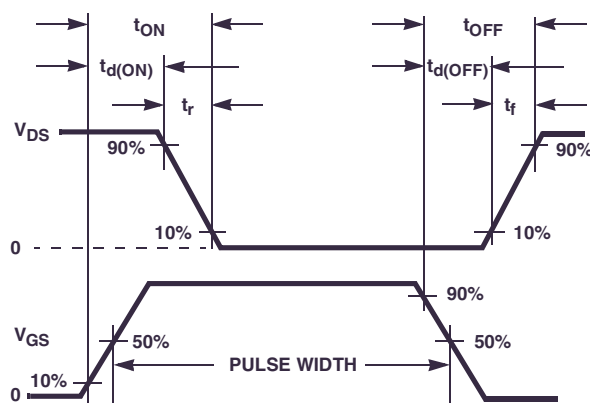


FIGURE 22. SWITCHING TIME WAVEFORM

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM} , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM} , in an application. Therefore the application's ambient temperature, T_A ($^{\circ}\text{C}$), and thermal resistance $R_{\theta JA}$ ($^{\circ}\text{C}/\text{W}$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the SOT-223 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 23 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve. Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM} . The smallest areas represent

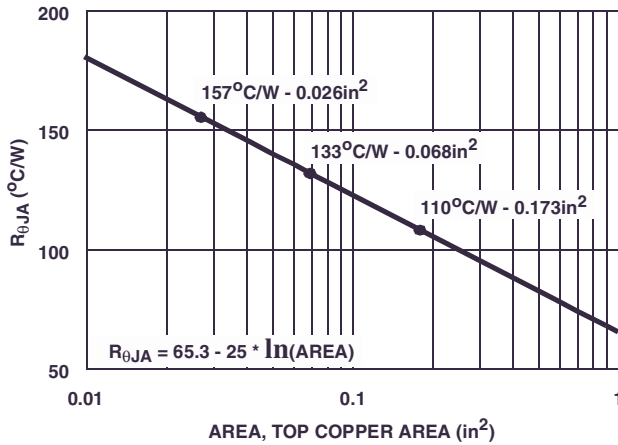


FIGURE 23. THERMAL RESISTANCE vs MOUNTING PAD AREA

the minimum bond pad area and the package outline area respectively as determined from the package diagram

Thermal resistances corresponding to other copper areas can be obtained from Figure 23 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 65.3 - 25 \times \ln(\text{Area}) \quad (\text{EQ. 2})$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 24 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, C THERM1 through C THERM5 and R THERM1 through R THERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

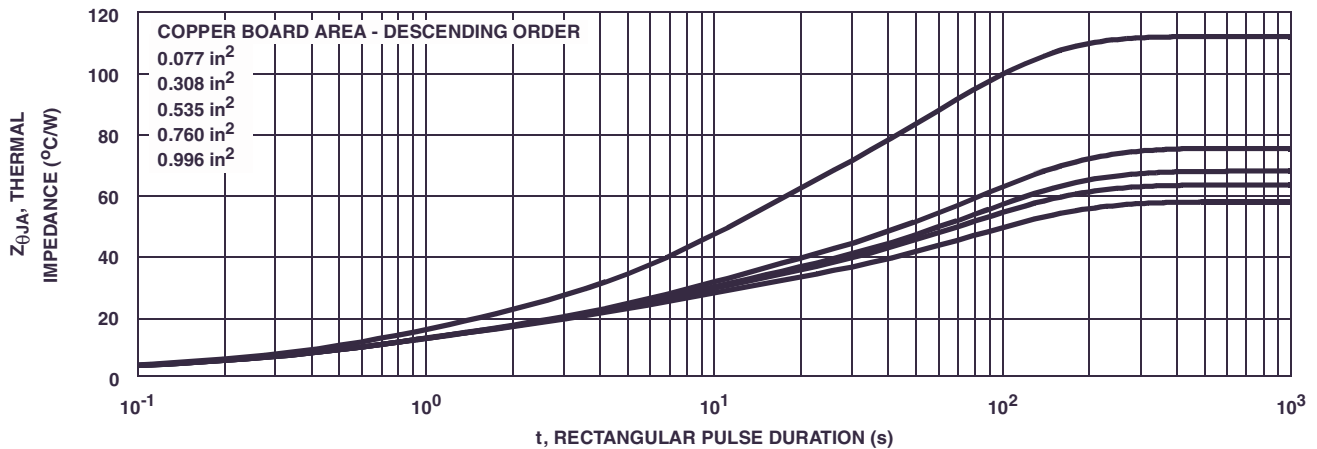


FIGURE 24. THERMAL IMPEDANCE vs MOUNTING PAD AREA

PSICE Electrical Model

.SUBCKT HUF76113T3 2 1 3 ; REV August 1998

CA 12 8 8.7e-10
CB 15 14 8.7e-10
CIN 6 8 5.6e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 34.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.69e-9
LSOURCE 3 7 4.1e-10

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 9.2e-3
RGATE 9 20 2.5
RLDRAIN 2 5 10
RLGATE 1 9 16.9
RLSOURCE 3 7 4.1
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 12.5e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

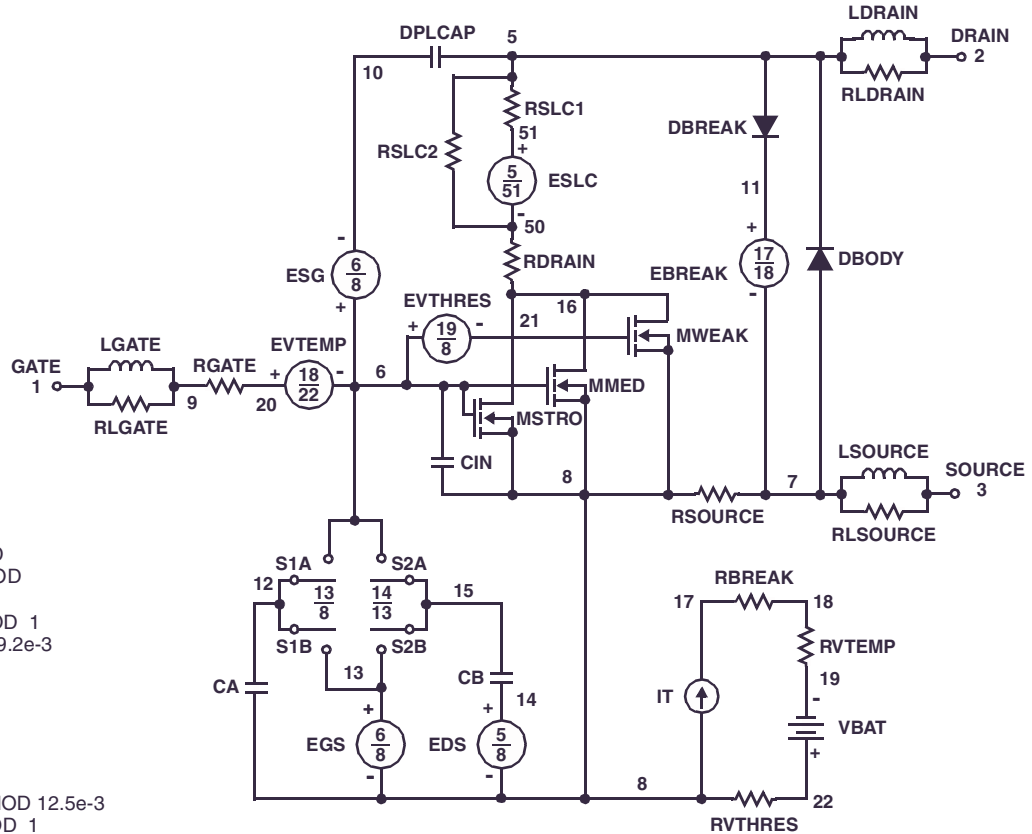
ESLC 51 50 VALUE=({(V(5,51)/ABS(V(5,51)))})*(PWR(V(5,51)/(1e-6*180),2.5)))

.MODEL DBODYMOD D (IS = 9.35e-13 RS = 1.39e-2 TRS1 = 1.12e-6 TRS2 = 1.05e-6 CJO = 9.85e-10 TT = 2.82e-8 M = 0.42)
.MODEL DBREAKMOD D (RS = 1.5e-1 TRS1 = 3.51e-3 TRS2 = -5e-5)
.MODEL DPLCAPMOD D (CJO = 4.4e-10 IS = 1e-30 N = 10 M = 0.6)
.MODEL MMEDMOD NMOS (VTO = 1.95 KP = 3.55 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.5)
.MODEL MSTROMOD NMOS (VTO = 2.23 KP = 29 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.68 KP = 0.095 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 25 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.7e-4 TC2 = -5e-7)
.MODEL RDRAINMOD RES (TC1 = 5.8e-3 TC2 = 1.12e-5)
.MODEL RSLCMOD RES (TC1 = -9.92e-3 TC2 = -2.06e-5)
.MODEL RSOURCEMOD RES (TC1 = 3e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -1.2e-3 TC2 = -5.42e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.9e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.0 VOFF = -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = -7.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.8 VOFF = 0.6)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.6 VOFF = -0.8)

.ENDS

NOTE: For further discussion of the PSICE model, consult **A New PSICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV August 1998

HUF76113T3ST

Copper Area = 0.077 in²

CTHERM1 th 8 1.9e-5

CTHERM2 8 7 9.5e-4

CTHERM3 7 6 1.9e-3

CTHERM4 6 5 3.5e-3

CTHERM5 5 4 2.0e-2

CTHERM6 4 3 6.5e-2

CTHERM7 3 2 2.4e-1

CTHERM8 2 tl 9.0e-1

RTHERM1 th 8 3.5e-3

RTHERM2 8 7 3.1e-2

RTHERM3 7 6 2.0e-1

RTHERM4 6 5 8.0e-1

RTHERM5 5 4 2.1

RTHERM6 4 3 11

RTHERM7 3 2 32

RTHERM8 2 tl 66

SABER Thermal Model

Copper Area = 0.077 in²

template thermal_model th tl

thermal_c th, tl

```
{
  ctherm.ctherm1 th 8 = 1.9e-5
  ctherm.ctherm2 8 7 = 9.5e-4
  ctherm.ctherm3 7 6 = 1.9e-3
  ctherm.ctherm4 6 5 = 3.5e-3
  ctherm.ctherm5 5 4 = 2.0e-2
  ctherm.ctherm6 4 3 = 6.5e-2
  ctherm.ctherm7 3 2 = 2.4e-1
  ctherm.ctherm8 2 tl = 9.0e-1

```

```
rtherm.rtherm1 th 8 = 3.5e-3
rtherm.rtherm2 8 7 = 3.1e-2
rtherm.rtherm3 7 6 = 2.0e-1
rtherm.rtherm4 6 5 = 8.0e-1
rtherm.rtherm5 5 4 = 2.1
rtherm.rtherm6 4 3 = 11
rtherm.rtherm7 3 2 = 32
rtherm.rtherm8 2 tl = 66
}
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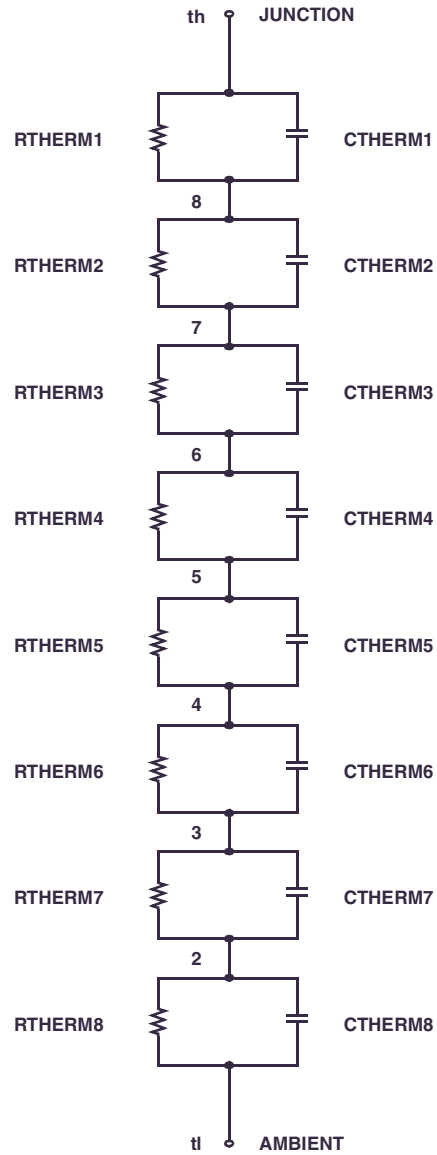


TABLE 1. THERMAL MODELS

COMPONENT	0.077 in ²	0.308 in ²	0.535 in ²	0.76 in ²	0.996 in ²
CTHERM6	6.5e-2	6.7e-2	6.7e-2	6.7e-2	6.7e-2
CTHERM7	2.4e-1	3.5e-1	3.5e-1	3.5e-1	3.5e-1
CTHERM8	9.0e-1	1.7	1.9	2	2.4
RTHERM6	11	9	9	9	9
RTHERM7	32	18	16	15.5	14.5
RTHERM8	66	45.5	40	36	31.5

TRADEMARKS

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ACEx™	FACT™	ImpliedDisconnect™	PACMAN™	SPM™
ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E ² CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I ² C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™	OCXPro™	OPTOLOGIC®	RapidConnect™	UltraFET®
The Power Franchise™	OPTOPLANAR™	SMART START™	SILENT SWITCHER®	VCX™
Programmable Active Droop™				

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.