

56A, 100V, 0.025 Ohm, N-Channel UltraFET Power MOSFETs



These N-Channel power MOSFETs are manufactured using the innovative UltraFET™ process.

This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75639.

Ordering Information

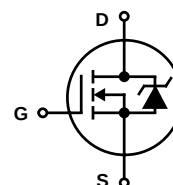
PART NUMBER	PACKAGE	BRAND
HUF75639G3	TO-247	75639G
HUF75639P3	TO-220AB	75639P
HUF75639S3S	TO-263AB	75639S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75639S3ST.

Features

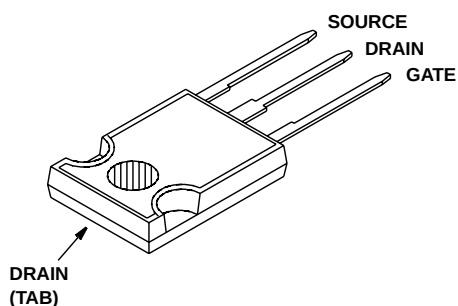
- 56A, 100V
- Simulation Models
 - Temperature Compensated PSPICE™ and SABER® Electrical Models
 - Spice and Saber Thermal Impedance Models
 - www.Intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
 - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

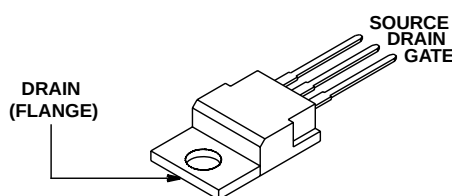


Packaging

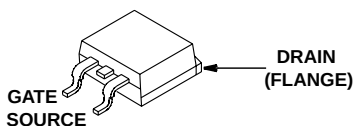
JEDEC STYLE TO-247



JEDEC TO-220AB



JEDEC TO-263AB



HUF75639G3, HUF75639P3, HUF75639S3S

Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	100	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	V_{DGR}	100	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current			
Continuous (Figure 2)	I_D	56	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	E_{AS}	Figures 6, 14, 15	
Power Dissipation	P_D	200	W
Derate Above 25°C		1.35	$\text{W}/^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^{\circ}\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	$^{\circ}\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260	$^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^{\circ}\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	100	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 95V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 90V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 56A, V _{GS} = 10V (Figure 9)	-	0.021	0.025	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	(Figure 3)	-	-	0.74	⁰ C/W	
Thermal Resistance Junction to Ambient	R _{θJA}	TO-247	-	-	30	⁰ C/W	
		TO-220, TO-263	-	-	62	⁰ C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 50V, I _D ≅ 56A, R _L = 0.89Ω, V _{GS} = 10V, R _{GS} = 5.1Ω	-	-	110	ns	
Turn-On Delay Time	t _{d(ON)}		-	15	-	ns	
Rise Time	t _r		-	60	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	20	-	ns	
Fall Time	t _f		-	25	-	ns	
Turn-Off Time	t _{OFF}		-	-	70	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 50V, I _D ≅ 56A, R _L = 0.89Ω I _{g(REF)} = 1.0mA (Figure 13)	-	110	130	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	57	75	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	3.7	4.5	nC
Gate to Source Gate Charge	Q _{gs}			-	9.8	-	nC
Reverse Transfer Capacitance	Q _{gd}			-	24	-	nC

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12)	-	2000	-	pF
Output Capacitance	C_{OSS}		-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	65	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 56\text{A}$	-	-	1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 56\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 56\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	320	nC

Typical Performance Curves

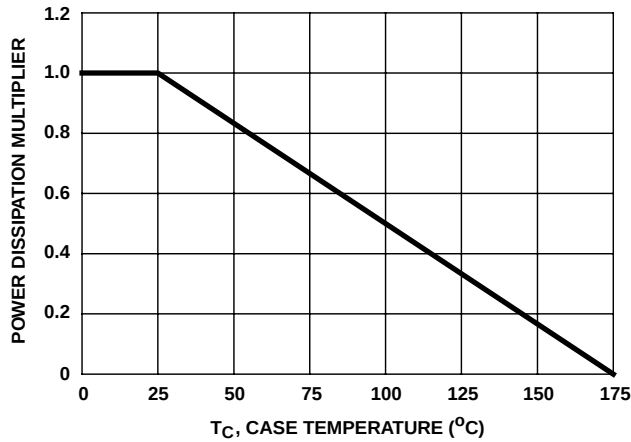


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

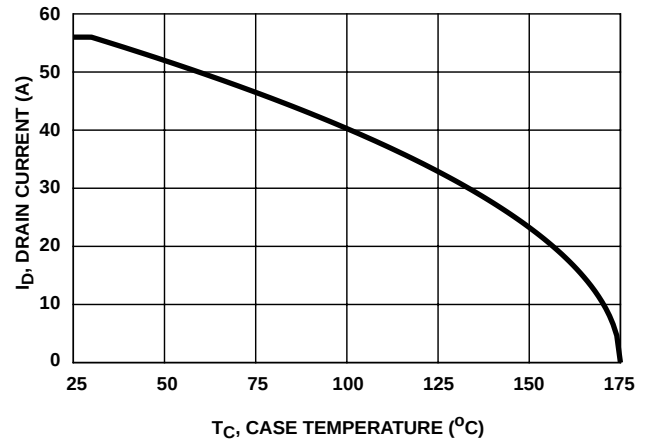


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

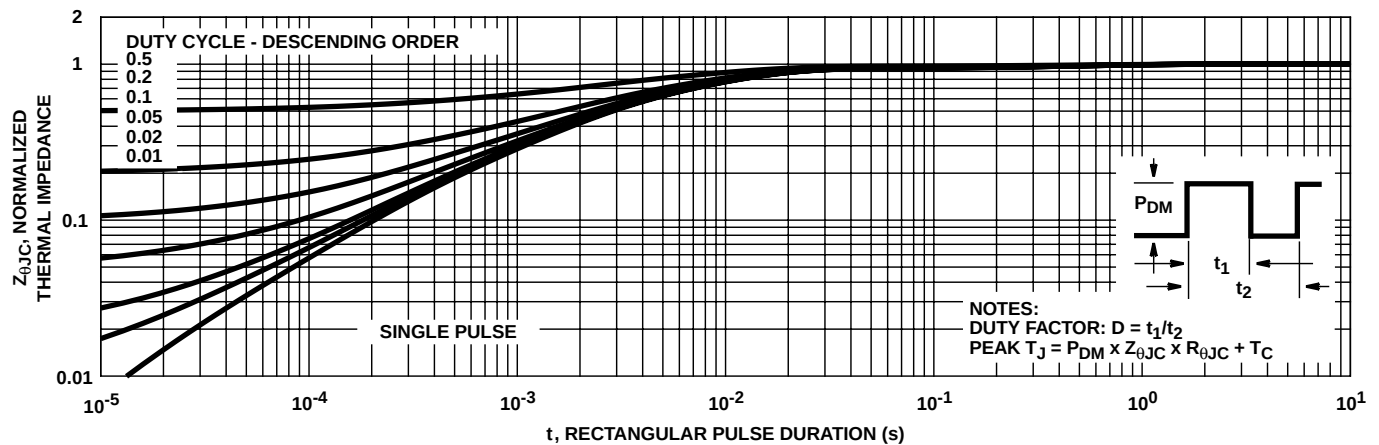
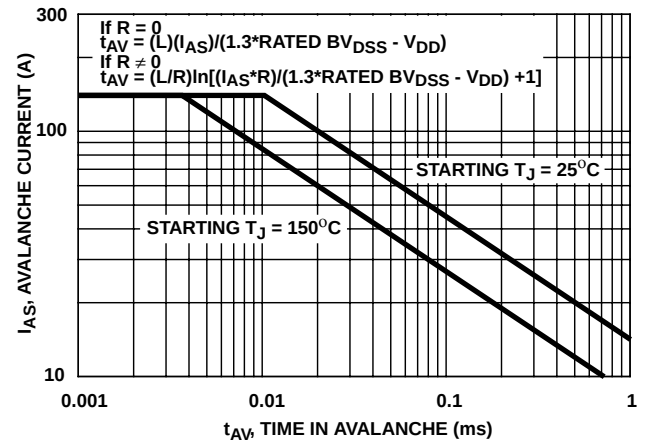
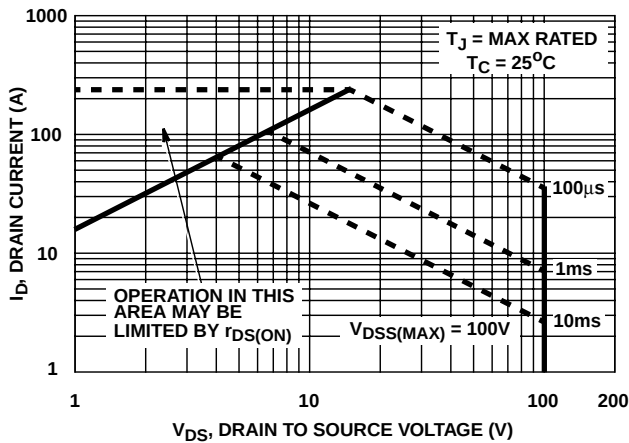
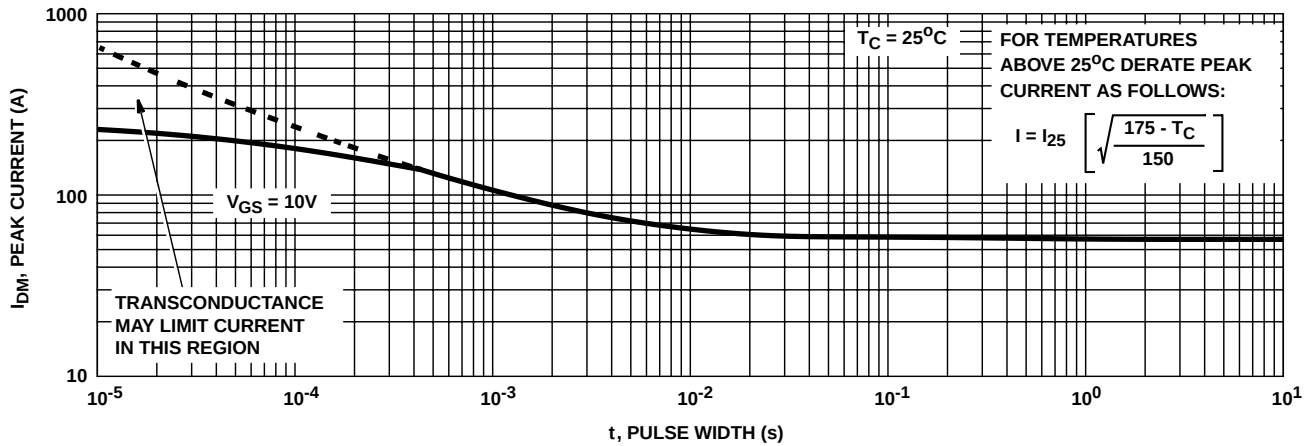
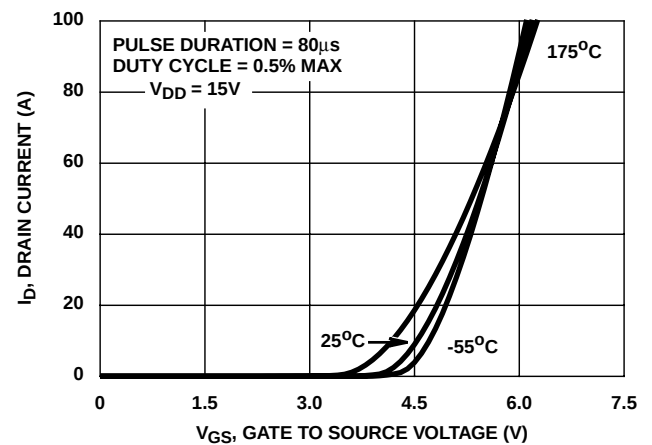
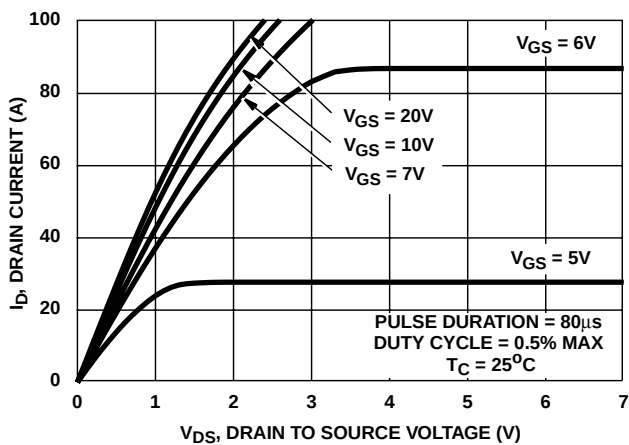


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.



Typical Performance Curves (Continued)

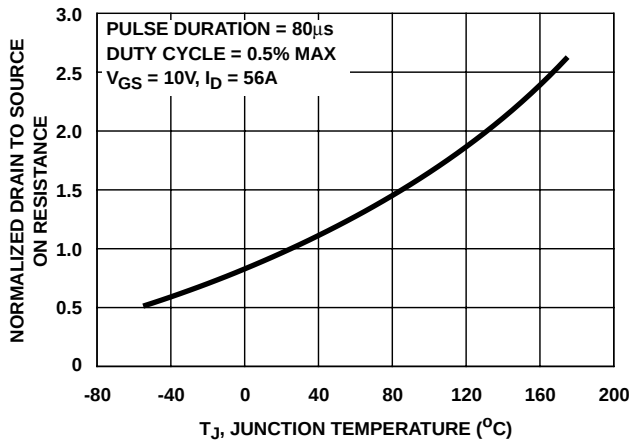


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

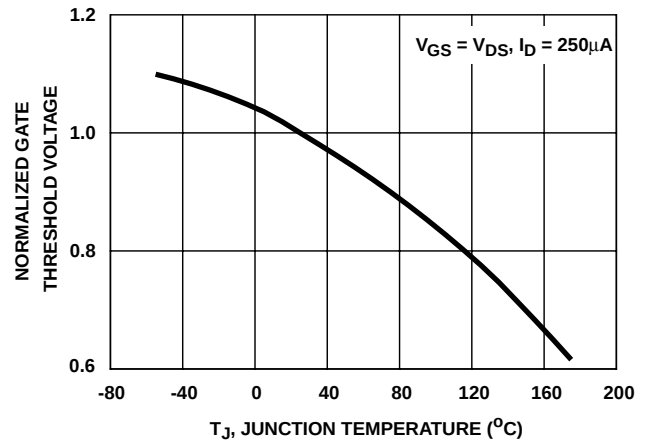


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

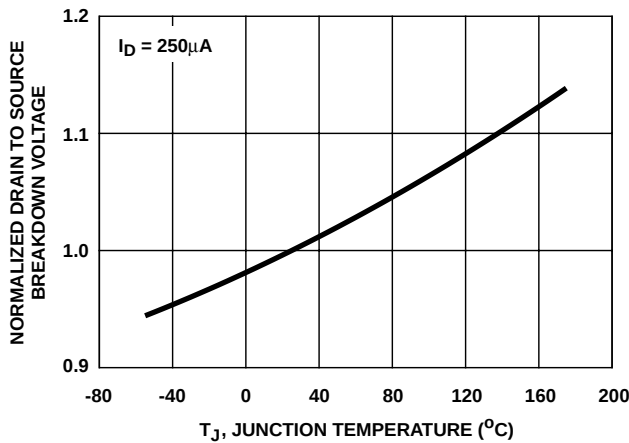


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

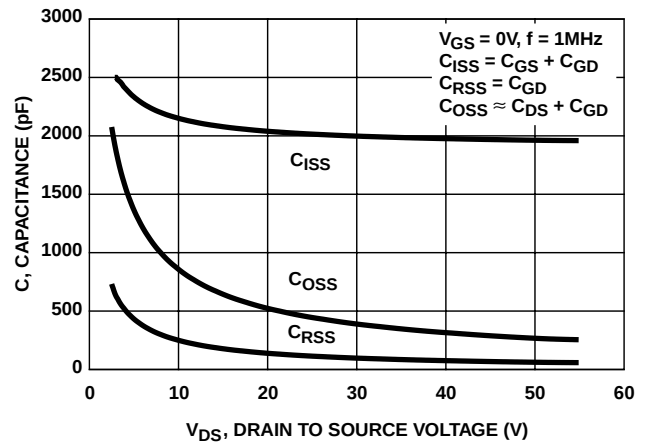
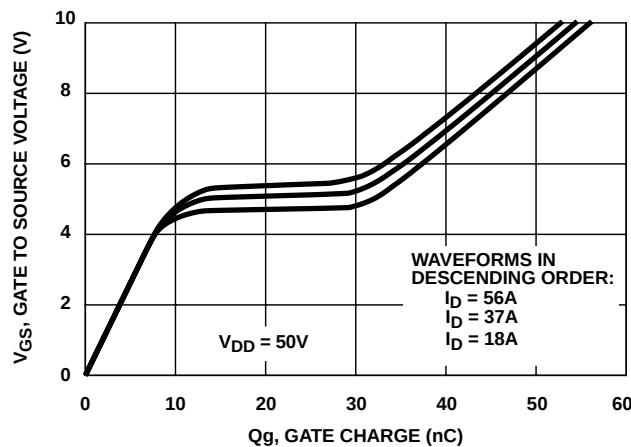


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

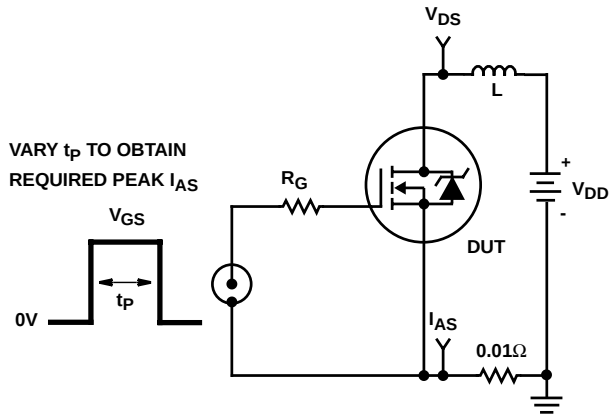


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

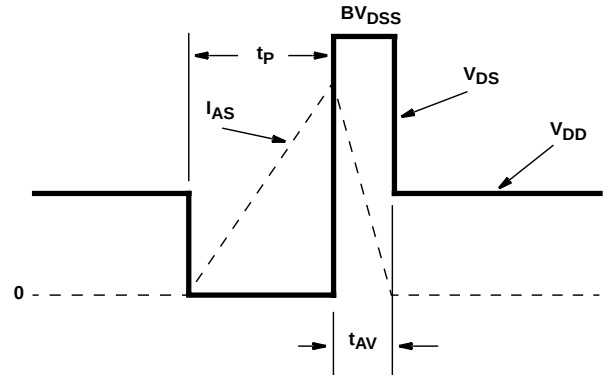


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

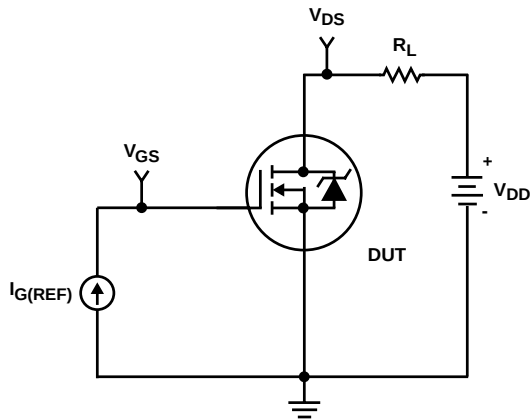


FIGURE 16. GATE CHARGE TEST CIRCUIT

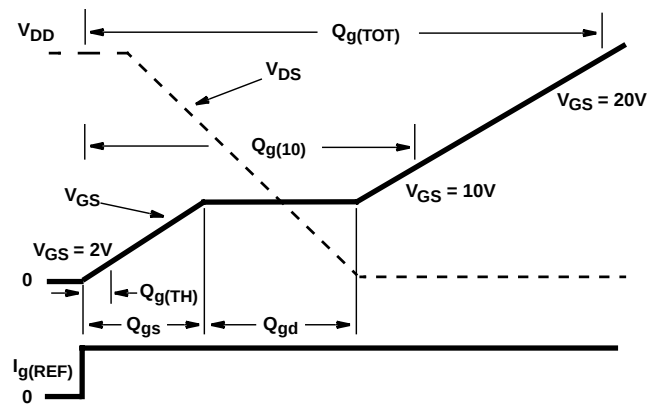


FIGURE 17. GATE CHARGE WAVEFORM

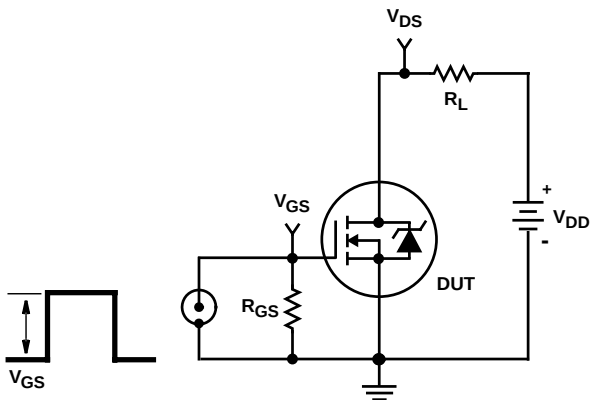


FIGURE 18. SWITCHING TIME TEST CIRCUIT

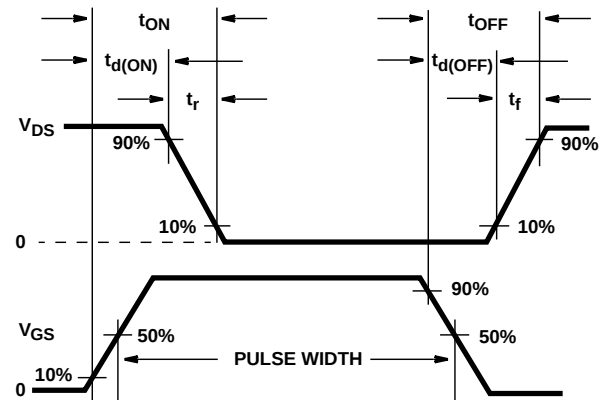


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

SABER Electrical Model

nom temp=25 deg c 100v Ultrafet

REV Oct. 98

template huf75639 n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
```

```
d..model dbodymod = (is=1.4e-12, xti=4.7, cjo=33e-10, tt=6.1e-8, m=0.7)
d..model dbreakmod = ()
d..model dplcapmod = (cjo=22e-10, is=1e-30, n=10, m=0.95, vj=1.0)
m..model mmedmod = (type=_n, vto=3.5, kp=4.8, is=1e-30, tox=1)
m..model mstrongmod = (type=_n, vto=3.97, kp=56.5, is=1e-30, tox=1)
m..model mweakmod = (type=_n, vto=3.11, kp=0.085, is=1e-30, tox=1)
sw_vcsp..model s1amod = (ron=1e-5, roff=0.1, von=-6.0, voff=-3.5)
sw_vcsp..model s1bmod = (ron=1e-5, roff=0.1, von=-3.5, voff=-6.0)
sw_vcsp..model s2amod = (ron=1e-5, roff=0.1, von=-2.5, voff=4.95)
sw_vcsp..model s2bmod = (ron=1e-5, roff=0.1, von=4.95, voff=-2.5)
```

```
c.ca n12 n8 = 28.5e-10
c.cb n15 n14 = 26.5e-10
c.cin n6 n8 = 19e-10
```

```
d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod
```

```
i.it n8 n17 = 1
```

```
l.ldrain n2 n5 = 2.0e-9
l.lgate n1 n9 = 1e-9
l.lsource n3 n7 = 4.69e-10
```

```
m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u
```

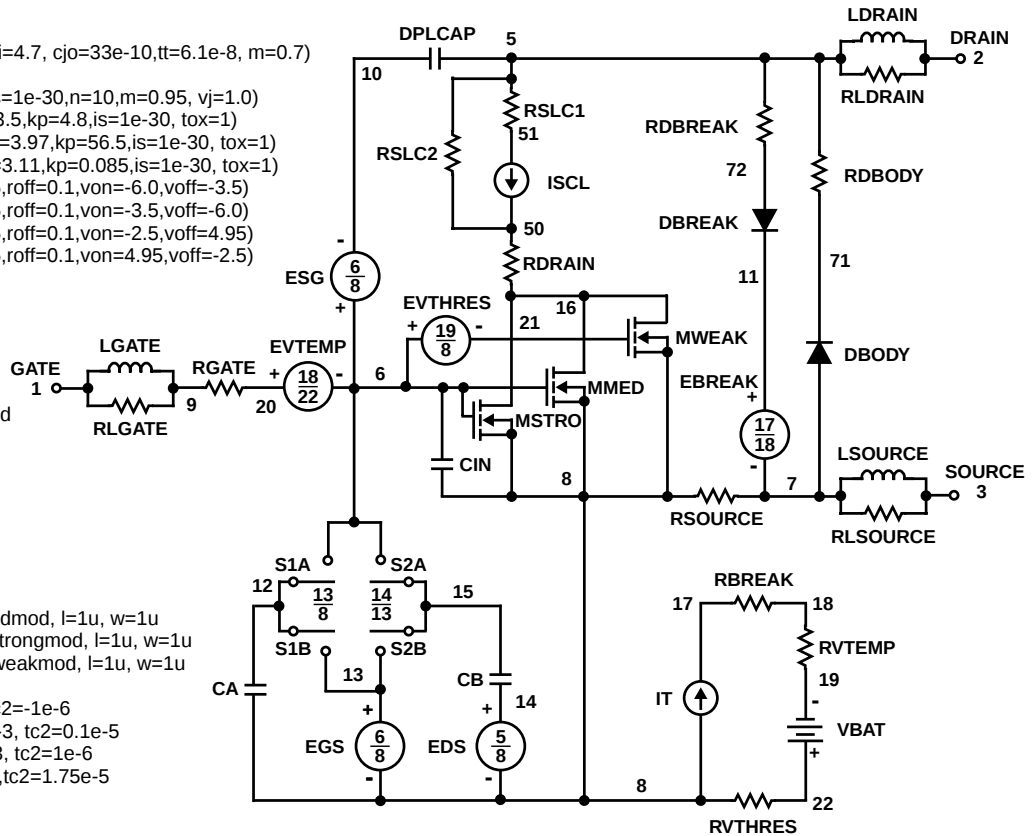
```
res.rbreak n17 n18 = 1, tc1=0.8e-3, tc2=-1e-6
res.rbody n71 n5 = 3.3e-3, tc1=2.0e-3, tc2=0.1e-5
res.rdbreak n72 n5 = 3.5e-1, tc1=1e-3, tc2=1e-6
res.rdrain n50 n16 = 13e-3, tc1=1e-2, tc2=1.75e-5
res.rgate n9 n20 = 0.7
res.rldrain n2 n5 = 20
res.rlgate n1 n9 = 10
res.rlsource n3 n7 = 4.69
res.rslc1 n5 n51 = 1e-6, tc1=2.8e-3, tc2=14e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7 = 4.5e-3, tc1=0, tc2=0
res.rvtemp n18 n19 = 1, tc1=-2.75e-3, tc2=0.05e-9
res.rvthres n22 n8 = 1, tc1=-2e-3, tc2=-1.75e-5
```

```
spe.ebreak n11 n7 n17 n18 = 110
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1
```

```
sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod
```

```
v.vbat n22 n19 = dc=1
```

```
equations {
i (n51->n50) += iscl
iscl: v(n51,n50) = (((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/115))** 4))
}
}
```



Spice Thermal Model

REV APRIL 1998

HUF75639

CTHERM1 TH 6 5.0e-3
CTHERM2 6 5 1.9e-2
CTHERM3 5 4 7.95e-3
CTHERM4 4 3 9.0e-3
CTHERM5 3 2 2.95e-2
CTHERM6 2 TL 12.55

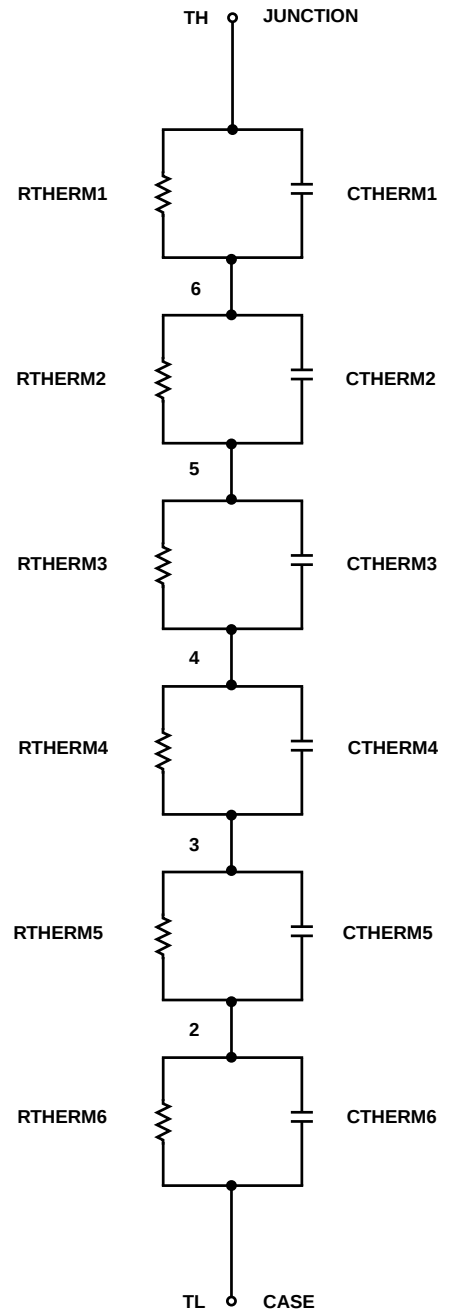
R THERM1 TH 6 5.04e-3
R THERM2 6 5 1.25e-2
R THERM3 5 4 3.54e-2
R THERM4 4 3 1.98e-1
R THERM5 3 2 2.99e-1
R THERM6 2 TL 3.97e-2

Saber Thermal Model

Saber thermal model HUF75639

```
template thermal_model th tl
thermal_c th, tl
{
  ctherm.ctherm1 th 6 = 5.0e-3
  ctherm.ctherm2 6 5 = 1.9e-2
  ctherm.ctherm3 5 4 = 7.95e-3
  ctherm.ctherm4 4 3 = 9.0e-3
  ctherm.ctherm5 3 2 = 2.95e-2
  ctherm.ctherm6 2 tl = 12.55
```

```
rtherm.rtherm1 th 6 = 5.04e-3
rtherm.rtherm2 6 5 = 1.25e-2
rtherm.rtherm3 5 4 = 3.54e-2
rtherm.rtherm4 4 3 = 1.98e-1
rtherm.rtherm5 3 2 = 2.99e-1
rtherm.rtherm6 2 tl = 3.97e-2
}
```



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