
HN58S65A Series

64 k EEPROM (8-kword × 8-bit)
Ready/ $\overline{\text{Busy}}$ function

HITACHI

ADE-203-691A (Z)
Preliminary
Rev. 0.3
Nov. 1997

Description

The Hitachi HN58S65A series is electrically erasable and programmable ROM organized as 8192-word × 8-bit. It has realized high speed, low power consumption and high reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

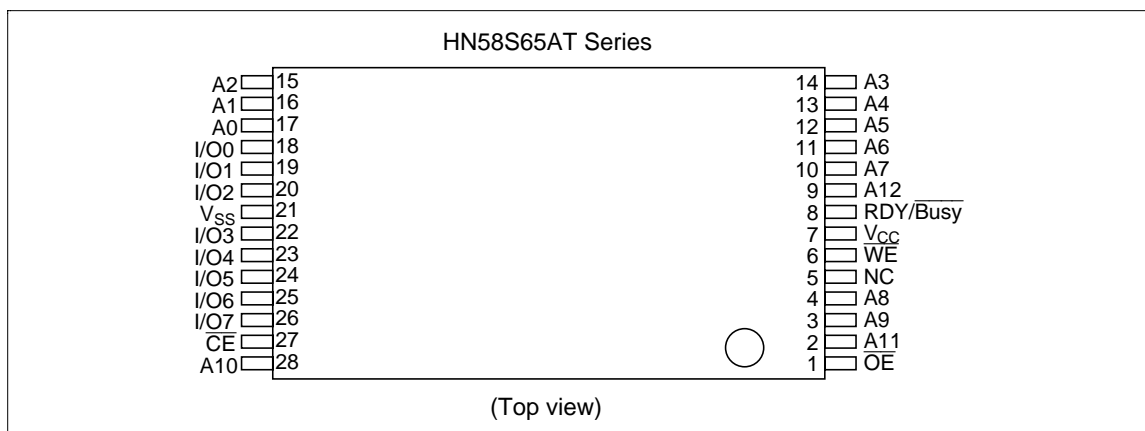
- Single supply: 2.2 to 3.6 V
- Access time: 150 ns (max)
- Power dissipation
 - Active: 10 mW/MHz (typ)
 - Standby: 36 μ W (max)
- On-chip latches: address, data, $\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$
- Automatic byte write: 15 ms (max)
- Automatic page write (64 bytes): 15 ms (max)
- Ready/ $\overline{\text{Busy}}$
- $\overline{\text{Data}}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Industrial versions (Temperature range: -40 to $+85^\circ\text{C}$) are also available.

HN58S65A Series

Ordering Information

| Type No. | Access time | Package |
|--------------|-------------|-------------------------------|
| HN58S65AT-15 | 150 ns | 28-pin plastic TSOP(TFP-28DB) |

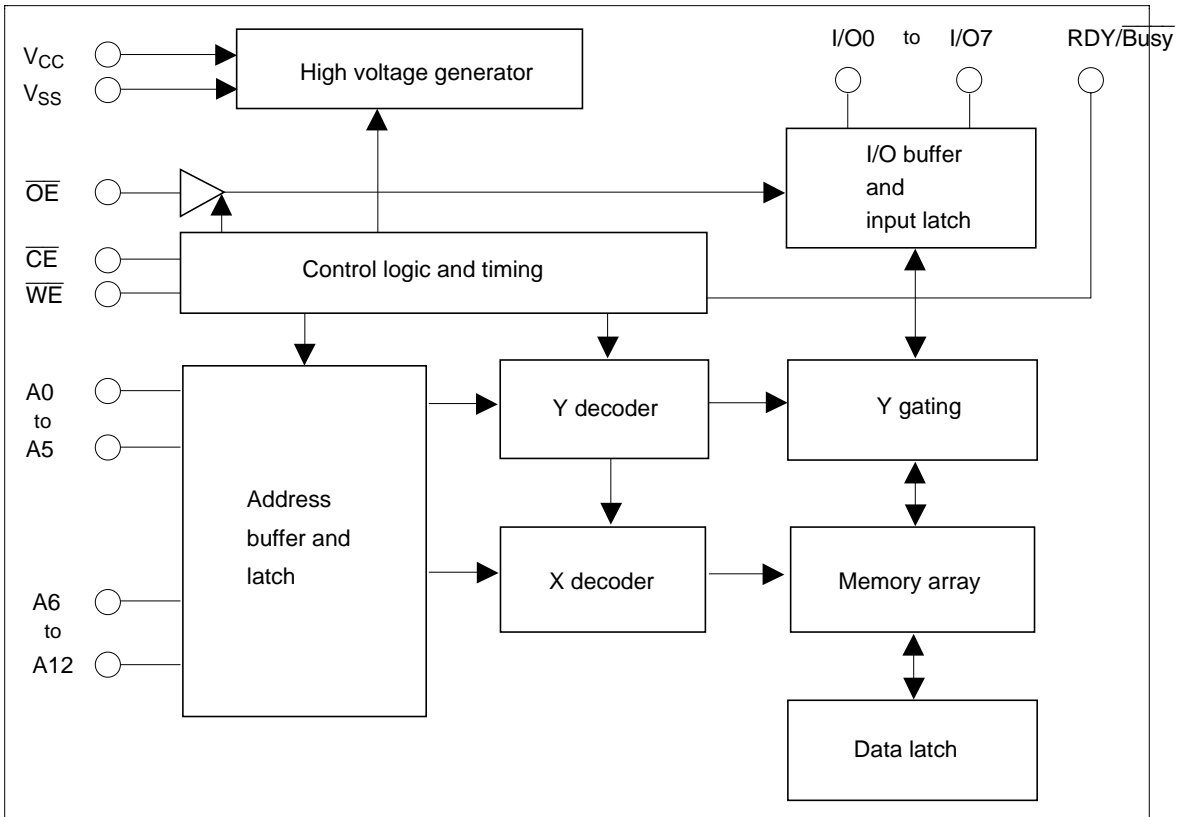
Pin Arrangement



Pin Description

| Pin name | Function |
|-----------------------|-------------------|
| A0 to A12 | Address input |
| I/O0 to I/O7 | Data input/output |
| \overline{OE} | Output enable |
| \overline{CE} | Chip enable |
| \overline{WE} | Write enable |
| V_{cc} | Power supply |
| V_{ss} | Ground |
| $\overline{RDY/Busy}$ | Ready busy |
| NC | No connection |

Block Diagram



Operation Table

| Operation | \overline{CE} | \overline{OE} | \overline{WE} | $\overline{RDY/Busy}$ | I/O |
|---------------|-----------------|-----------------|-----------------|-----------------------|-------------|
| Read | V_{IL} | V_{IL} | V_{IH} | High-Z | Dout |
| Standby | V_{IH} | \times^{*1} | \times | High-Z | High-Z |
| Write | V_{IL} | V_{IH} | V_{IL} | High-Z to V_{OL} | Din |
| Deselect | V_{IL} | V_{IH} | V_{IH} | High-Z | High-Z |
| Write Inhibit | \times | \times | V_{IH} | — | — |
| | \times | V_{IL} | \times | — | — |
| Data Polling | V_{IL} | V_{IL} | V_{IH} | V_{OL} | Dout (I/O7) |

Notes: 1. \times : Don't care

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------|--|------|
| Power supply voltage relative to V_{SS} | V_{CC} | -0.6 to +7.0 | V |
| Input voltage relative to V_{SS} | V_{in} | -0.5* ¹ to +7.0* ³ | V |
| Operating temperature range * ² | T_{opr} | 0 to +70 | °C |
| Storage temperature range | T_{stg} | -55 to +125 | °C |

- Notes: 1. V_{in} min : -3.0 V for pulse width \leq 50 ns.
 2. Including electrical characteristics and data retention.
 3. Should not exceed $V_{CC} + 1.0$ V.

Recommended DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|-----------------------|-----------|---------------------|-----|-------------------------------|------|
| Supply voltage | V_{CC} | 2.2 | 3.0 | 3.6 | V |
| | V_{SS} | 0 | 0 | 0 | V |
| Input voltage | V_{IL} | -0.3* ¹ | — | 0.4 | V |
| | V_{IH} | $V_{CC} \times 0.7$ | — | $V_{CC} + 0.3$ * ² | V |
| Operating temperature | T_{opr} | 0 | — | 70 | °C |

- Notes: 1. V_{IL} min: -1.0 V for pulse width \leq 50 ns.
 2. V_{IH} max: $V_{CC} + 1.0$ V for pulse width \leq 50 ns.

DC Characteristics ($T_a = 0$ to +70°C, $V_{CC} = 2.2$ to 3.6 V)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|----------------------------|-----------|---------------------|--------|-----|---------|---|
| Input leakage current | I_{LI} | — | — | 2 | μ A | $V_{CC} = 5.5$ V, $V_{in} = 5.5$ V |
| Output leakage current | I_{LO} | — | — | 2 | μ A | $V_{CC} = 5.5$ V, $V_{out} = 5.5/0.4$ V |
| Standby V_{CC} current | I_{CC1} | — | 1 to 2 | 3.5 | μ A | $\overline{CE} = V_{CC}$ |
| | I_{CC2} | — | — | 500 | μ A | $\overline{CE} = V_{IH}$ |
| Operating V_{CC} current | I_{CC3} | — | — | 6 | mA | $I_{out} = 0$ mA, Duty = 100%, Cycle = 1 μ s at $V_{CC} = 3.6$ V |
| | | — | — | 12 | mA | $I_{out} = 0$ mA, Duty = 100%, Cycle = 150 ns at $V_{CC} = 3.6$ V |
| Output low voltage | V_{OL} | — | — | 0.4 | V | $I_{OL} = 1.0$ mA |
| Output high voltage | V_{OH} | $V_{CC} \times 0.8$ | — | — | V | $I_{OH} = -100$ μ A |

Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions |
|--------------------|----------------|-----|-----|-----|------|------------------------|
| Input capacitance | C_{in}^{*1} | — | — | 6 | pF | $V_{in} = 0\text{ V}$ |
| Output capacitance | C_{out}^{*1} | — | — | 12 | pF | $V_{out} = 0\text{ V}$ |

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = 0\text{ to }+70^\circ\text{C}$, $V_{CC} = 2.2\text{ to }3.6\text{ V}$)

Test Conditions

- Input pulse levels : $0.4\text{ V to }2.4\text{ V}$ ($V_{CC} = 2.7\text{ to }3.6\text{ V}$), $0.4\text{ V to }1.9\text{ V}$ ($V_{CC} = 2.2\text{ to }2.7\text{ V}$)
- Input rise and fall time : $\leq 5\text{ ns}$
- Input timing reference levels : $0.8, 1.8\text{ V}$
- Output load : 1TTL Gate +100 pF
- Output reference levels : $1.5\text{ V}, 1.5\text{ V}$ ($V_{CC} = 2.7\text{ to }3.6\text{ V}$)
 $1.1\text{ V}, 1.1\text{ V}$ ($V_{CC} = 2.2\text{ to }2.7\text{ V}$)

Read Cycle

| Parameter | Symbol | HN58S65A | | Unit | Test conditions |
|--|-----------|----------|-----|------|--|
| | | Min | Max | | |
| Address to output delay | t_{ACC} | — | 150 | ns | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| \overline{CE} to output delay | t_{CE} | — | 150 | ns | $\overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| \overline{OE} to output delay | t_{OE} | 10 | 80 | ns | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ |
| Address to output hold | t_{OH} | 0 | — | ns | $\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$ |
| \overline{OE} (\overline{CE}) high to output float*1 | t_{DF} | 0 | 80 | ns | $\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$ |

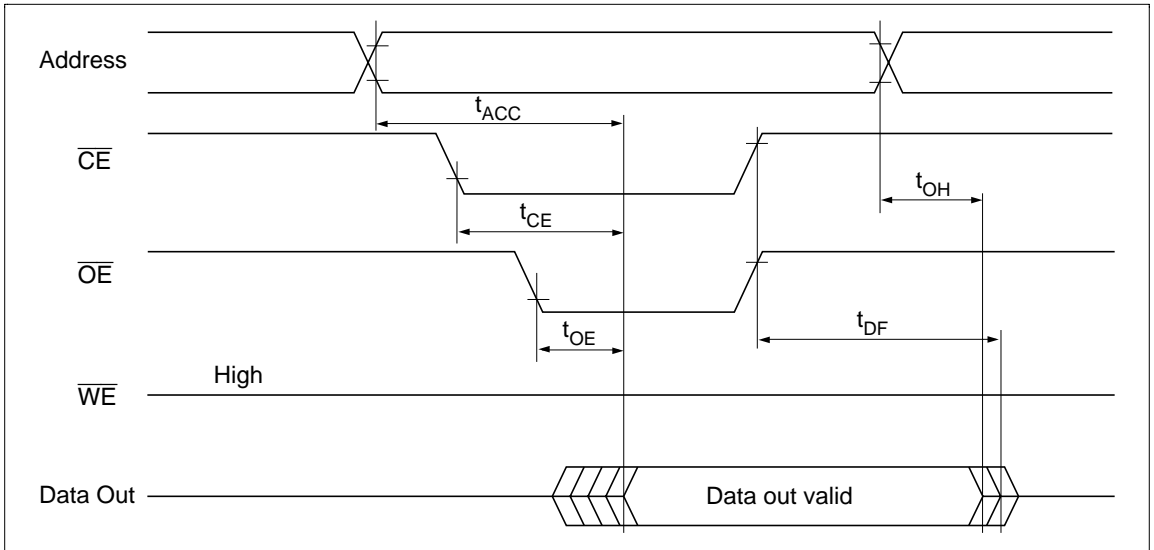
Write Cycle

| Parameter | Symbol | Min* ² | Typ | Max | Unit | Test conditions |
|---|-----------|-------------------|-----|------------------|---------|-----------------|
| Address setup time | t_{AS} | 0 | — | — | ns | |
| Address hold time | t_{AH} | 150 | — | — | ns | |
| \overline{CE} to write setup time (\overline{WE} controlled) | t_{CS} | 0 | — | — | ns | |
| \overline{CE} hold time (\overline{WE} controlled) | t_{CH} | 0 | — | — | ns | |
| \overline{WE} to write setup time (\overline{CE} controlled) | t_{WS} | 0 | — | — | ns | |
| \overline{WE} hold time (\overline{CE} controlled) | t_{WH} | 0 | — | — | ns | |
| \overline{OE} to write setup time | t_{OES} | 0 | — | — | ns | |
| \overline{OE} hold time | t_{OEH} | 0 | — | — | ns | |
| Data setup time | t_{DS} | 150 | — | — | ns | |
| Data hold time | t_{DH} | 0 | — | — | ns | |
| \overline{WE} pulse width (\overline{WE} controlled) | t_{WP} | 200 | — | — | ns | |
| \overline{CE} pulse width (\overline{CE} controlled) | t_{CW} | 200 | — | — | ns | |
| Data latch time | t_{DL} | 200 | — | — | ns | |
| Byte load cycle | t_{BLC} | 0.4 | — | 30 | μ s | |
| Byte load window | t_{BL} | 100 | — | — | μ s | |
| Write cycle time | t_{WC} | — | — | 15* ³ | ms | |
| Time to device busy | t_{DB} | 120 | — | — | ns | |
| Write start time | t_{DW} | 0* ⁴ | — | — | ns | |

- Notes:
- t_{DF} is defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.
 - Use this device in longer cycle than this value.
 - t_{WC} must be longer than this value unless polling techniques or RDY/\overline{Busy} are used. This device automatically completes the internal write operation within this value.
 - Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/\overline{Busy} are used.
 - A6 through A12 are page addresses and these addresses are latched at the first falling edge of \overline{WE} .
 - A6 through A12 are page addresses and these addresses are latched at the first falling edge of \overline{CE} .
 - See AC read characteristics.

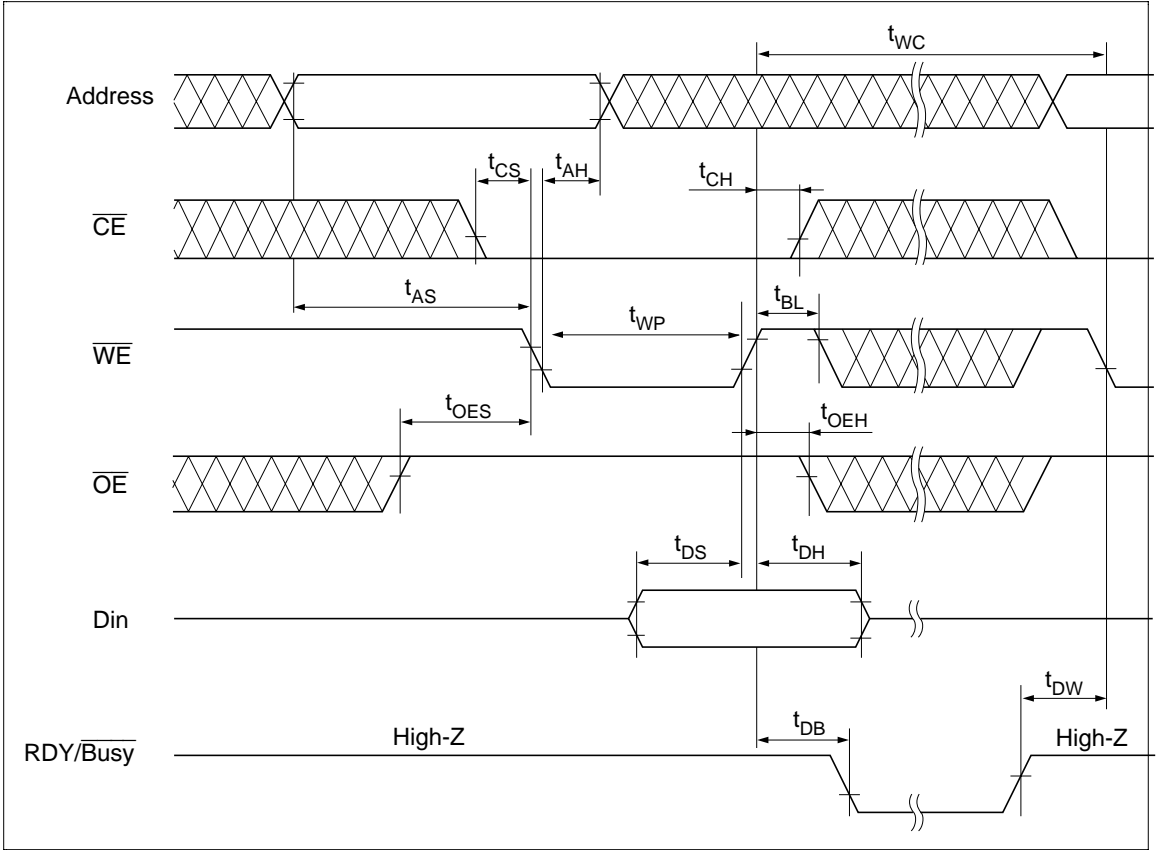
Timing Waveforms

Read Timing Waveform

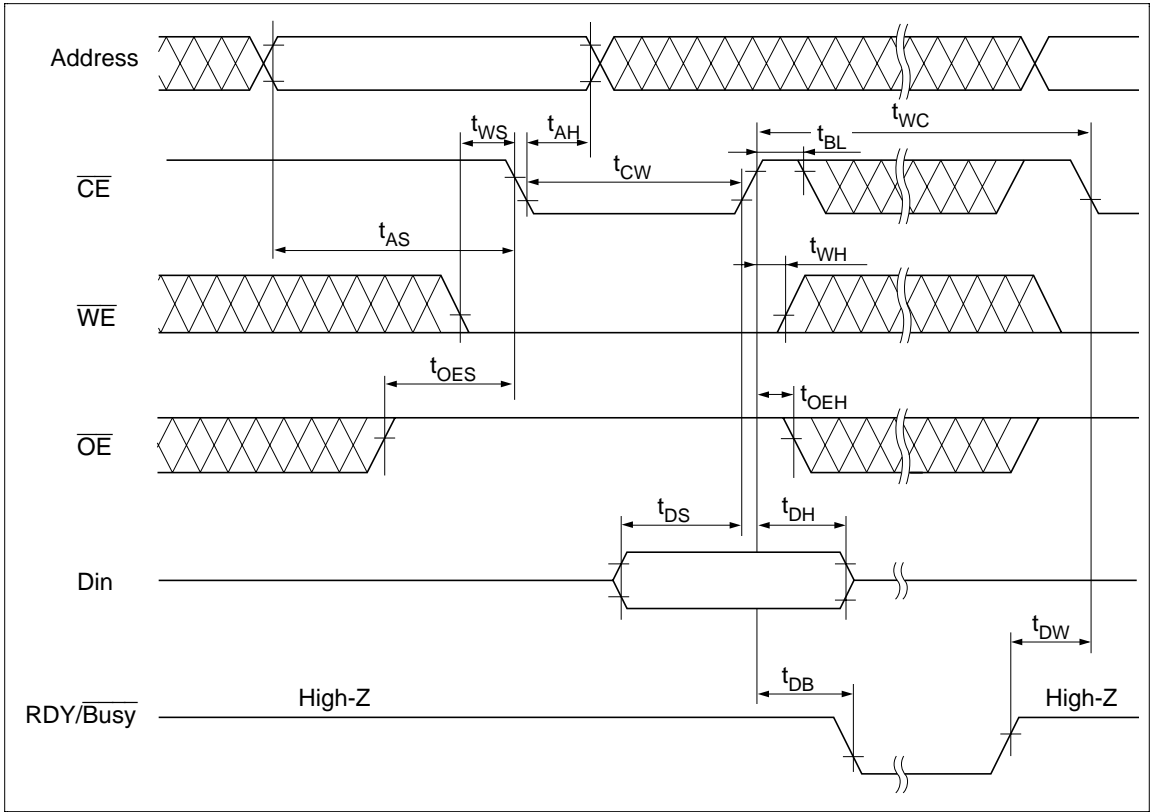


HN58S65A Series

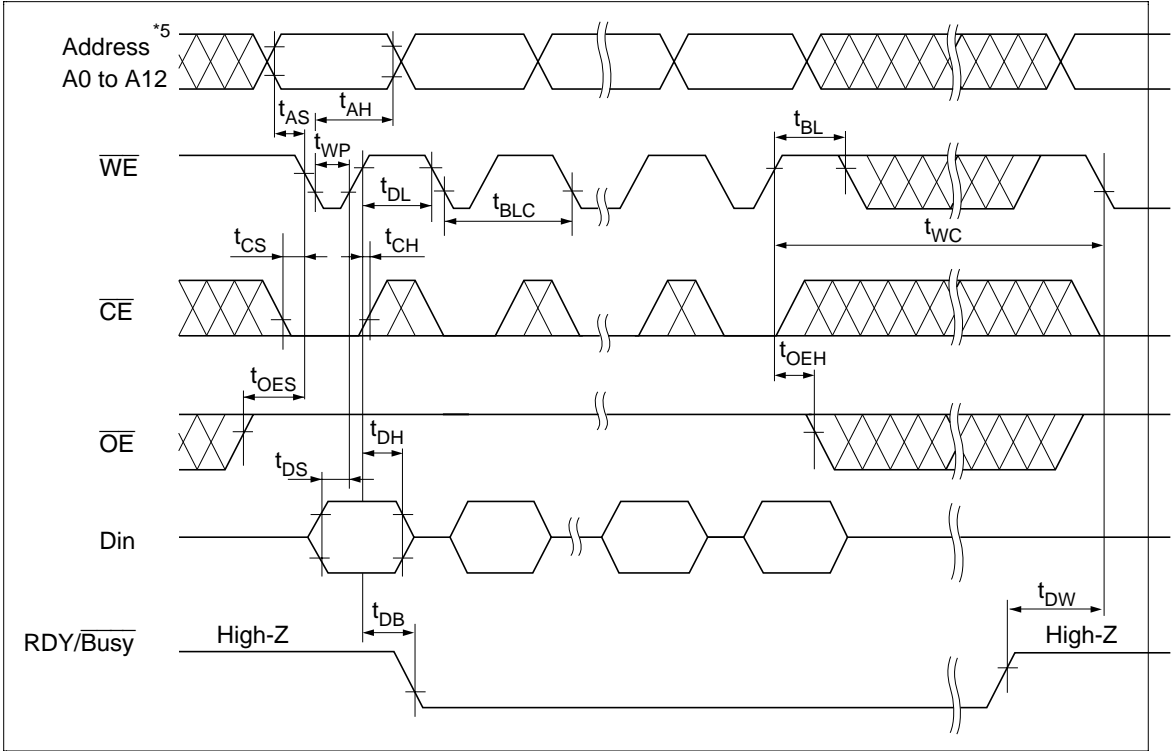
Byte Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



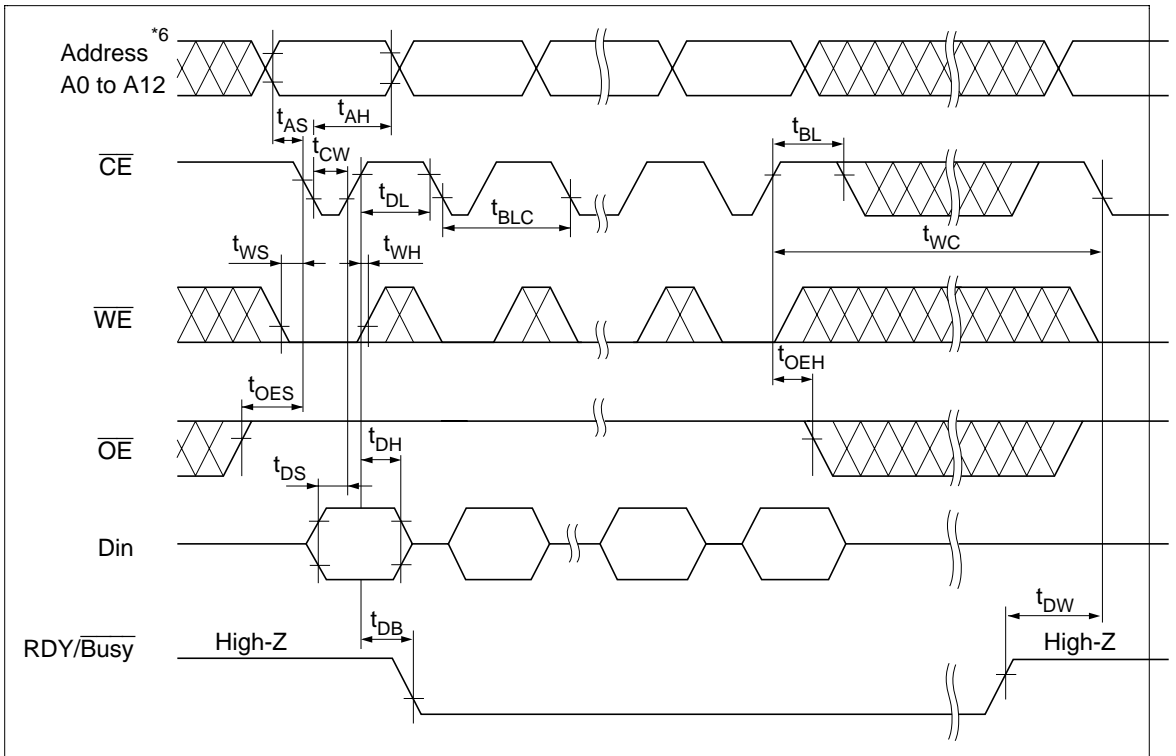
Byte Write Timing Waveform(2) (\overline{CE} Controlled)



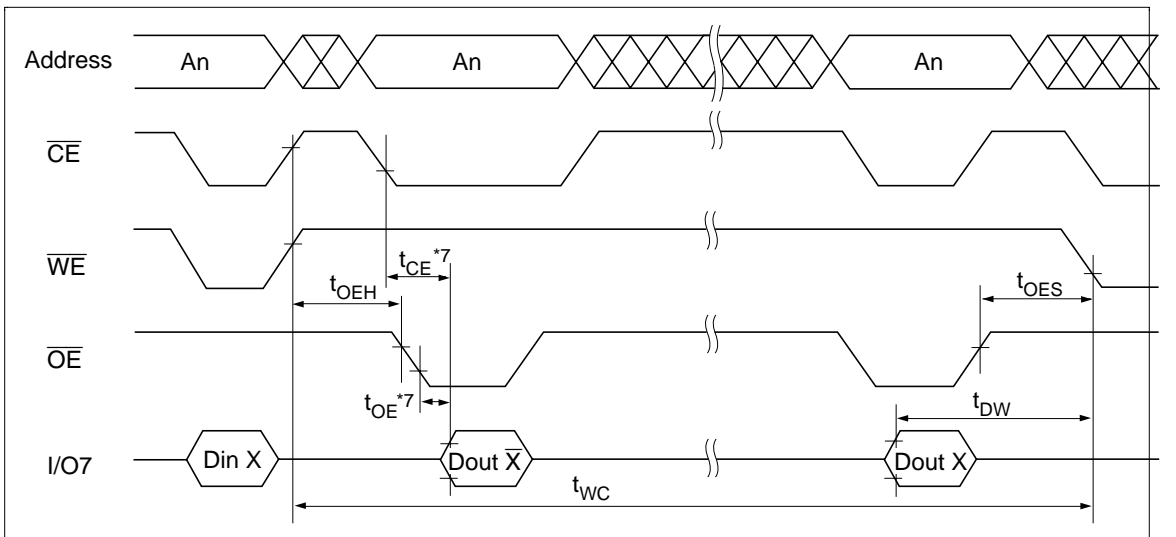
Page Write Timing Waveform(1) ($\overline{\text{WE}}$ Controlled)



Page Write Timing Waveform(2) ($\overline{\text{CE}}$ Controlled)



Data Polling Timing Waveform

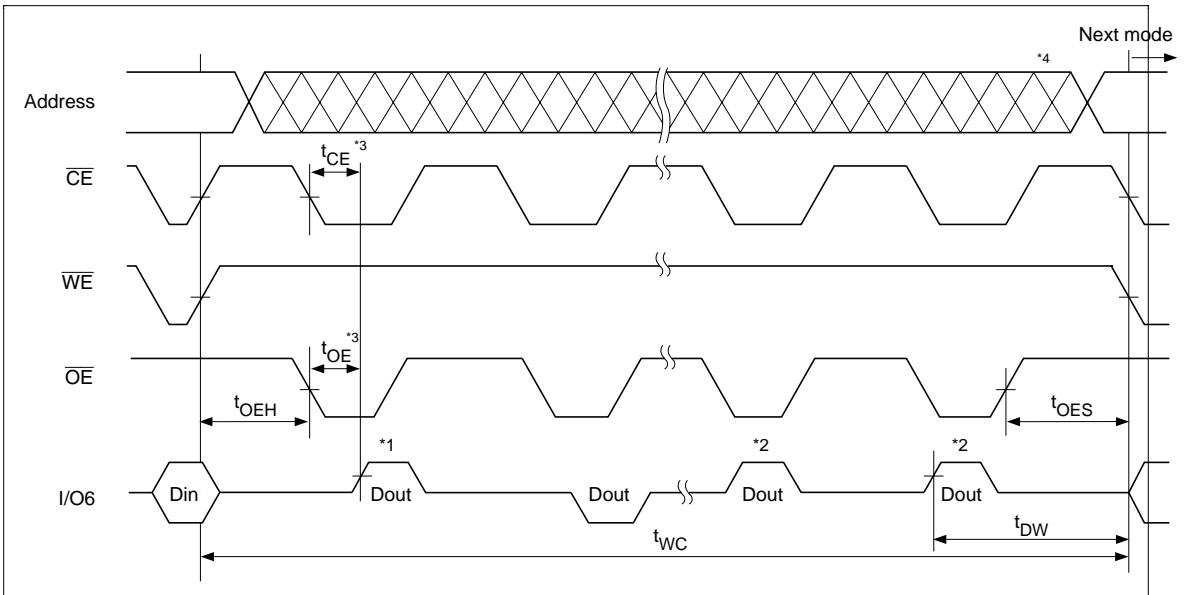


Toggle Bit

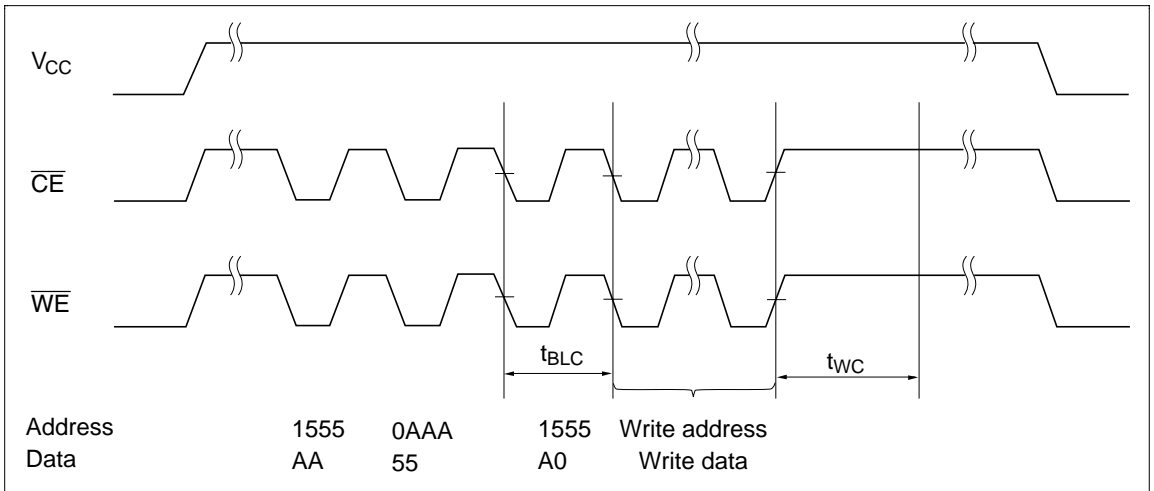
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

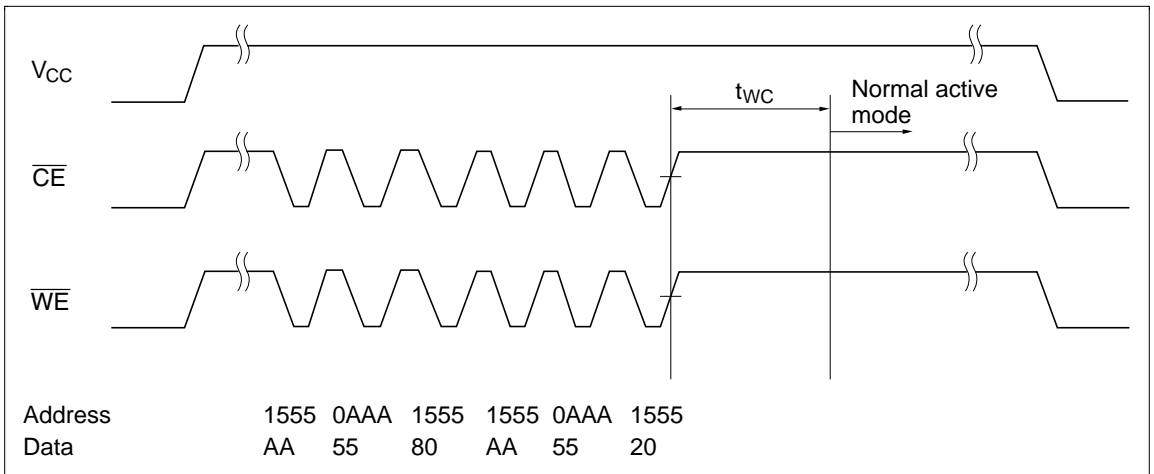
- Notes: 1. I/O6 beginning state is "1".
2. I/O6 ending state will vary.
3. See AC read characteristics.
4. Any address location can be used, but the address must be fixed.



Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 μ s from the preceding falling edge of \overline{WE} or \overline{CE} . When \overline{CE} or \overline{WE} is kept high for 100 μ s after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

\overline{Data} Polling

\overline{Data} polling indicates the status that the EEPROM is in a write cycle or not. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/ \overline{Busy} Signal

RDY/ \overline{Busy} signal also allows status of the EEPROM to be determined. The RDY/ \overline{Busy} signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/ \overline{Busy} signal changes state to high impedance.

\overline{WE} , \overline{CE} Pin Operation

During a write cycle, addresses are latched by the falling edge of \overline{WE} or \overline{CE} , and data is latched by the rising edge of \overline{WE} or \overline{CE} .

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

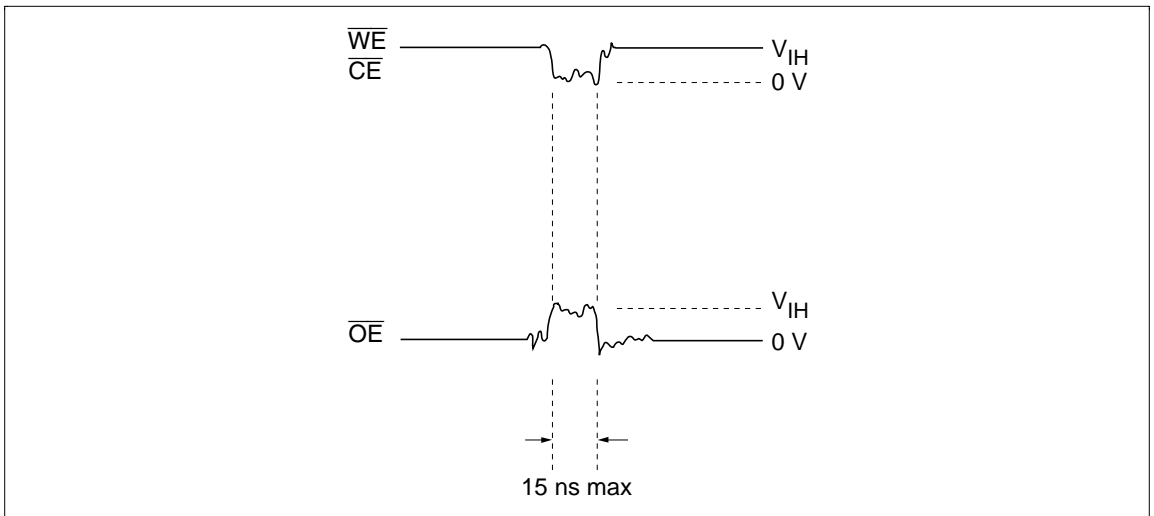
Data Protection

1. Data Protection against Noise on Control Pins (\overline{CE} , \overline{OE} , \overline{WE}) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 15 ns or less.

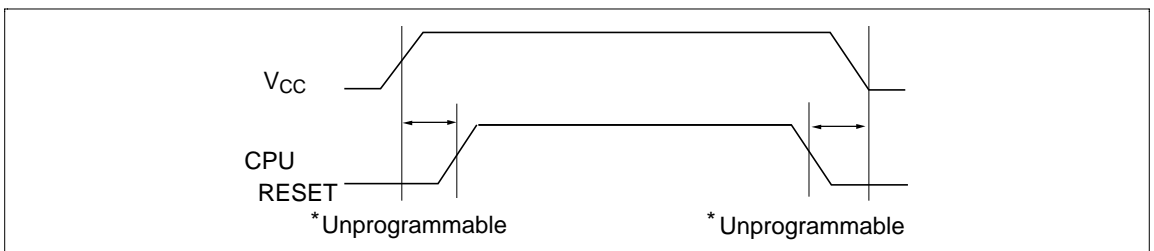
Be careful not to allow noise of a width of more than 15 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.

Note: The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.



HN58S65A Series

(1) Protection by \overline{CE} , \overline{OE} , \overline{WE}

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

| | | | |
|-----------------|----------|----------|----------|
| \overline{CE} | V_{CC} | × | × |
| \overline{OE} | × | V_{SS} | × |
| \overline{WE} | × | × | V_{CC} |

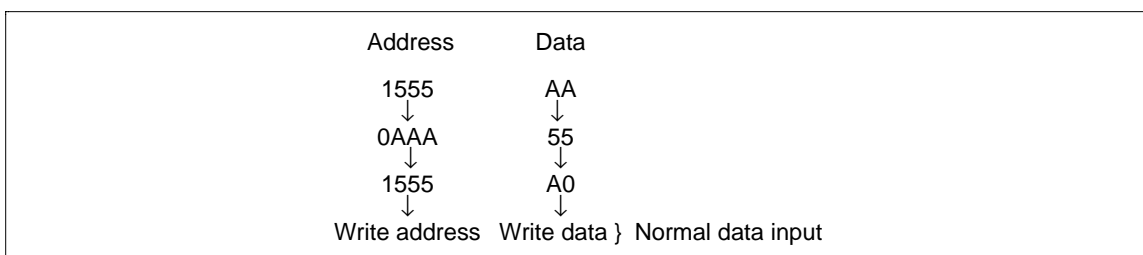
×: Don't care.

V_{CC} : Pull-up to V_{CC} level.

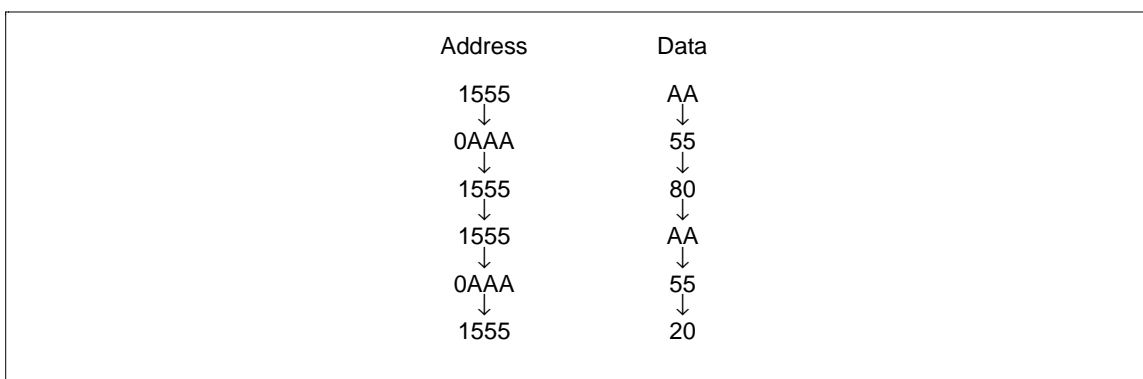
V_{SS} : Pull-down to V_{SS} level.

3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, this device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode. SDP is enabled if only the 3 byte code is input.



Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.



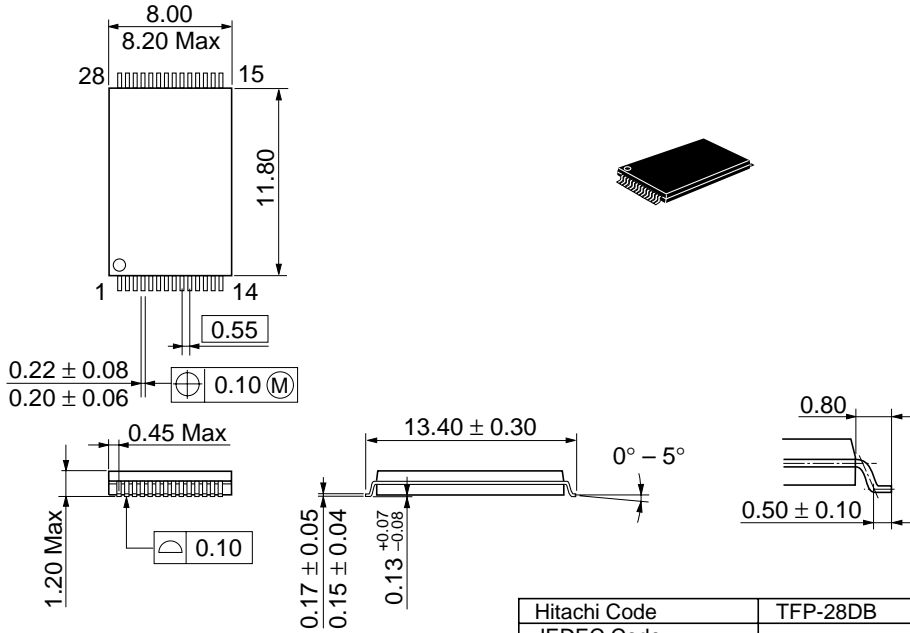
The software data protection is not enabled at the shipment.

Note: There are some differences between Hitachi's and other company's for enable/disable sequence of software data protection. If there are any questions, please contact with Hitachi sales offices.

Package Dimensions

HN58S65AT Series (TFP-28DB)

Unit: mm



Dimension including the plating thickness
Base material dimension

| | |
|--------------------------|----------|
| Hitachi Code | TFP-28DB |
| JEDEC Code | — |
| EIAJ Code | — |
| Weight (reference value) | 0.23 g |

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HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071