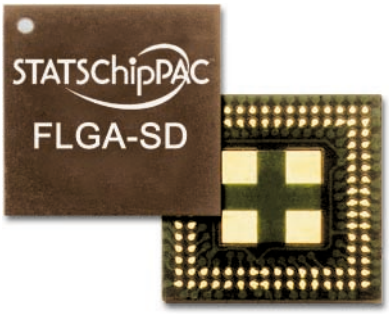
FLGA-SD

Fine Pitch Land Grid Array - Stacked Die

- Stacking of die allows for more functionality in an array molded, cost effective, space saving package solution
- Available in 1.2mm (TFLGA), 1.0mm (VFLGA), and 0.8mm (WFLGA) maximum thickness
- Thinner than FBGA
- Exposed thermal/mechanical lands available
- Laminate substrate based enabling 2 and 4 layers of routing flexibility



FEATURES

- 2 to 7 die stack with spacer capability
- Flexible body sizes range from 4mm x 4mm to 13mm x 13mm
- Package height at 1.0, 1.2, 1.4mm max
- Flexible die stacking options (“pyramid,” “same die,” etc.)
- 0.5mm minimum land pitch, flexible land pattern
- Flash/SRAM/PSRAM/Logic/Analog combinations
- JEDEC standard package outlines
- Die thinning to 75um (3mils) capability
- Low loop wire bonding; reverse and die to die
- Up to 2mm die overhang per side
- Halogen-free and Low-K wafer compatible BOM

DESCRIPTION

STATS ChipPAC’s chip stack technology offers the flexibility of stacking 2 to 7 die in a single package. Die to die bonding capability enables device and signal integration to improve electrical performance and reduce overall package I/O requirements. Wafer thinning technology, overhang wire bond technology, and the use of spacers between stacked die provide the flexibility to stack almost any desirable configuration of die in one package. This capability uses existing assembly infrastructure, which results in more functional integration with lower overall package cost. The use of the latest packaging materials allows this package to meet JEDEC Moisture Resistance Test Level 2a with Lead-free reflow condition. This is an ideal package for cell phone applications where Digital, Flash, SRAM, PSRAM and Logic are stacked into a single package.

APPLICATIONS

- Handheld devices
- Wireless RF
- Analog
- ASIC
- Memory
- Simple PLDs

FLGA-SD

Fine Pitch Land Grid Array - Stacked Die

SPECIFICATIONS

Die Thickness	75–165µm (3-6.5 mils)
Mold Cap Thickness	0.45-0.9mm
Marking	Laser
Packing Options	Tape & reel/JEDEC tray

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (–65°C to 150°C), 1000 cycles
High Temp Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C/100%RH/2atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

ELECTRICAL PERFORMANCE

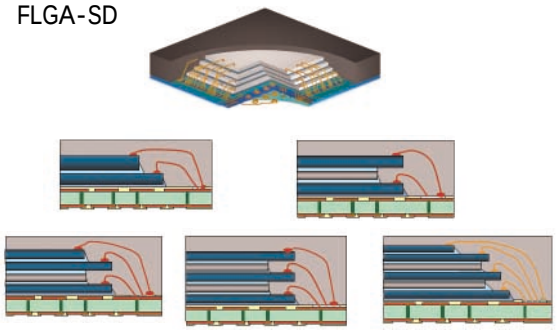
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	25 -110	1.10 - 4.35	0.25 - 2.27	0.20 - 0.90	0.05 - 0.41
Total (2L)	4 - 0	145 - 230	2.75 - 6.00	0.70 - 3.12	0.30 - 1.00	0.06 - 0.43
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	25 - 110	0.70 - 2.95	0.17 - 1.57	0.30 - 1.05	0.05 - 0.41
Total (4L)	4 - 9	145 - 230	2.35 - 4.60	0.62 - 2.42	0.40 - 1.15	0.06 - 0.43

Note: Net = Total Trace Length + Via

CROSS-SECTION

FLGA-SD



PACKAGE CONFIGURATIONS

Body Sizes (mm)	4x4 to 13x13
Terminal Count	8 to 200
Terminal Pitch (mm)	0.5 to 0.8
Typ. Pkg. Thickness	TFLGA-SD: 1.2mm VFLGA-SD: 1.0mm max. WFLGA-SD: 0.8mm max.

Corporate Office 10 Ang Mo Kio St. 65, #05-17/20 Techpoint, Singapore 569059 Tel: 65-6824-7777 Fax: 65-6720-7823
Global Offices USA 510-979-8000 JAPAN 81-3-5789-5850 CHINA 86-21-5976-5858 MALAYSIA 603-4257-6222
KOREA 82-31-639-8911 TAIWAN 886-3-593-6565 UK 44-1483-413-700 NETHERLANDS 31-38-333-2023

May 2006