



## EMIF03-SIM01

A.S.D.<sup>TM</sup>

### 3 LINES EMI FILTER INCLUDING ESD PROTECTION

#### MAIN APPLICATIONS

EMI filtering protection and ESD for :

- SIM Interface (Subscriber identify Module)

#### DESCRIPTION

The EMIF03-SIM01 is a highly integrated array designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences.

The EMIF03-SIM01 flip-chip packaging means the package size is equal to the die size. That's why EMIF03-SIM01 is a very small device.

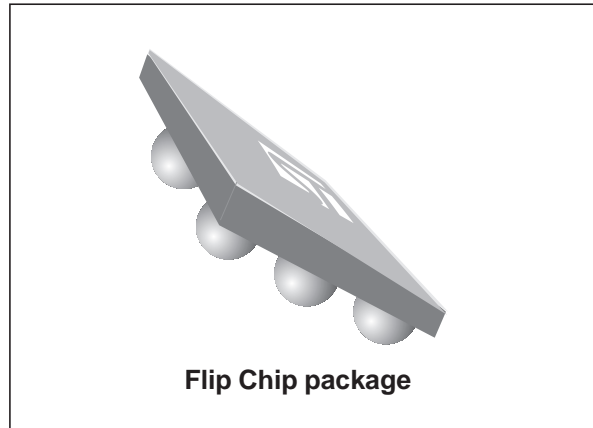
Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

#### BENEFITS

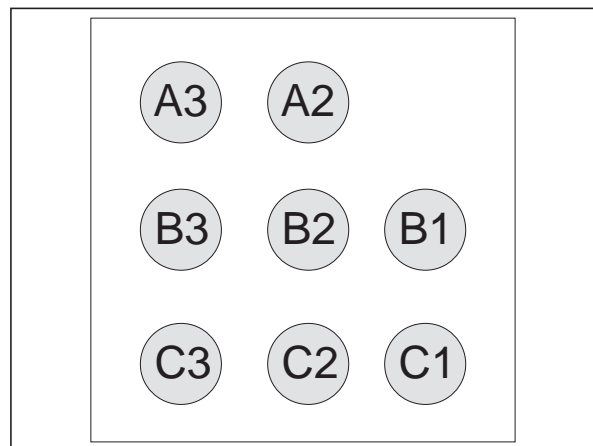
- 3 lines symmetrical (I/O) low-pass-filter
- High efficiency in EMI filtering
- Very low PCB space consuming: 1.6 x 1.6 mm<sup>2</sup>
- Very thin package: 0.65 mm
- High efficiency in ESD suppression on both input & output PINS (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.

#### COMPLIES WITH THE FOLLOWING STANDARDS :

**IEC61000-4-2** 15kV (air discharge)  
8 kV (contact discharge)  
on input & output pins.



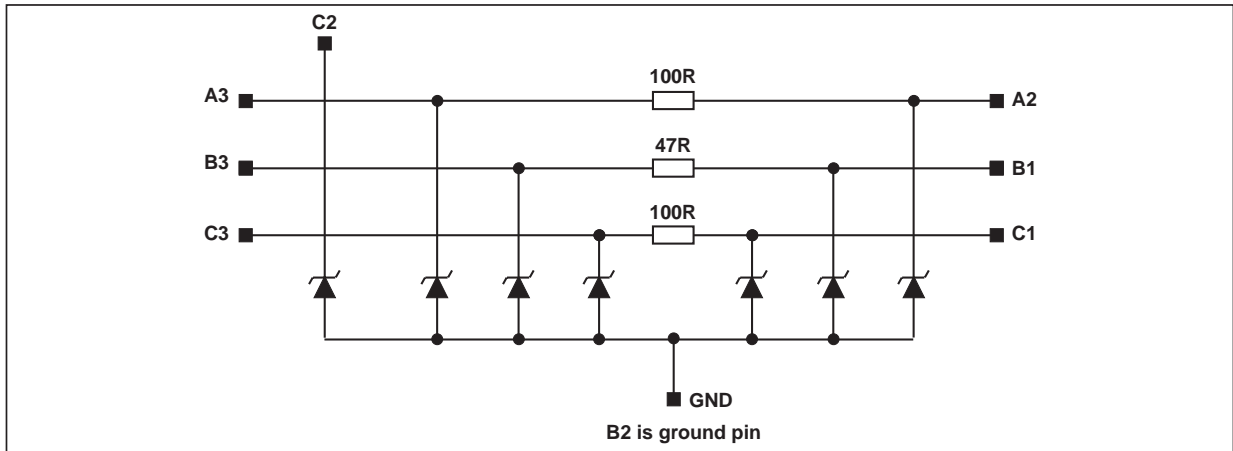
#### PIN CONFIGURATION (Ball side)



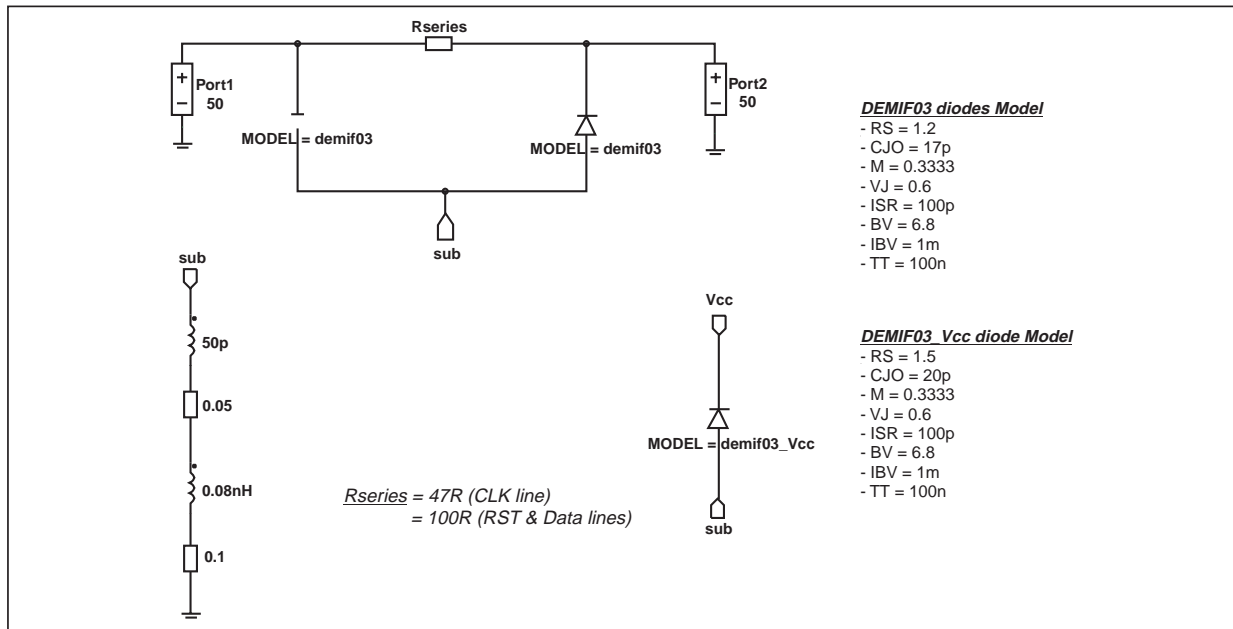
<sup>TM</sup> : ASD is a trademark of STMicroelectronics.

# EMIF03-SIM01

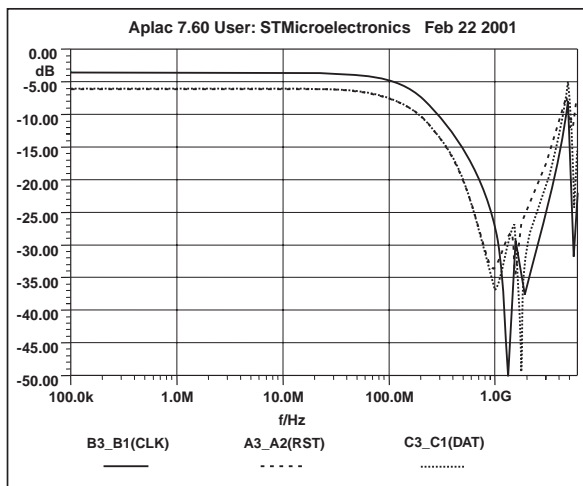
## Schematic



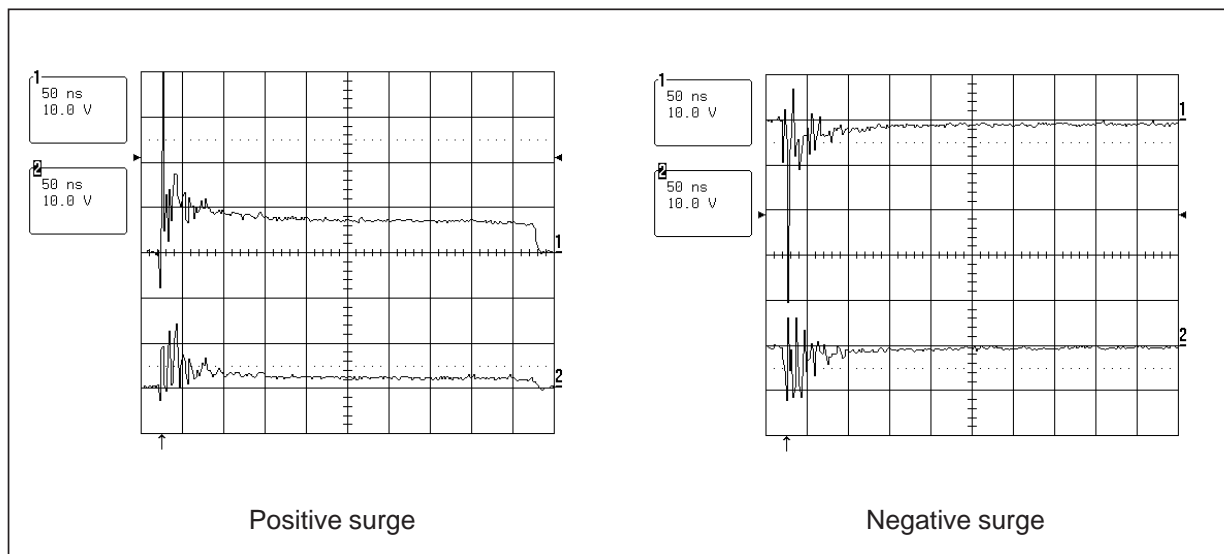
## Aplac model



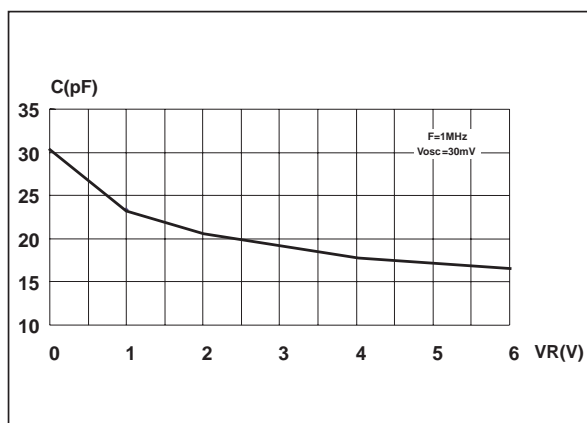
## Filtering behavior



## ESD response to IEC61000-4-2 (15kV air discharge)



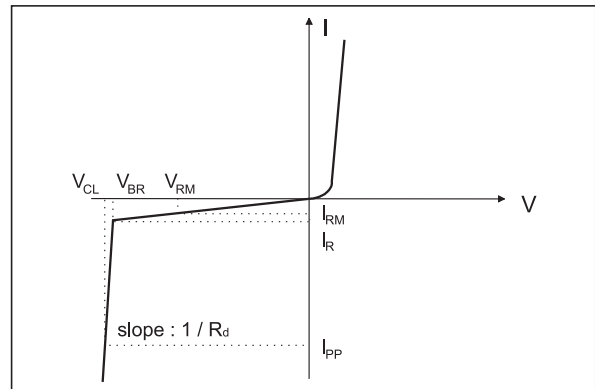
## Capacitance versus reverse applied voltage.

ABSOLUTE MAXIMUM RATINGS ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )

Symbol	Parameter and test conditions	Value	Unit
$V_{PP}$	ESD discharge IEC61000-4-2, air discharge ESD discharge IEC61000-4-2, contact discharge	15 8	kV
$T_j$	Junction temperature	125	$^{\circ}\text{C}$
$T_{op}$	Operating temperature range	-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-55 to +150	$^{\circ}\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ )

Symbol	Parameter
$V_{BR}$	Breakdown voltage
$I_{RM}$	Leakage current @ $V_{RM}$
$V_{RM}$	Stand-off voltage
$V_{CL}$	Clamping voltage
$R_d$	Dynamic impedance
$I_{PP}$	Peak pulse current



Symbol	Test conditions	Min.	Typ.	Max.	Unit
$V_{BR}$	$I_R = 1\text{ mA}$	6			V
$I_{RM}$	$V_{RM} = 3\text{ V}$			1	$\mu\text{A}$
$R_d$			1.5		$\Omega$
$R_1$		95	100	105	$\Omega$
$R_2$		44.65	47	49.35	$\Omega$
$R_3$		95	100	105	$\Omega$
$C_{line}$	@ 0V			35	pF

**TECHNICAL INFORMATION****FREQUENCY BEHAVIOR**

The EMIF03-SIM01 is firstly designed as an EMI / RFI filter. This low-pass filter is characterized by the following parameters:

- Cut-off frequency
- Insertion loss
- High frequency rejection

Figure A1 shows that attenuation is better than -20dB at mobile phone frequencies (800MHz to 2.5GHz).

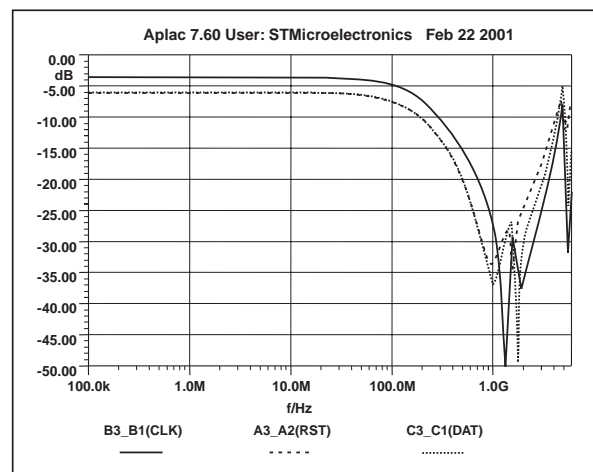
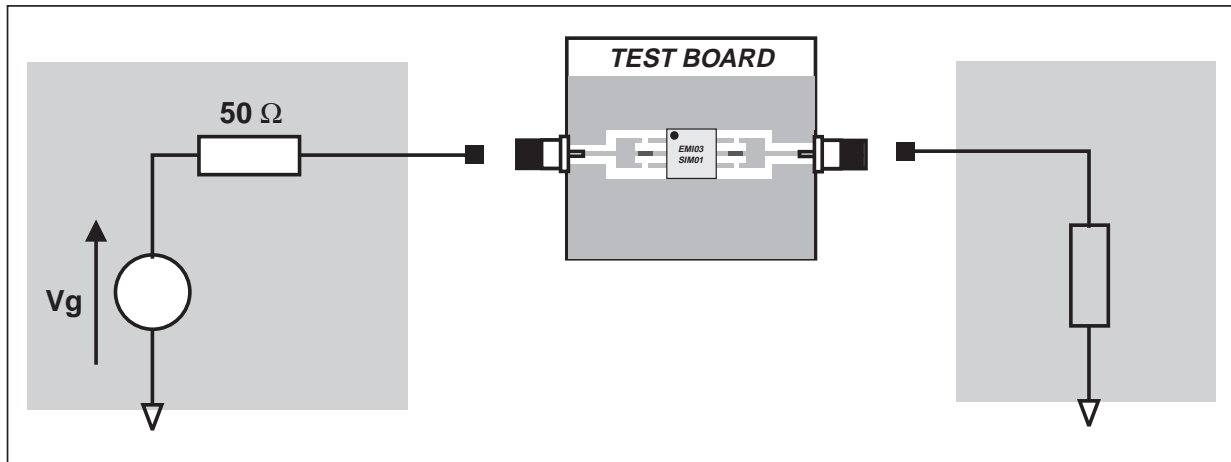
**Fig. A1:** Frequency response curve

Fig. A2: Measurements conditions



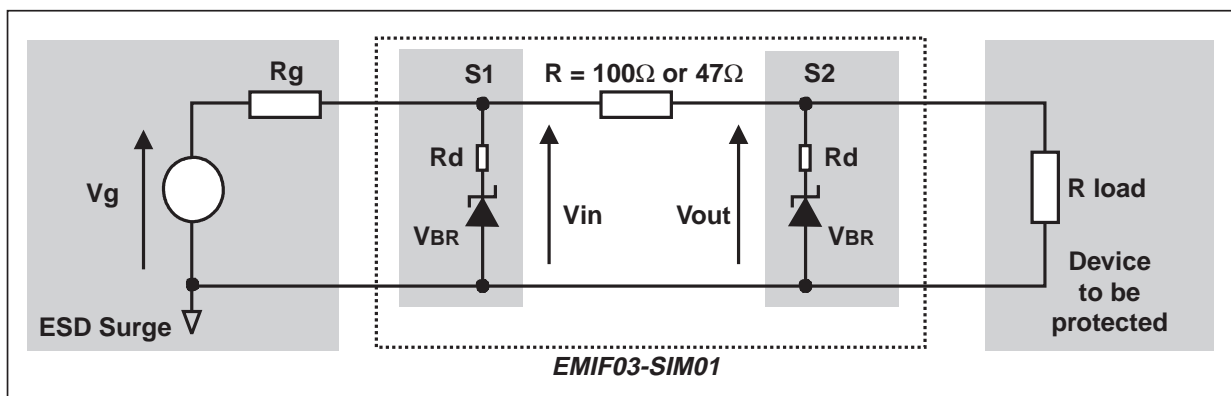
### ESD PROTECTION

In addition with the filtering the EMIF03-SIM01 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at:

$$V_{cl} = V_{br} + R_d \cdot I_{pp}$$

This protection function is splitted in 2 stages. As shown in Figure A3, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the  $V_{out}$  level.

Fig. A3: ESD clamping behavior



## EMIF03-SIM01

To have a good approximation of the remaining voltages at both  $V_{in}$  and  $V_{out}$  stages, we give the typical dynamic resistance value  $R_d$ . By taking into account these following hypothesis :  $R \gg R_d$ ,  $R_g \gg R_d$  and  $R_{load} \gg R_d$ , it gives these formulas:

$$V_{input} = \frac{R_g \cdot V_{br} + R_d \cdot V_g}{R_g}$$

$$V_{output} = \frac{R \cdot V_{br} + R_d \cdot V_{in}}{R}$$

The results of the calculation done for an IEC 1000-4-2 Level 4 Contact Discharge surge ( $V_g=8kV$ ,  $R_g=330\Omega$ ) and  $V_{br}=7V$  (typ.) give:

$$V_{input} = 43.36V$$

$$V_{output} = 7.65V (R = 100\Omega)$$

$$8.38V (R = 47\Omega)$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the  $V_{in}$  side. This parasitic effect is not present at the  $V_{out}$  side due the low current involved after the series resistance  $R$ .

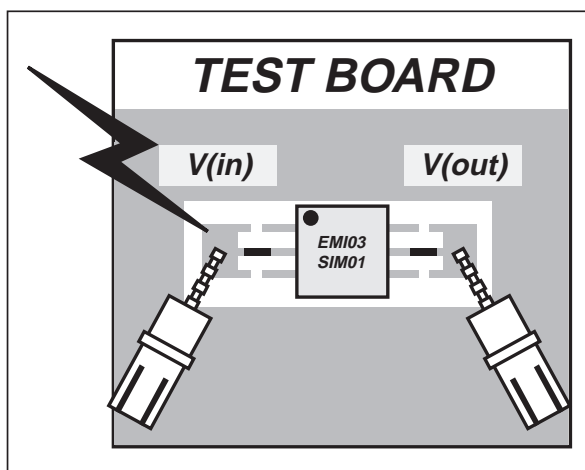
### LATCH-UP PHENOMENA

The early ageing and destruction of IC's is often due to latch-up phenomena which mainly induced by  $dV/dt$ . Thanks to its RC structure, the EMIF03-SIM01 provides a high immunity to latch-up by integration of fast edges. (Please refer to the response of the EMIF03-SIM01 to a 30 ns edge on Fig. A9)

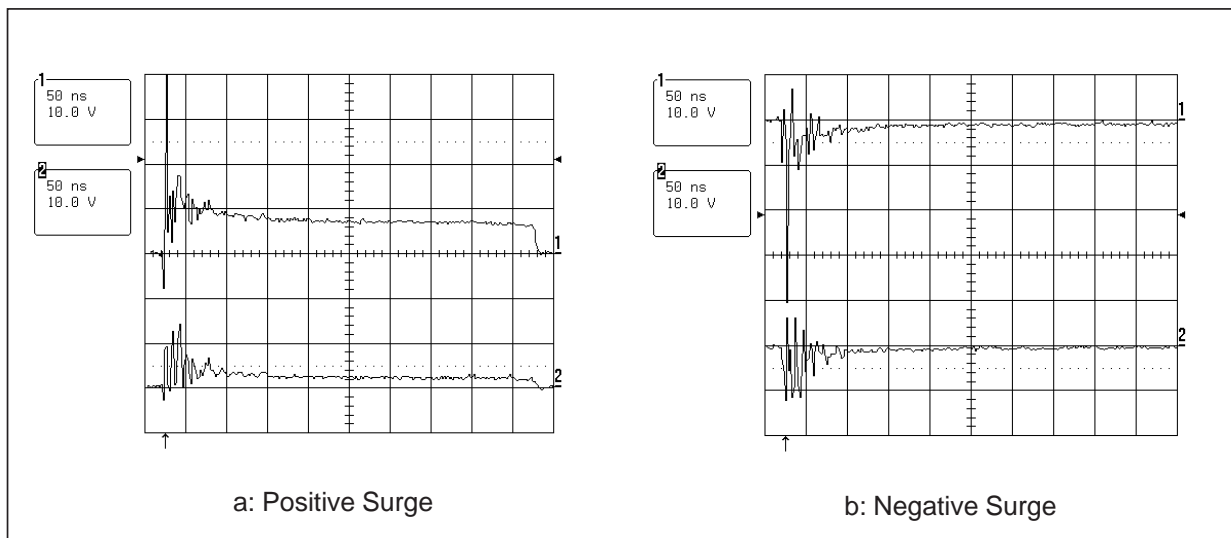
The measurements done here after show very clearly (Fig. A5a & A5b) the high efficiency of the ESD protection :

- almost no influence of the parasitic inductances on  $V_{out}$  stage
- $V_{out}$  clamping voltage very close to  $V_{br}$  for positive surge and close to ground for negative one

Fig. A4: Measurements conditions



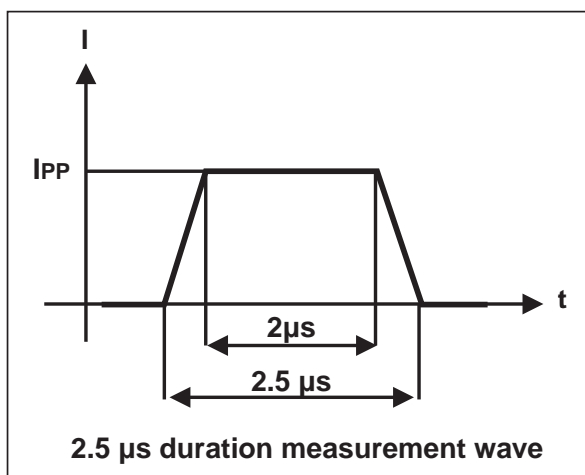
**Fig. A5:** Remaining voltage at both stages S1 (Vin1) and S2 (Vout1) during ESD surge



Please note that the EMIF03-SIM01 is not only acting for positive ESD surges but also for negative ones. For negative surges, it clamps close to ground voltage as shown in Fig. A5b.

**Note:** Dynamic resistance measurements

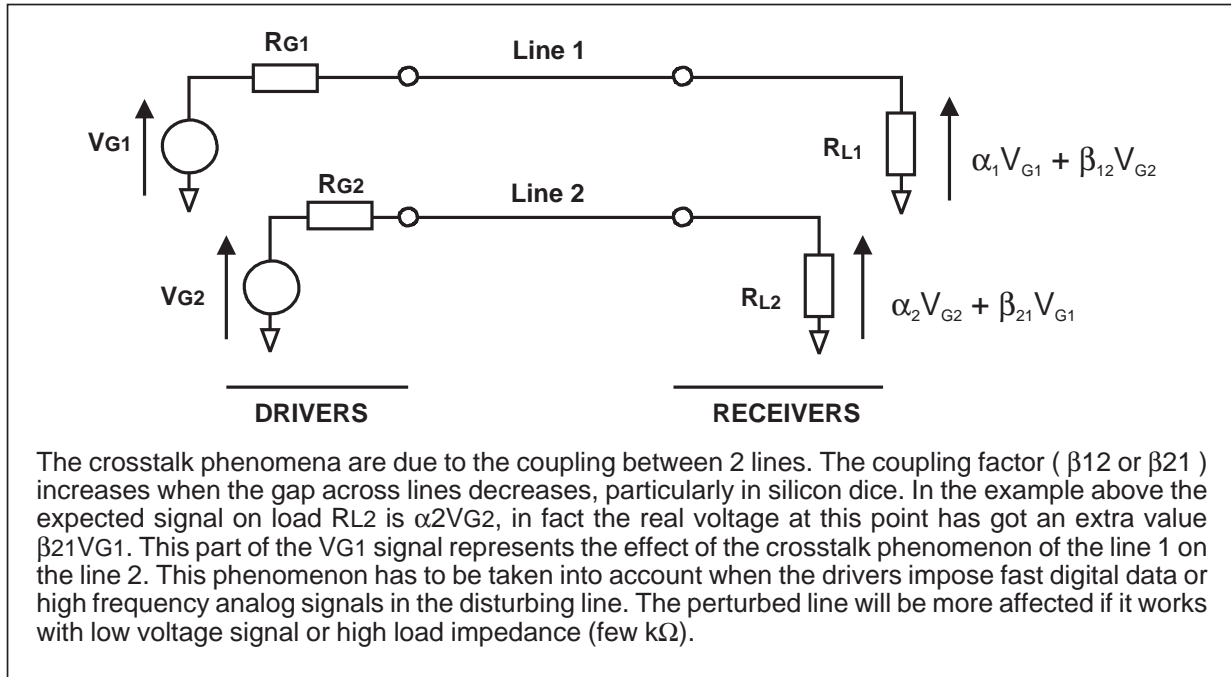
**Fig. A6:** Rd measurement current wave



As the value of the dynamic resistance remains stable for a surge duration lower than 20 $\mu$ s, the 2.5 $\mu$ s rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd

## CROSSTALK BEHAVIOR

Fig. A7: Crosstalk phenomena



## 1- Digital crosstalk

Fig. A8: Digital crosstalk measurements

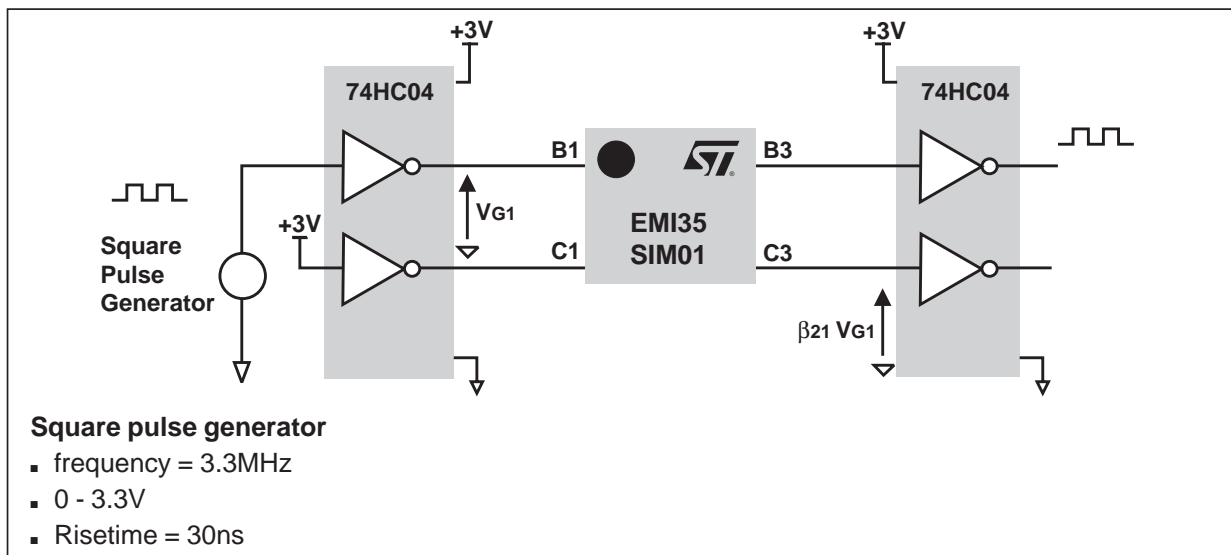
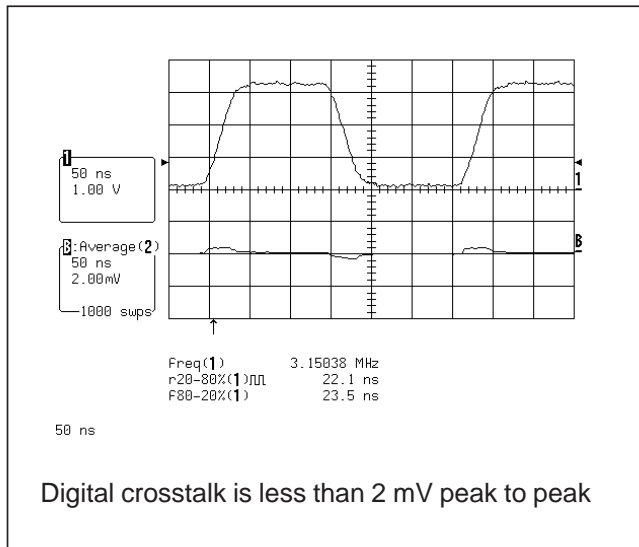


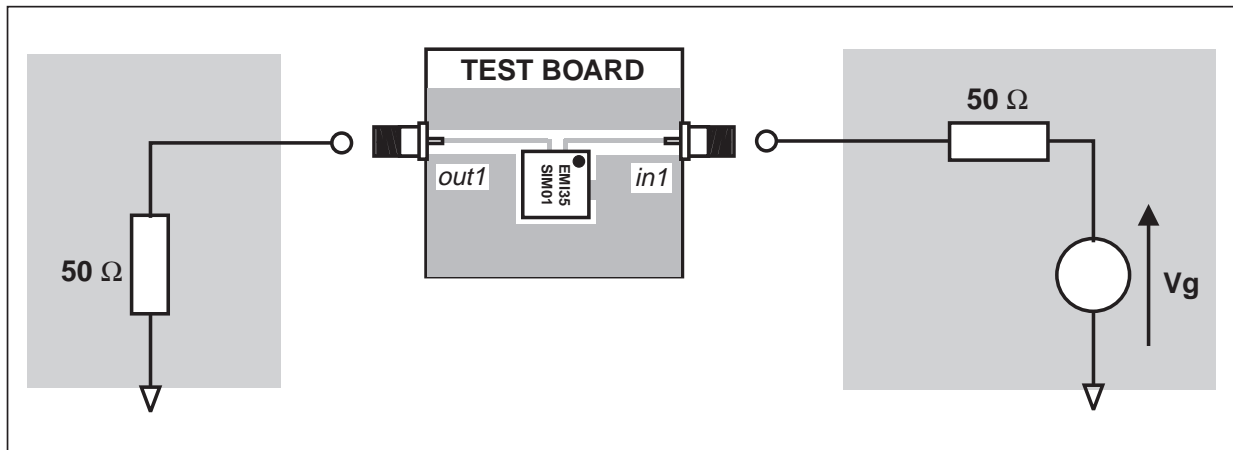


Fig. A9: Digital crosstalk results



## 2- Analog crosstalk

Fig. A10: Analog crosstalk phenomena



# EMIF03-SIM01

**Fig. A11: Analog crosstalk results**

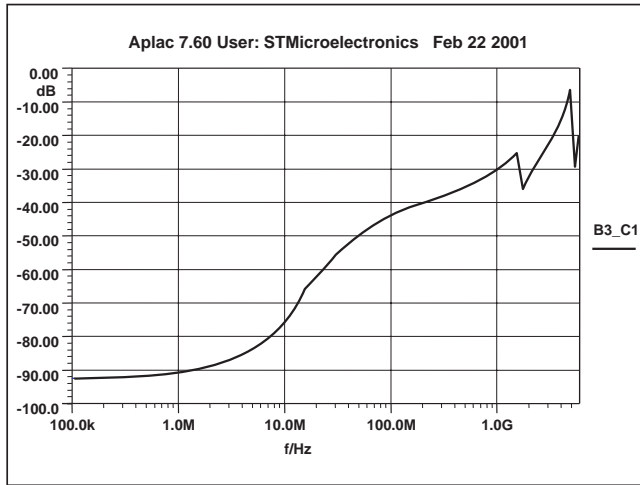
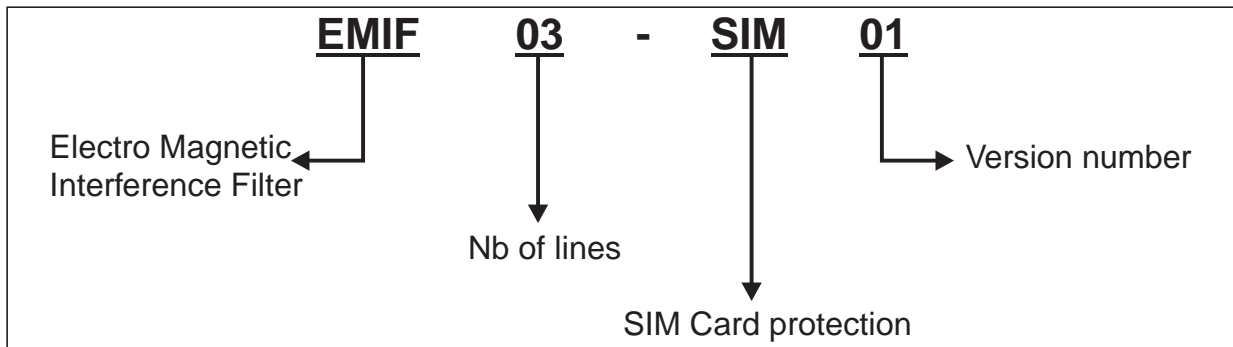


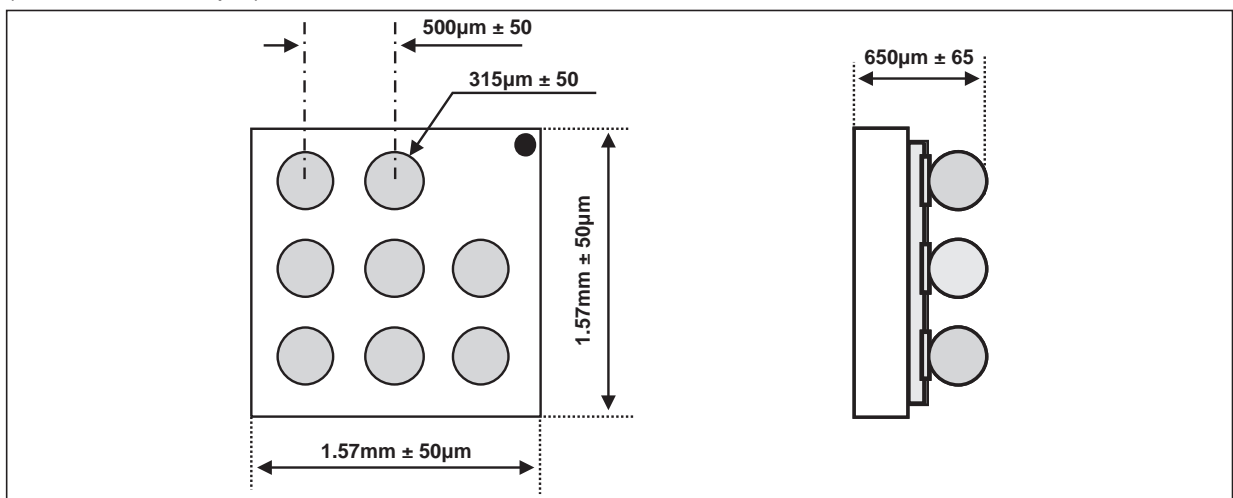
Figure A10 gives the measurement circuit for the analog application. In Figure A11, the curve shows the EMIF03-SIM01 provides a crosstalk immunity better than - 20dB up to 3GHz.

## ORDER CODE

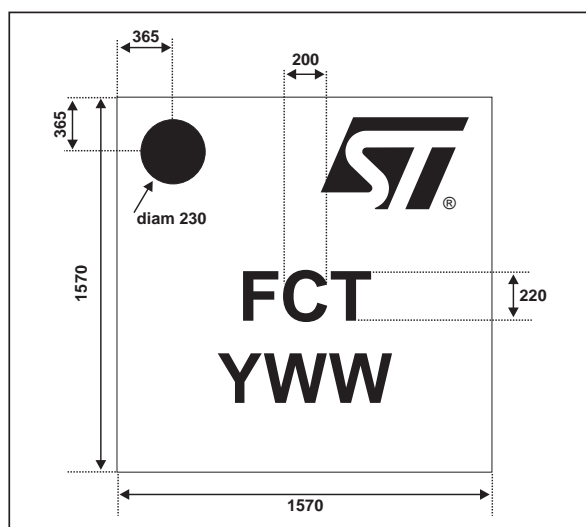


## PACKAGE MECHANICAL DATA

(all dimensions in  $\mu\text{m}$ )



- Bottom side (ball view): Pin A1 missing for die orientation
- Top side (balls underneath): see the marking .

**MARKING and DIE SIZE (typical values)**

YWW: Date code (year + week code)

**PACKING**

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF03-SIM01	FCT	Flip Chip	3.3 mg	5000	Tape & reel 7"

**Note:** More packing information are available in the application note AN1235: "Flip-Chip: Package description and recommendations for use"

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