PROCESS CPS057

Silicon Controlled Rectifier

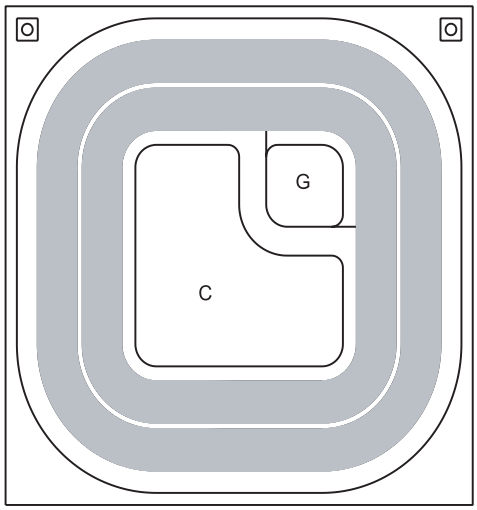
Sensitive Gate SCR Chip

Central Semiconductor Corp.

PROCESS DETAILS

Process	GLASS PASSIVATED MESA
Die Size	57 x 57 MILS
Die Thickness	8.7 MILS ± 0.6 MILS
Cathode Bonding Pad Area	24 x 14 MILS
Gate Bonding Pad Area	7.9 x 7.9 MILS
Top Side Metalization	Al - 45,000Å
Back Side Metalization	Al/Mo/Ni/Ag - 32,000Å

GEOMETRY



BACKSIDE ANODE R0

GROSS DIE PER 4 INCH WAFER

3,374

PRINCIPAL DEVICE TYPES

CS39-4D
2N2323 thru 2N2329
CS223-4M

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
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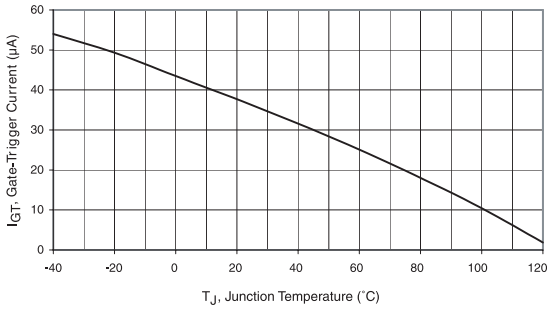
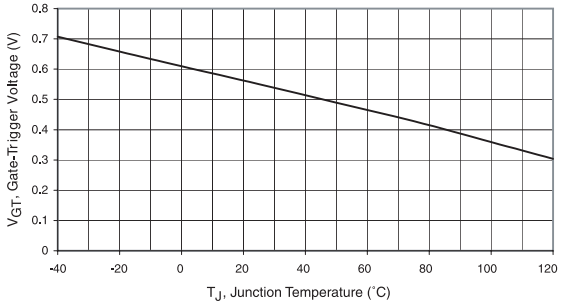
PROCESS CPS057
Typical Electrical Characteristics

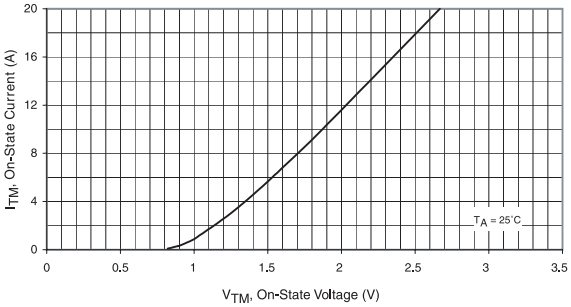
Typical Gate-Trigger Current



Typical Gate-Trigger Voltage



Typical On-State Voltage



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