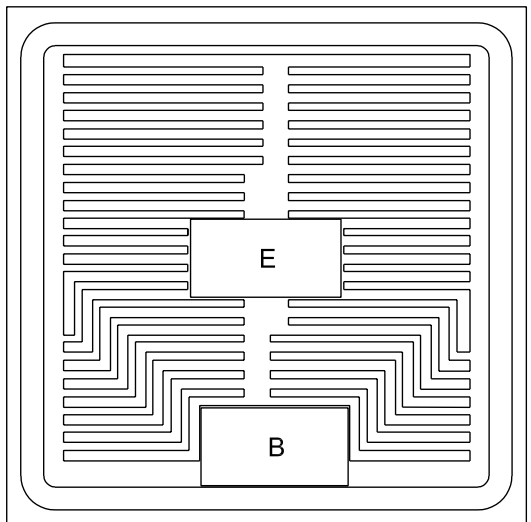


PROCESS CP287
Power Transistor
8.0 Amp NPN Silicon Power Transistor Chip

PROCESS DETAILS

| | |
|--------------------------|--------------------------------------|
| Die Size | 130 x 130 MILS |
| Die Thickness | 9.5 MILS |
| Base Bonding Pad Area | 37 x 20 MILS |
| Emitter Bonding Pad Area | 38 x 20 MILS |
| Top Side Metalization | Al - 45,000Å |
| Back Side Metalization | Ti/Ni/Ag - (3000Å, 10,000Å, 10,000Å) |

GEOMETRY



GROSS DIE PER 4 INCH WAFER

974

PRINCIPAL DEVICE TYPES

MJE13007

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centrasemi.com

R0 (26-July 2005)