CHT-CG-050

Preliminary datasheet
Version 0.4 (08/2005)

Versatile High Temperature Clock Generator

General Description

The CHT-CG-050 is a versatile High-Temperature crystal clock generator with extended functional capabilities. The chip features a programmable crystal oscillator driver with an enable/disable control signal, an external clock input, a programmable divider chain and a programmable strength three-state output buffer. Using an external crystal, it is intended to provide reliable precision performance throughout the -30 to +225°C temperature range for supply voltages between 3V and 5V.

The CHT-CG-050 can operate with crystals from 1MHz to 50MHz. The output frequency can be selected by means of a programmable divider, providing division factors of one, two, four and eight. The programmability of the crystal driver allows working with a wide range of crystals. A crystal driver enable pin (**/XtalEn**) is included for extremely low power applications, as well as an output enable pin (**/OE**). In applications requiring only a precision divider chain, where an external clock source is already present, the crystal driver may be bypassed by means of inputs **ExtClkIn** and **ExtClkEn**.

Features

- 3V to 5V power supply
- Qualified from -30 to +225°C (T_j)
- Operational up to +250°C (T_j)
- Two input sources: crystal (1 to 50 MHz), external clock (DC to 50MHz)
- Operation from 32.768kHz crystals
- Programmable frequency divider: f_{in}, $f_{in}/2$, $f_{in}/4$ and $f_{in}/8$
- Programmable crystal driver and output driver strength
- Available in several standard packages or as die

Applications

- Well logging, Automotive, Aeronautics & Aerospace
- Precision timing

Pin Description

C1_10pF
C1_20pF
C2_10pF
C2_20pF — Built-in capacitors with a common terminal connected to Vss.

DIV_0
DIV_1 — Inputs to set the division factor.

TRUTH TABLE

DIV_1	DIV_0	Factor
0	0	1
0	1	2
1	0	4
1	1	8

DRI_0
DRI_1 — Inputs to set the output buffer strength.

TRUTH TABLE

DRI_1	DRI_0	Strength
0	0	8mA
0	1	16mA
1	0	24mA
1	1	32mA

ExtClkEn — When driven HIGH, operation from the external clock source is selected.

ExtClkIn — Input for an external clock source.

FOUT — Output signal.

/OE — When driven LOW, output is enabled, When driven HIGH, output is at high impedance.

R2 — Terminal of a 200Ω resistor. The other terminal of this resistor is connected to X2.

Pin Description (Cnt'd)

Vdd Circuit core power supply terminal.

Vdd_Buff Output buffer power supply terminal.

Vss Circuit core ground terminal.

Vss_Buff Output buffer ground terminal.

X1 Input of crystal driver

X2 Output of crystal driver

XtalDR_0
XtalDR_1 Inputs to set the crystal drive strength.

TRUTH TABLE

XtalDR_1	XtalDR_0	Strength
0	0	Lowest
0	1	Low
1	0	High
1	1	Highest

/XtalEn When driven LOW, the crystal oscillator is enabled. When driven HIGH, the crystal oscillator is stopped.

Internal architecture

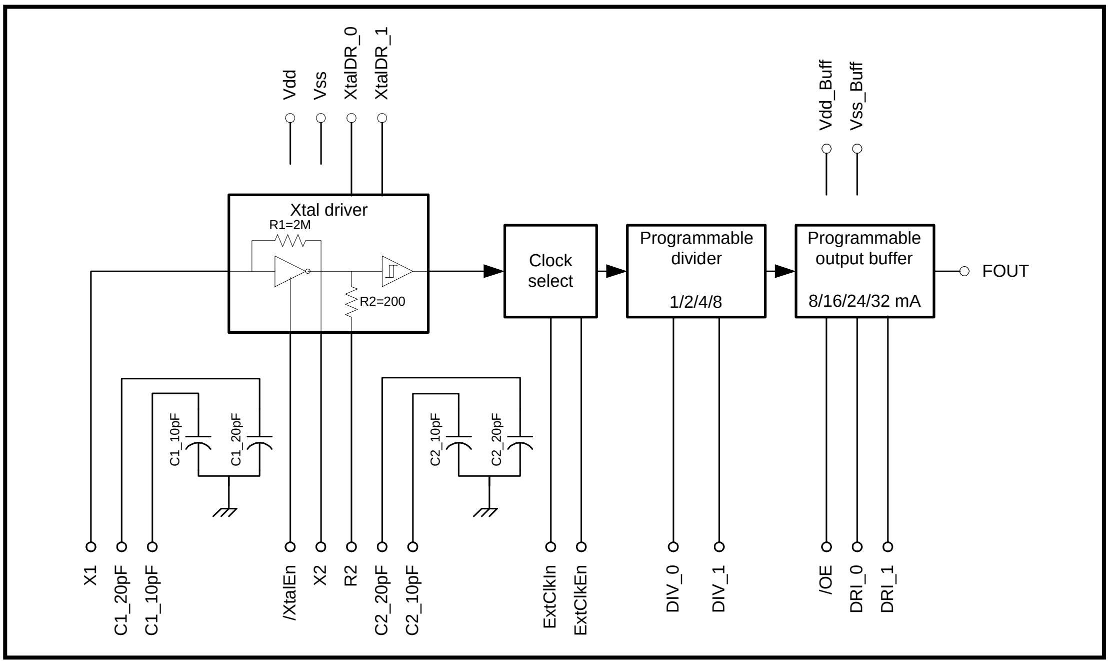


Figure 1. CHT-CG-050: simplified blocks diagram.

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND	-0.5 to 6.0V
Voltage on any Pin to GND	-0.5 to V_{DD}+0.3V

ESD Rating (expected)

Human Body Model	1kV

Operating Conditions

Supply Voltage V_{DD} to GND	3.3V to 5V
Junction temperature	-30°C to +225°C

Operation up to +250°C (T_j) can be obtained with little increase of the current consumption.

Electrical Characteristics

Unless otherwise stated: V_{DD}=5V, T_j=25°C. **Bold** figures indicate values over the whole temperature range (-30°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage **V_{DD}**		3.13		5.5	V
Current consumption[a] **Idd**	V_{DD} = 3V, F_{IN} = 1.8MHz Output disabled (/OE: HIGH)		**0.141**		mA
	V_{DD} = 3V, F_{IN} = 1.8MHz Output enabled (/OE: LOW) C_L = 22pF		0.374 **0.405**		
	V_{DD} = 3V, F_{IN} = 32MHz Output disabled (/OE: HIGH)		**0.800**		
	V_{DD} = 3V, F_{IN} = 32MHz Output enabled (/OE: LOW) C_L = 22pF		5.08 **5.15**		
	V_{DD} = 5V, F_{IN} = 1.8MHz Output disabled (/OE: HIGH)		**1.01**		
	V_{DD} = 5V, F_{IN} = 1.8MHz Output enabled (/OE: LOW) C_L = 22pF		1.40 **1.44**		
	V_{DD} = 5V, F_{IN} = 32MHz Output disabled (/OE: HIGH)		**1.84**		
	V_{DD} = 5V, F_{IN} = 32MHz Output enabled (/OE: LOW) C_L = 22pF		8.97 **9.08**		
	V_{DD} = 5V, F_{IN} = 50MHz Output disabled (/OE: HIGH)		**2.49**		
	V_{DD} = 5V, F_{IN} = 50MHz Output enabled (/OE: LOW) C_L = 22pF		14.82 **15.03**		
Minimum HIGH level output voltage **V_{OH}**	R_{LOAD} = 600Ω	**4.67**			V
Maximum LOW level output voltage **V_{OL}**	R_{LOAD} = 600Ω			**0.30**	V
Minimum HIGH level input voltage **V_{IH}**		**3.15**			V
Maximum LOW level input voltage **V_{IL}**				**1.35**	V
Internal capacitors					
Initial accuracy			17		%
Temperature dependence	ΔT = 200°C		0.6		%
TC1	$C(T) = C(T_0)\,[1+TC1.(T-T_0)+TC2.(T-T_0)^2]$		0.023		10^{-3}/K
TC2			0.013		$10^{-6}/K^2$

[a] The given value includes the consumption due to the load. Current consumption due to a capacitive load must be computed according to $I_{LOAD} = C_L.V_{DD}.f$.

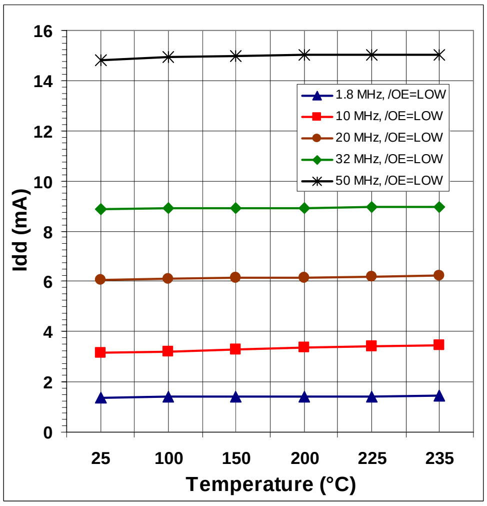
AC Electrical Characteristics

Unless otherwise stated: V_{DD}=5V, T_j=25°C. **Bold** figures indicate values over the whole temperature range (-30°C < T_j < +225°C).

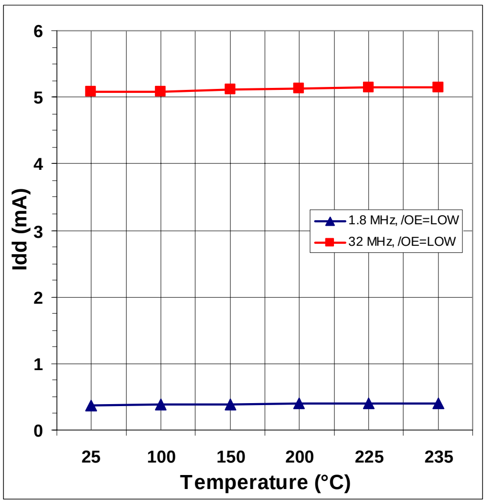
Parameter	Condition	Min	Typ	Max	Units
Frequency range **F_{IN}**		1		50	MHz
Duty cycle @ 50% V_{DD} **DC**[b c]	F_{IN}=1.8MHz, V_{DD} = 5V			**48/52**	%
	F_{IN}=32MHz, V_{DD} = 5V		**47/53**	**45/55**	
	F_{IN}=50MHz, V_{DD} = 5V			**45/55**	
Output rise time[d] 10% to 90% V_{DD} **t_r**	Vdd = 5V, Z_{LOAD} = 1MΩ // 22pF		**3.0**		ns
	Vdd = 5V, Z_{LOAD} = 600Ω // 15pF		2.5		
Output fall time[e] 10% to 90% V_{DD} **t_f**	Vdd = 5V, Z_{LOAD} = 1MΩ // 22pF		**2.5**		ns
	Vdd = 5V, Z_{LOAD} = 600Ω // 15pF		2.1		
Oscillation established after Vdd goes high[f] **$t_{power-on}$**	V_{DD} from 0 to 5V		1.2 **3.2**		ms
Oscillation established after /XtalEn goes LOW[g] **$t_{start-up}$**	V_{DD} = 5V /XtalEn from LOW to HIGH		0.6 **1.4**		ms

[b] Duty cycle is measured with a unitary division factor and Z_{LOAD} = 1050Ω // 22pF.
[c] Depends on used crystal and **R2** value.
[d] Depends on load conditions and **DRI_0**, **DRI_1** settings.
[e] Depends on load conditions and **DRI_0**, **DRI_1** settings.
[f] Depends on used crystal and **XtalDR_0**, **XtalDR_1** settings.
[g] Depends on used crystal and **XtalDR_0**, **XtalDR_1** settings.

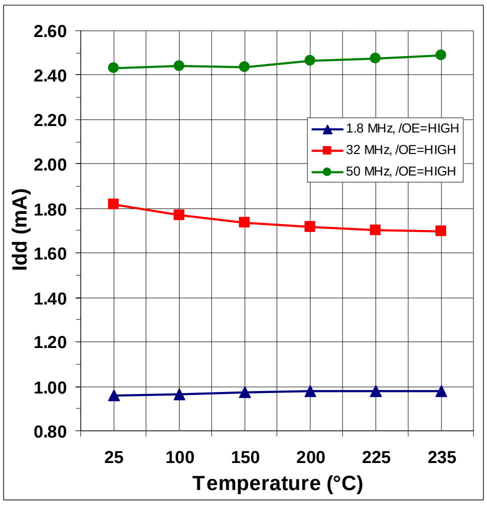
Typical Performance Characteristics



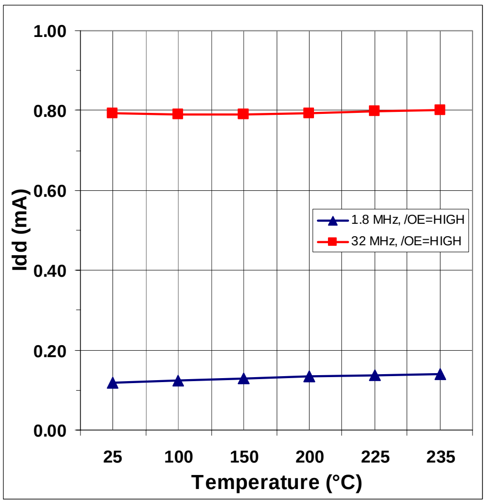
Current consumption, V_{DD} = 5V, /OE = LOW, C_L = 22pF



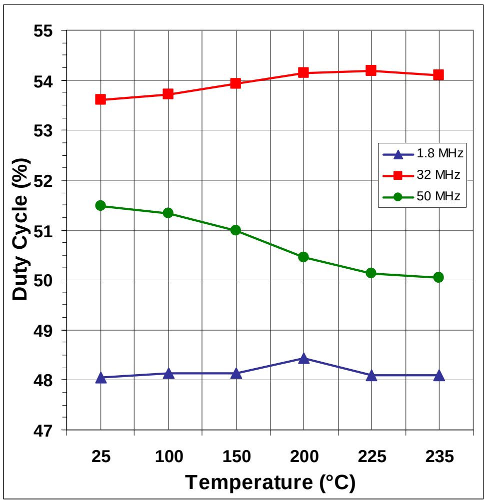
Current consumption, V_{DD} = 3V, /OE = LOW, C_L = 22pF



Current consumption, V_{DD} = 5V, /OE = HIGH



Current consumption, V_{DD} = 3V, /OE = HIGH



Duty cycle, V_{DD} = 5V

Circuit functionality

Operating conditions

The CHT-CG-050 has been qualified for supply voltages ranging from 3V up to 5.5V. The upper limit is imposed by the technology on which the CHT-CG-050 is implemented.

The qualification temperature range extends from -30°C to +225°C, though functionality is above +250°C is achieved with little increase of the current consumption.

Crystal driver

XtalDR_0 and **XtalDR_1** allow the crystal driver to change its strength to be able to oscillate with a wide range of crystals, under any supply (3V to 5V) and temperature (up to 225°C) condition.

The presence of integrated passive components offers a great versatility to the final user. Highly temperature-stable capacitors allow for a nearly-constant crystal load along the whole temperature range. Internal passive components can be bypassed or tied to ground if needed.

/XtalEn enables or disables the crystal oscillator to operate, allowing the CHT-CG-050 to be embedded into power-optimized high-temperature applications.

Clock source selector

By means of **ExtClkEn** and **ExtClkIn**, the CHT-CG-050 is able to operate either from its internal crystal oscillator or from an external clock source.

Frequency divider

Four division factors (1, 2, 4 and 8) can be selected depending on the levels at the control lines **DIV_0** and **DIV_1**.

Output buffer

A programmable-strength output buffer, controlled by **DRI_0** and **DRI_1**, enables the CHT-CG-050 to drive a large range of output loads, improving the output signal integrity. The four possible output strengths are 8mA, 16mA, 24mA and 32mA.

The output buffer has supply terminals independent from the rest of the circuit, allowing the system designer to properly decouple them in noise-sensitive application.

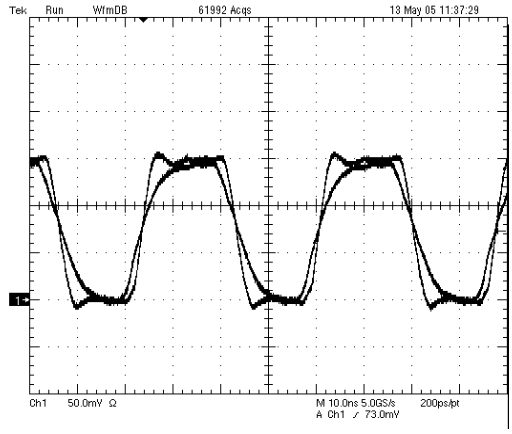


Figure 2. Effect of **DRI_0** and **DRI_1** on the output signal.

Figure 2 shows the superposition of the output signal when **DRI_0**, **DRI_1** = LOW and **DRI_1** is then set to HIGH, V_{DD}=3V, T=235°C, Freq = 27MHz. As a result, the signal integrity is improved.

Packaging options

As mentioned above, the layout of the CHT-CG-050 allows for a very high level of flexibility for the system designer. Several packaging configurations are possible, from 8-pin to 24-pin standard carriers.

At the packaging stage, many functional features can be enabled or safely disabled in order to optimize the form factor according to the final user needs.

Typical application

The CHT-CG-050 offers the final user several possible configurations depending upon the characteristics of the target application.

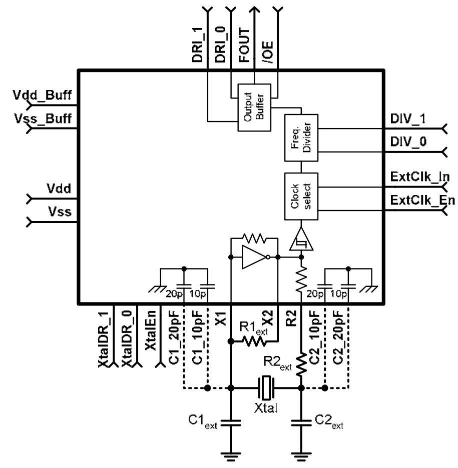


Figure 3. Full configuration.

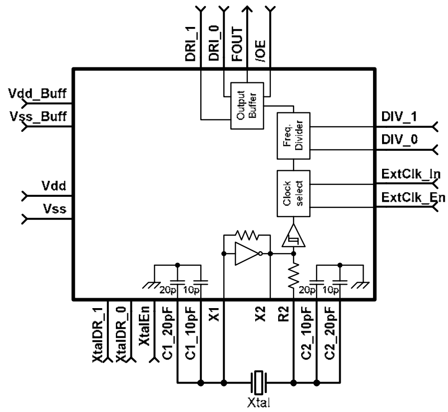


Figure 4. Minimal configuration.

Dashed lines in Figure 3 indicate optional connections. Figure 4 shows the minimal possible configuration with no external components. Any configuration in between those of Figure 3 and Figure 4 can be obtained by properly bypassing or tying to ground the corresponding internal component.

Any programmable feature can be changed on-the-fly, allowing the CHT-CG-050 to accommodate to new operating conditions in smart or adaptive applications.

Possible Packaging Options

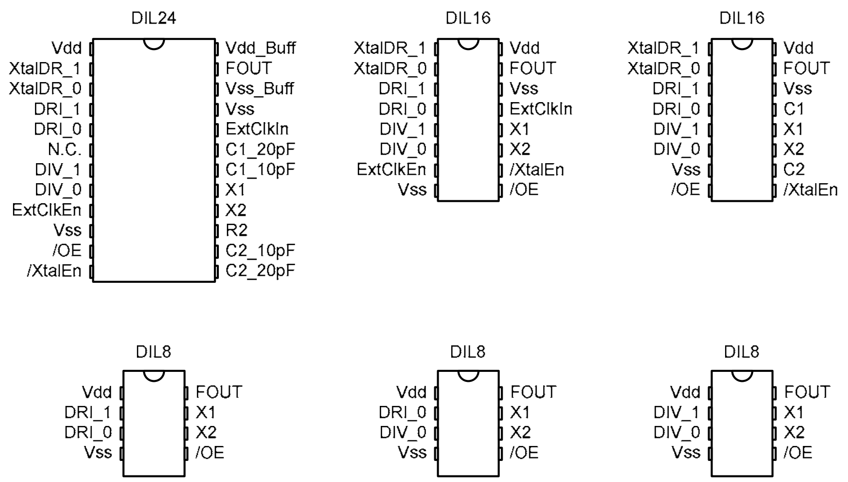


Figure 5. CHT-CG-050: possible packaging options.

NOTES:

- **The CHT-CG-050 can also be ordered as die.**
- **Packaging options shown are only indicative. Other possibilities are also available.**
- **Ask CISSOID for other packaging configurations.**

Contact & Ordering

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