

9- 19GHz Buffer Splitter Amplifier

GaAs Monolithic Microwave IC

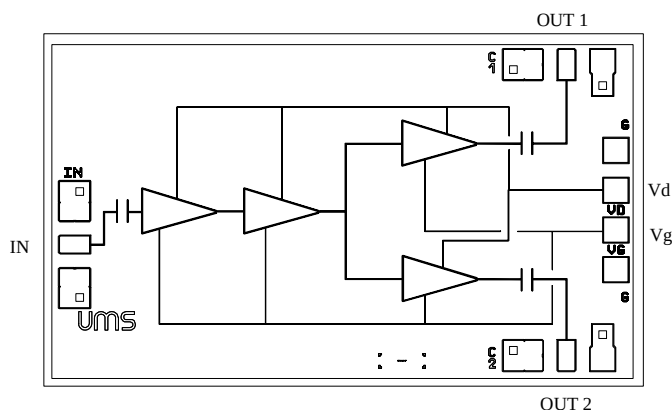
Description

The CHA2296 is a broadband buffer splitter three-stage monolithic amplifier.

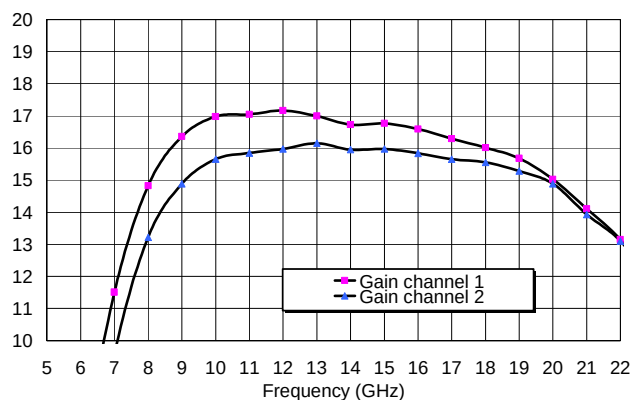
It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Typical on wafer measurements : Gain (dB)



Main Features

- Broadband performance : 9-19GHz
- 14dBm saturated output power.
- 16dB $\pm$ 1.5dB gain
- Very good broadband matching
- Low DC power consumption, 190mA @ 3.5V
- Chip size : 2.26 X 1.33 X 0.10 mm

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	9		19	GHz
G	Small signal gain	13	16		dB
Psat	Saturated Output power	12	14		dBm
Id_small signal	Bias current		190	250	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.5V Vg tuned for Id=190mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	9		19	GHz
G	Small signal gain (1)	13	16		dB
ΔG	Small signal gain flatness (1)		± 1.5		dB
Is	Reverse isolation (1)		60		dB
Ic	Isolation between channels (1)		20		dB
Psat	Saturated output power (1)	12	14		dBm
VSWRin	Input VSWR (1)			2.0:1	
VSWRout	Output VSWR (1)			2.0:1	
Id_small signal	Bias current		190	250	mA

(1) These values are representative for on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vds	Drain bias voltage_small signal	4.0	V
Ids	Drain bias current_small signal	300	mA
Vgs	Gate bias voltage	-2 to +0.4	V
Vdg	Negative Drain Gate voltage (= Vds – Vgs)	+5	V
P _{in}	Maximum peak input power overdrive (2)	+15	dBm
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

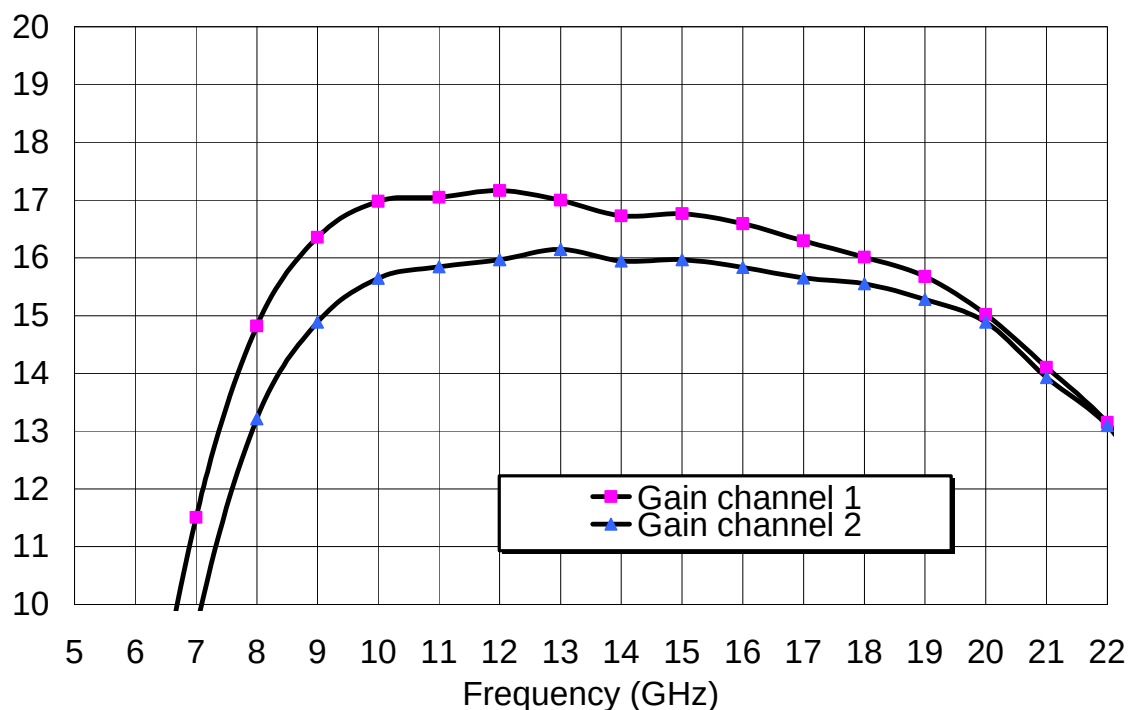
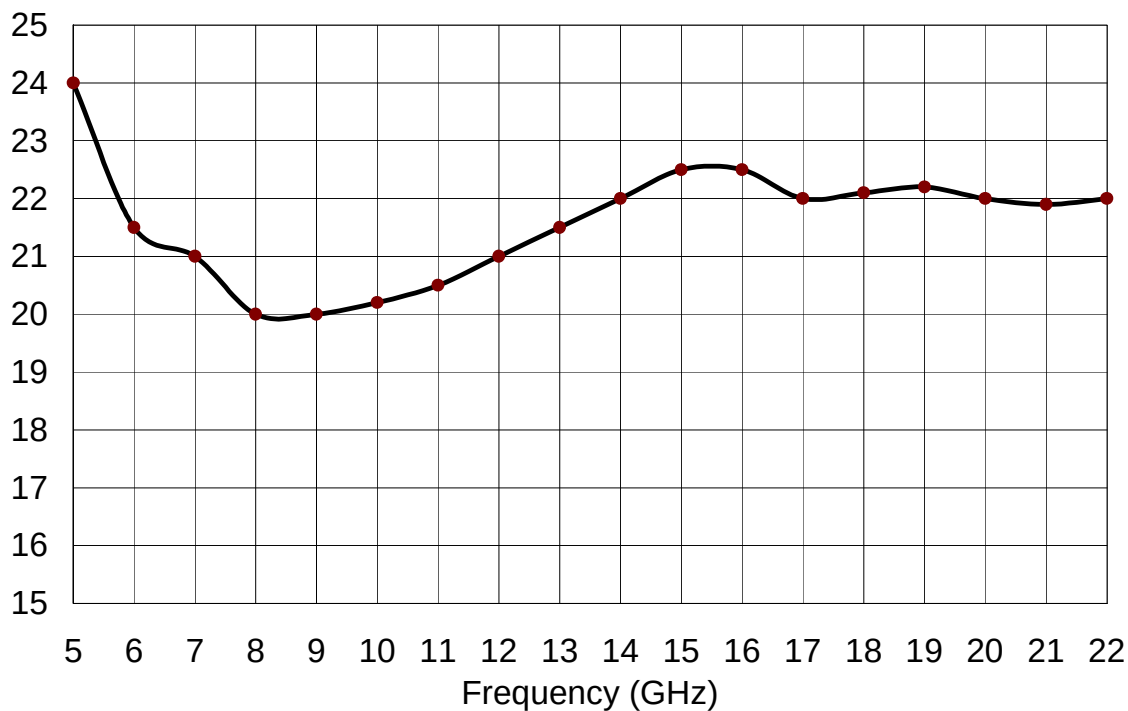
(2) Duration < 1s.

Typical Scattering Parameters (On wafer S_{ij} measurements)Bias Conditions : $V_d = 3.5$ Volt, V_g tuned for $I_d = 190$ mA.

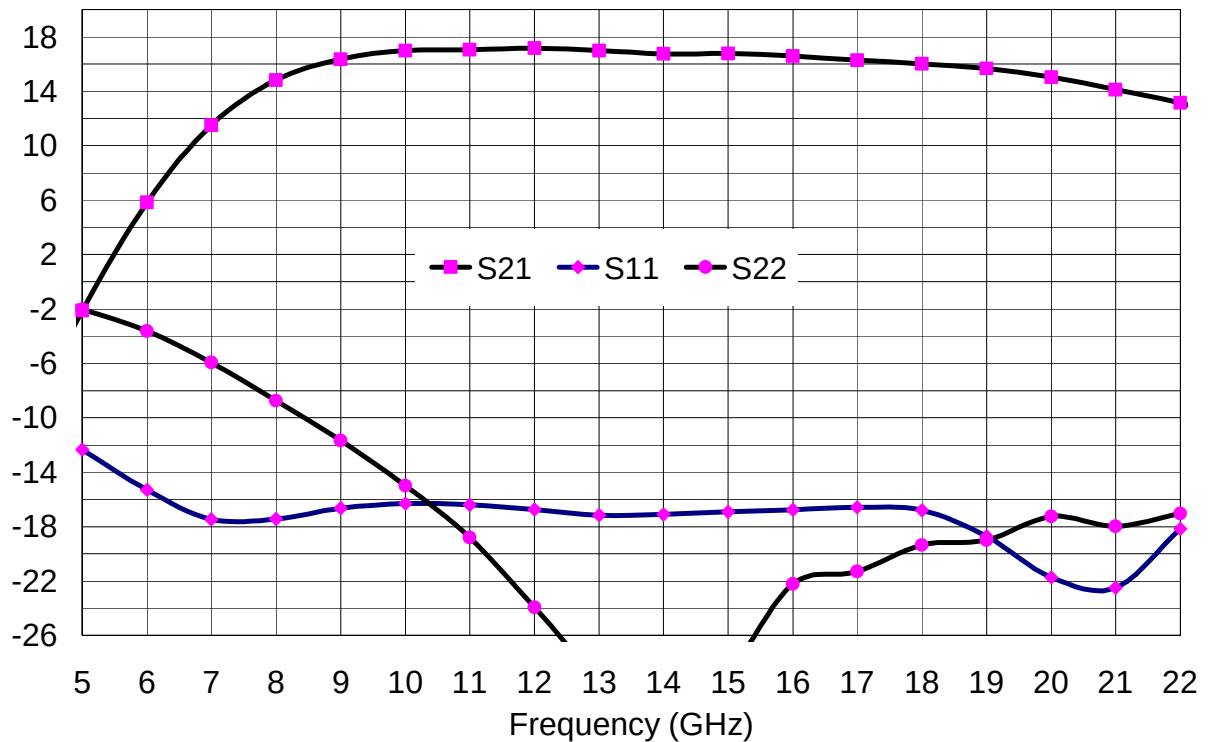
Channel	Freq. GHz	S11 dB	S11 /°	S12 dB	S12 /°	S21 dB	S21 /°	S22 dB	S22 /°
1	5	-12.34	-94.87	-66.94	-38.90	-2.14	41.09	-2.04	-88.40
1	6	-15.29	-102.89	-67.83	-87.89	5.84	-11.01	-3.64	-108.79
1	7	-17.46	-97.03	-66.67	-87.44	11.51	-68.31	-5.95	-127.83
1	8	-17.44	-90.47	-66.06	-140.51	14.82	-125.78	-8.74	-143.37
1	9	-16.63	-91.57	-67.50	-123.38	16.36	-177.87	-11.67	-156.13
1	10	-16.30	-97.50	-67.33	175.31	16.98	136.79	-15.00	-167.18
1	11	-16.41	-103.81	-65.23	-177.40	17.05	97.30	-18.81	-176.53
1	12	-16.72	-107.46	-69.95	145.63	17.17	61.74	-23.94	178.88
1	13	-17.15	-111.72	-66.02	138.93	16.99	27.77	-29.04	-146.27
1	14	-17.10	-110.94	-97.44	-155.97	16.72	-3.82	-31.35	-89.10
1	15	-16.93	-113.66	-70.70	166.71	16.76	-32.72	-28.61	-91.76
1	16	-16.76	-116.42	-63.72	170.65	16.59	-63.33	-22.22	-116.88
1	17	-16.59	-121.64	-70.22	97.77	16.29	-92.58	-21.30	-125.33
1	18	-16.80	-129.92	-64.92	154.63	16.01	-122.60	-19.35	-140.70
1	19	-18.71	-137.93	-66.62	-138.40	15.67	-151.31	-18.99	-154.19
1	20	-21.72	-133.29	-57.46	176.38	15.02	177.95	-17.24	-168.27
1	21	-22.50	-91.29	-60.06	117.94	14.10	148.71	-17.98	178.00
1	22	-18.17	-73.84	-66.35	142.93	13.15	119.32	-17.05	169.87
2	5	-12.32	-94.79	-67.52	-31.29	-4.49	37.49	-2.04	-88.02
2	6	-15.27	-102.90	-69.76	-103.63	3.64	-10.20	-3.61	-108.12
2	7	-17.46	-97.18	-66.21	-90.60	9.59	-65.41	-5.86	-127.23
2	8	-17.39	-90.48	-66.67	-140.90	13.21	-121.94	-8.59	-142.92
2	9	-16.63	-91.64	-66.58	-140.49	14.89	-173.34	-11.49	-155.45
2	10	-16.25	-97.89	-67.04	-155.99	15.65	141.31	-14.45	-167.89
2	11	-16.37	-103.76	-64.61	175.45	15.85	102.63	-18.12	-179.43
2	12	-16.71	-107.93	-65.01	-171.47	15.97	67.05	-22.97	170.53
2	13	-17.09	-111.39	-64.06	151.41	16.15	32.89	-30.44	174.52
2	14	-17.11	-110.96	-65.31	142.93	15.95	1.43	-34.60	-115.92
2	15	-16.84	-113.34	-64.26	156.24	15.97	-28.92	-27.80	-89.11
2	16	-16.78	-116.77	-61.83	107.47	15.84	-58.97	-24.72	-105.11
2	17	-16.51	-121.60	-72.17	144.18	15.65	-87.83	-22.65	-112.92
2	18	-16.82	-129.65	-69.62	130.95	15.55	-117.21	-20.65	-126.05
2	19	-18.61	-138.19	-64.20	168.06	15.28	-147.64	-19.63	-138.57
2	20	-21.50	-132.84	-60.17	135.42	14.89	-178.56	-18.58	-153.24
2	21	-22.46	-92.59	-60.24	126.24	13.93	151.11	-17.39	-164.66
2	22	-18.06	-74.29	-58.18	126.19	13.10	121.08	-16.21	-176.47

Typical On wafer Measurements

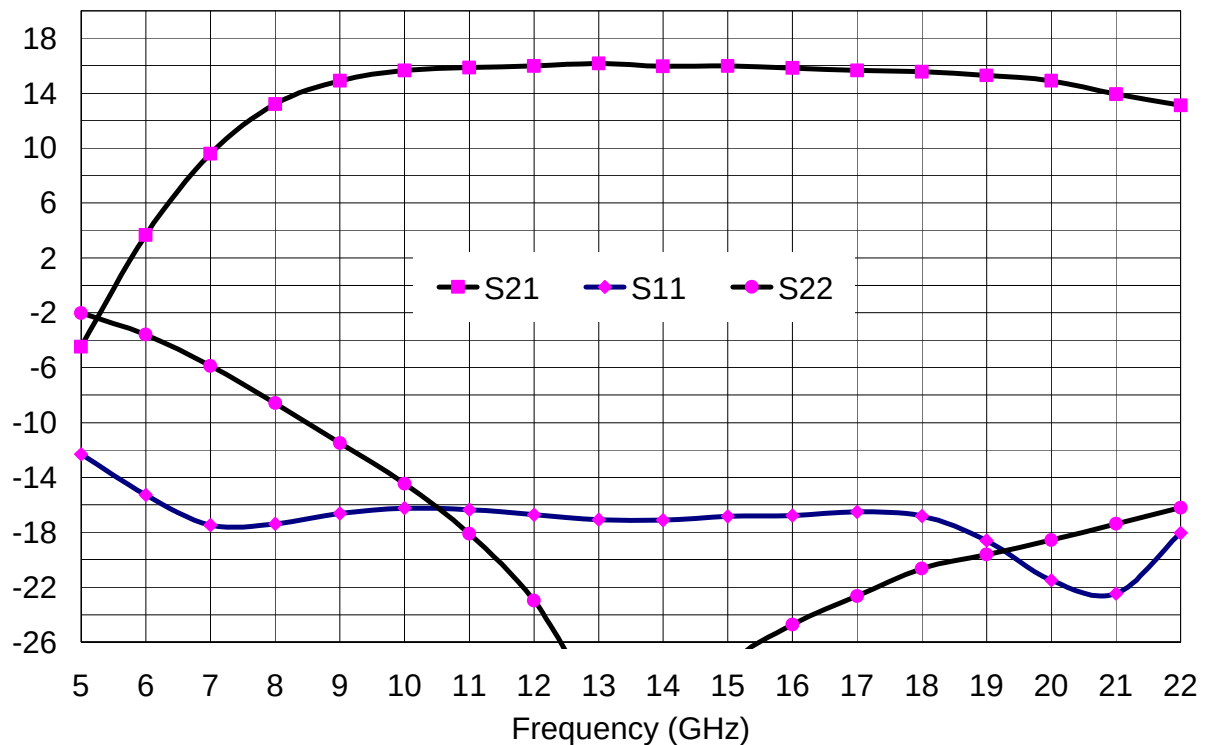
Bias Conditions : $V_d = 3.5$ Volt, V_g tuned for $I_d = 190$ mA.

Gain for each channel versus frequency (dB)**Isolation between channels versus frequency (dB)**

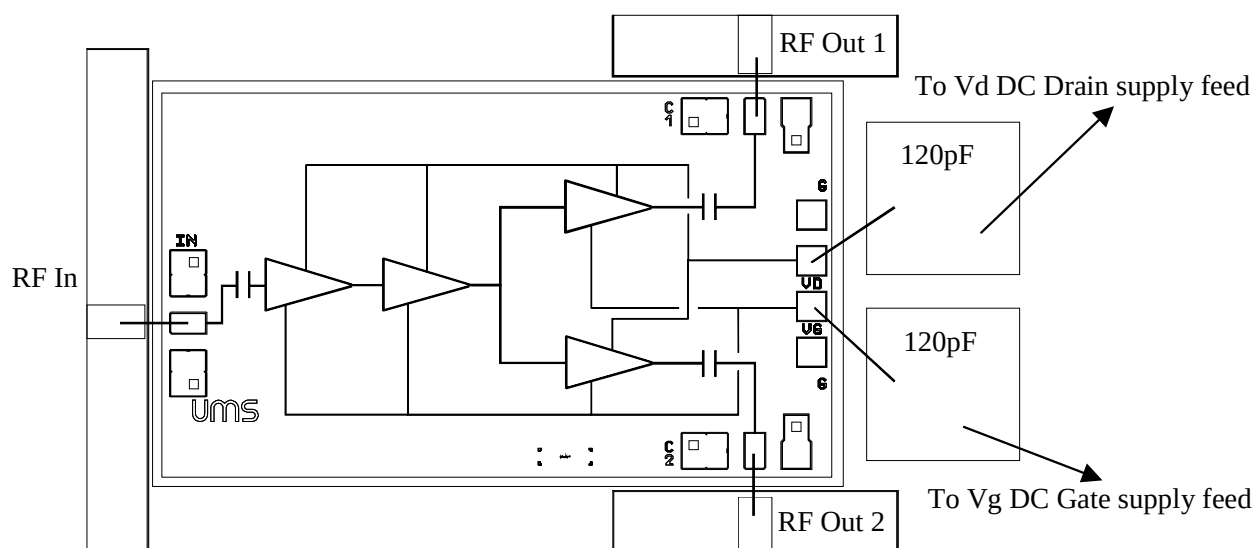
Gain & Return Loss channel 1 versus frequency (dB)



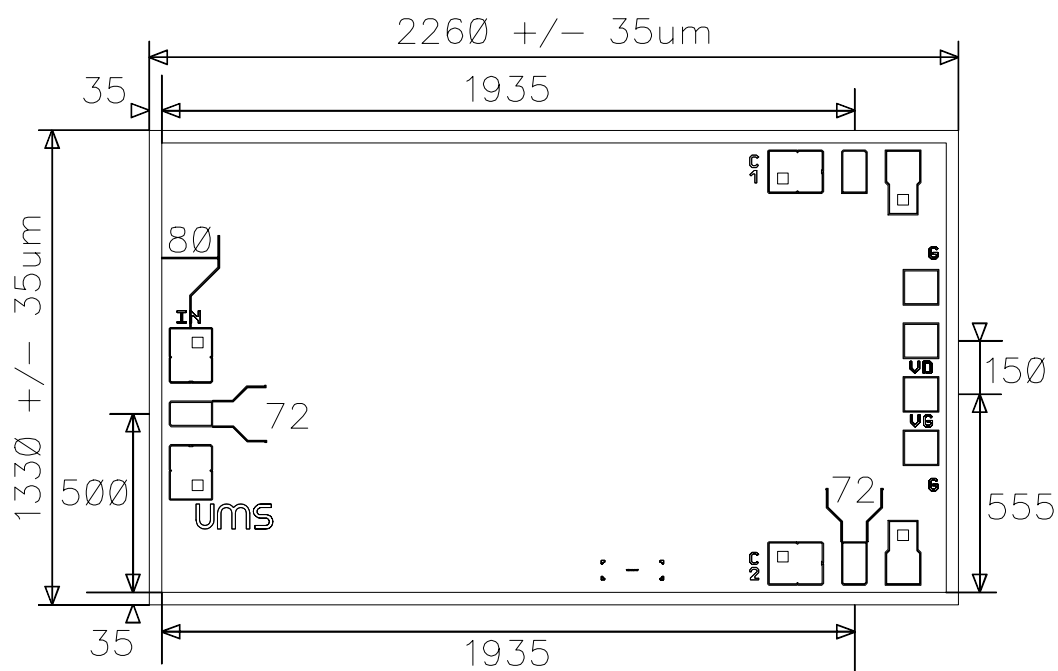
Gain & Return Loss channel 2 versus frequency (dB)



Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended.



Bonding pad positions.

(Chip thickness : 100µm. DC pads : 100*100 µm². All dimensions are in micrometers)

Ordering Information

Chip form : CHA2296-99F/00

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