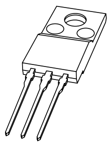


BT151X series

Thyristors

Rev. 04 — 9 June 2004 **Product data sheet**

1. Product profile

1.1 General description

Passivated thyristors in a SOT186A full pack plastic package.

1.2 Features

- High thermal cycling performance
- High bidirectional blocking voltage capability
- Isolated mounting base.

1.3 Applications

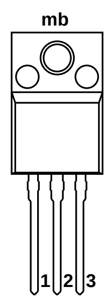
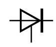
- Motor control
- Industrial and domestic lighting, heating and static switching.

1.4 Quick reference data

- V_{DRM}, V_{RRM} ≤ 800 V (BT151X-800)
- V_{DRM}, V_{RRM} ≤ 650 V (BT151X-650)
- V_{DRM}, V_{RRM} ≤ 500 V (BT151X-500)
- $I_{T(RMS)}$ ≤ 12 A
- $I_{T(AV)}$ ≤ 7.5 A
- I_{TSM} ≤ 120 A.

2. Pinning information

Table 1: Discrete pinning

Pin	Description	Simplified outline	Symbol
1	cathode (k)	 SOT186A (TO-220)	
2	anode (a)		
3	gate (g)		
mb	mounting base; isolated		

3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
BT151X-500	-	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 'full pack'	SOT186A
BT151X-650			
BT151X-800			

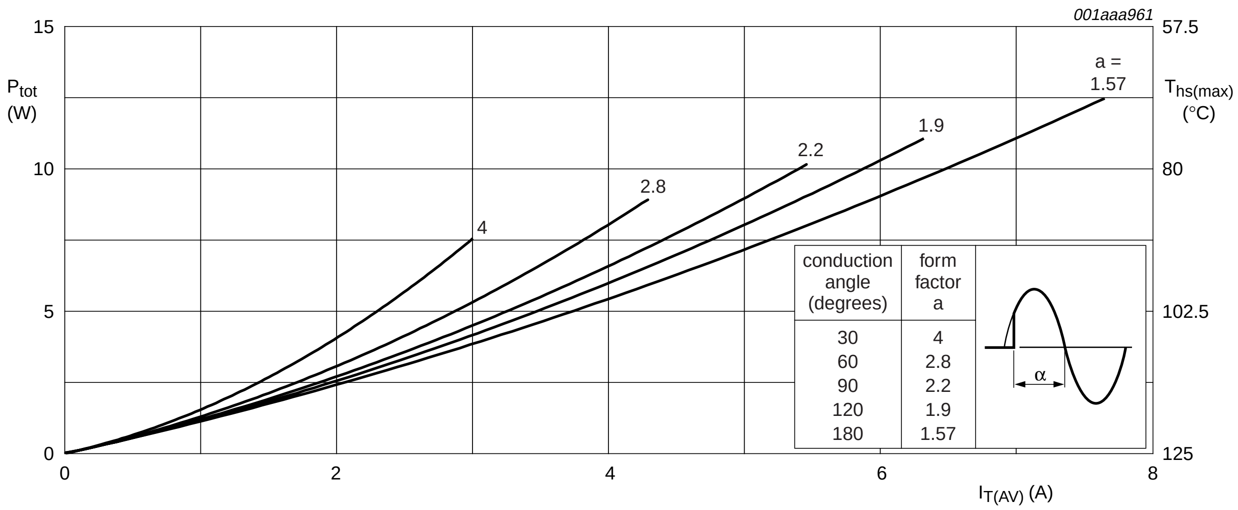
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

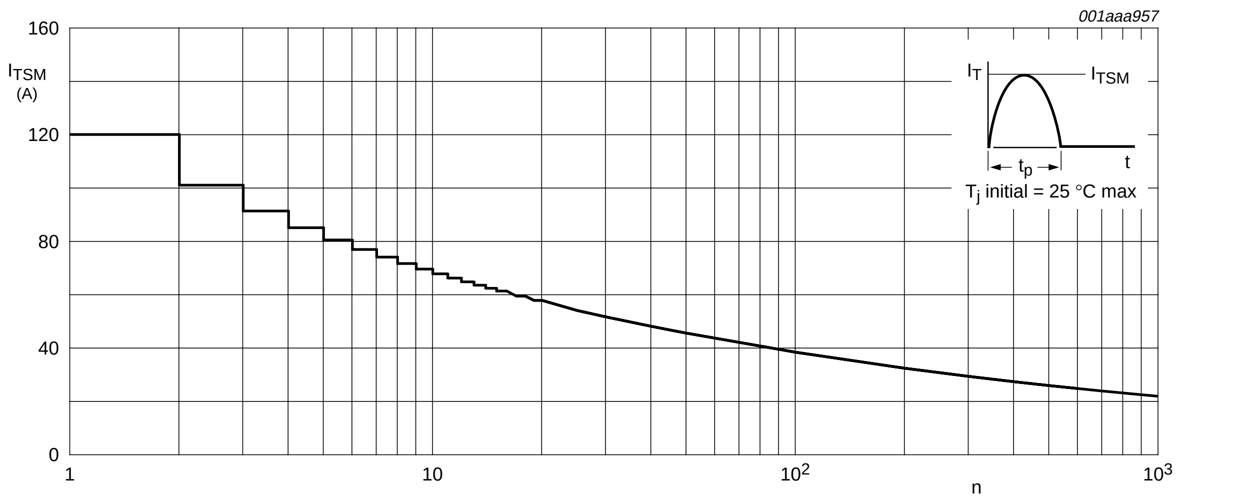
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}, V_{RRM}	repetitive peak off-state voltage				
	BT151X-500	[1]	-	500	V
	BT151X-650	[1]	-	650	V
	BT151X-800		-	800	V
$I_{T(AV)}$	average on-state current	half sinewave; $T_{hs} \leq 69$ °C; Figure 1	-	7.5	A
$I_{T(RMS)}$	RMS on-state current	all conduction angles; Figure 4 and Figure 5	-	12	A
I_{TSM}	non-repetitive peak on-state current	half sinewave; $T_j = 25$ °C prior to surge; Figure 2 and Figure 3			
		t = 10 ms	-	120	A
		t = 8.3 ms	-	132	A
I^2t	I^2t for fusing	t = 10 ms	-	72	A^2s
dI_T/dt	repetitive rate of rise of on-state current after triggering	$I_{TM} = 20$ A; $I_G = 50$ mA; dI_G/dt 50 mA/µs	-	50	A/µs
I_{GM}	peak gate current		-	2	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		–40	+150	°C
T_j	junction temperature		-	125	°C

[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/µs.



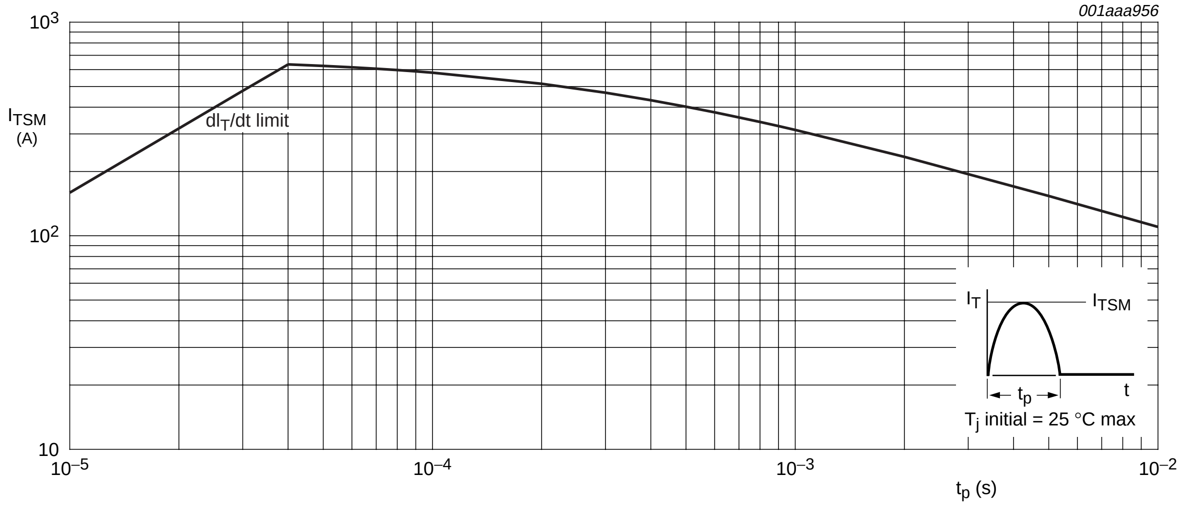
a = form factor = $I_{T(RMS)}/I_{T(AV)}$.

Fig 1. Total power dissipation as a function of average on-state current; maximum values.



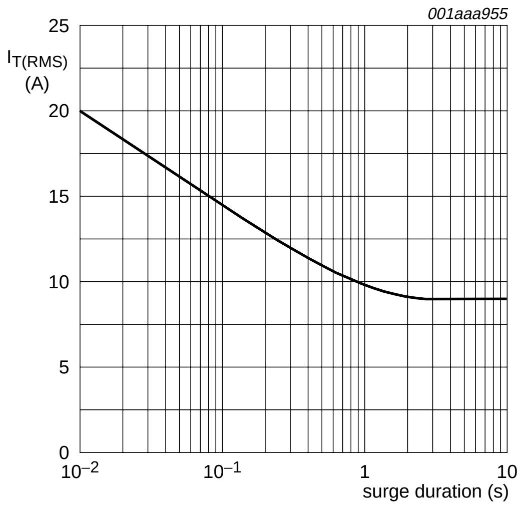
f = 50 Hz.

Fig 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values.



$t_p \leq 10$ ms.

Fig 3. Non-repetitive peak on-state current as a function of pulse width; maximum values.



f = 50 Hz; $T_{hs} \leq 87$ °C.

Fig 4. RMS on-state current as a function of surge duration; maximum values.

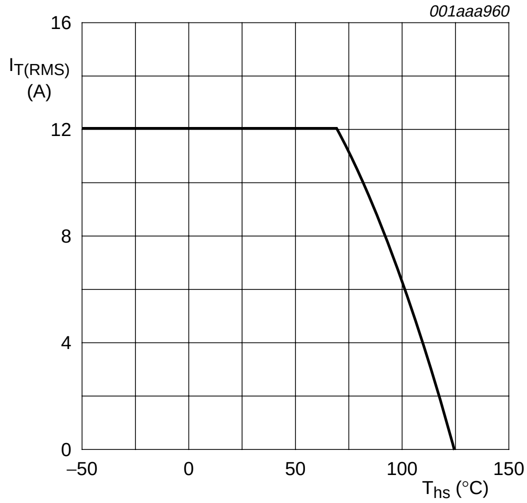
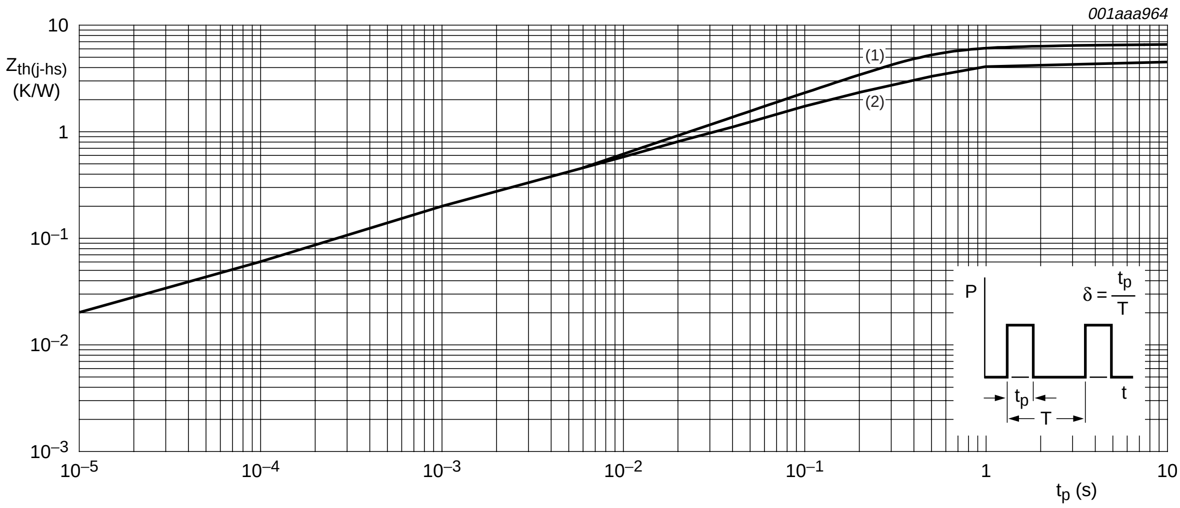


Fig 5. RMS on-state current as a function of heatsink temperature; maximum values.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-hs)}$	thermal resistance from junction to heatsink	Figure 6			
		with heatsink compound	-	4.5	K/W
		without heatsink compound	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	55	-	K/W



(1) Without heatsink compound.

(2) With heatsink compound.

Fig 6. Transient thermal impedance as a function of pulse width.

6. Isolation characteristics

Table 5: Isolation limiting values and characteristics

T_{hs} = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{isol}	RMS isolation voltage from all three terminals to external heatsink	f = 50 to 60 Hz; sinusoidal waveform; R.H. ≤ 65%; clean and dust free	-	2500	V
C_{isol}	capacitance from pin 2 to external heatsink	f = 1 MHz	10	-	pF

7. Characteristics

Table 6: Characteristics

T_j = 25 °C unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; Figure 8	-	2	15	mA
I_L	latching current	V_D = 12 V; I_{GT} = 0.1 A; Figure 10	-	10	40	mA
I_H	holding current	V_D = 12 V; I_{GT} = 0.1 A; Figure 11	-	7	20	mA
V_T	on-state voltage	I_T = 23 A; Figure 9	-	1.4	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; Figure 7	-	0.6	1.5	V
		$V_D = V_{DRM(max)}$; I_T = 0.1 A; T_j = 125 °C	0.25	0.4	-	V
I_D, I_R	off-state leakage current	$V_D = V_{DRM(max)}$; $V_R = V_{RRM(max)}$; T_j = 125 °C	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; Figure 12				
		gate open circuit	50	130	-	V/µs
		R_{GK} = 100 Ω	200	1000	-	V/µs
t_{gt}	gate controlled turn-on time	I_{TM} = 40 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs
t_q	circuit commuted turn-on time	V_D = 67% $V_{DRM(max)}$; T_j = 125 °C; I_{TM} = 20 A; V_R = 25 V; dI_{TM}/dt = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω	-	70	-	µs

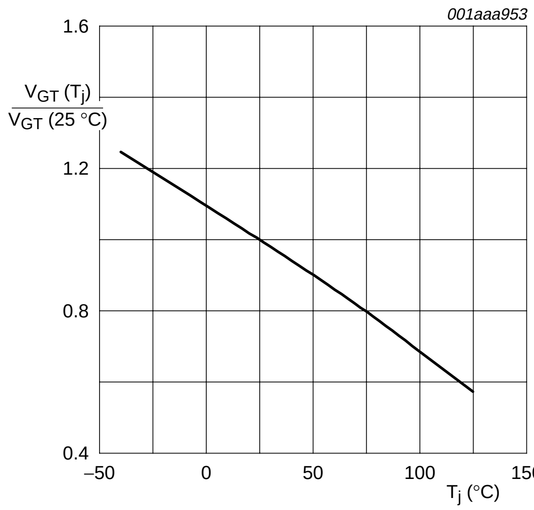


Fig 7. Normalized gate trigger voltage as a function of junction temperature.

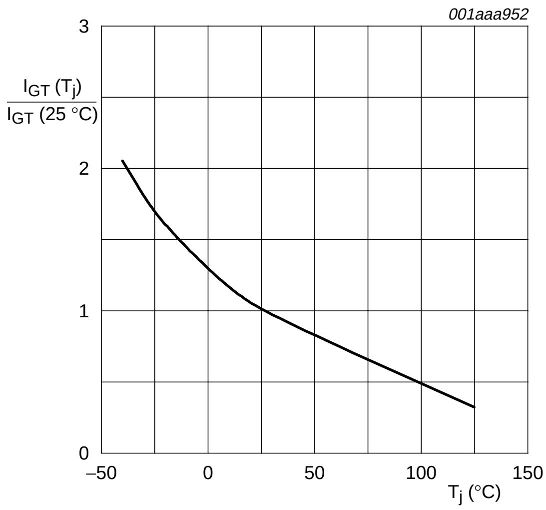
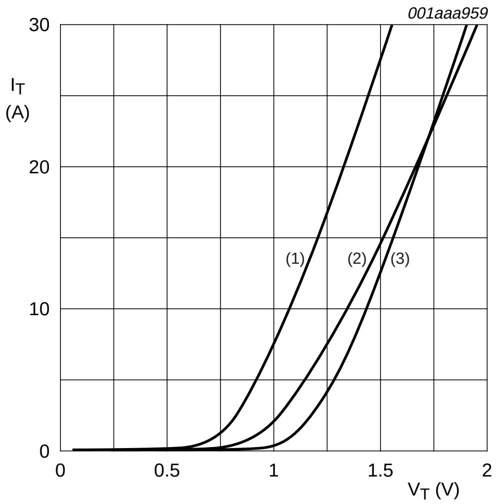


Fig 8. Normalized gate trigger current as a function of junction temperature.



V_O = 1.06 V.

R_S = 0.0304 Ω.

(1) T_j = 125 °C; typical values.

(2) T_j = 125 °C; maximum values.

(3) T_j = 25 °C; maximum values.

Fig 9. On-state current characteristics.

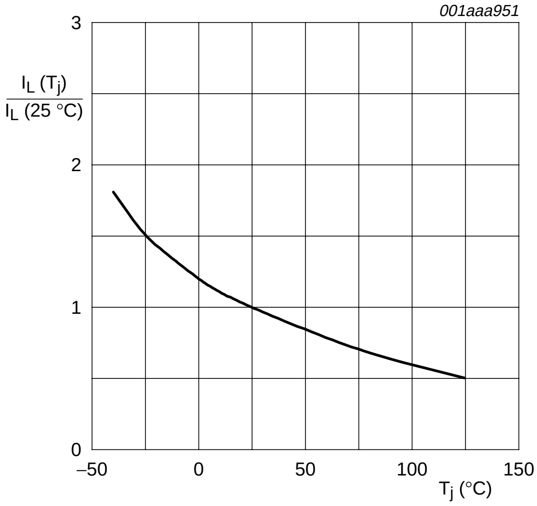


Fig 10. Normalized latching current as a function of junction temperature.

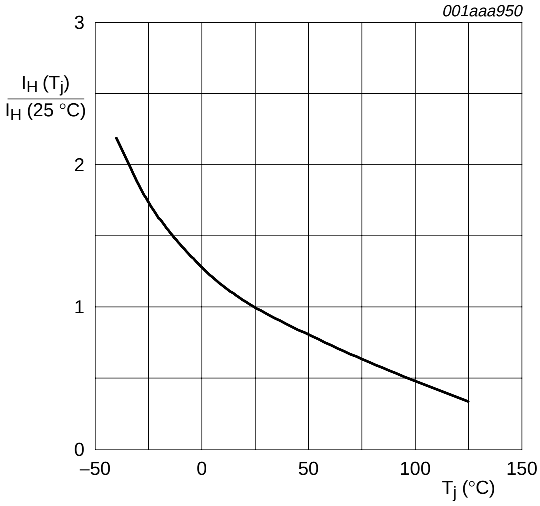
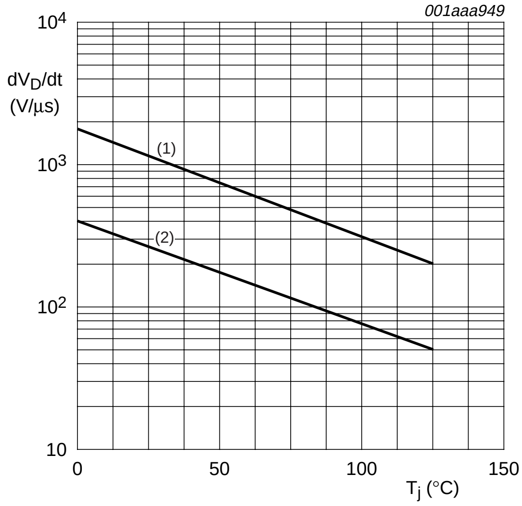


Fig 11. Normalized holding current as a function of junction temperature.



(1) R_{GK} = 100 Ω.

(2) Gate open circuit.

Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values.

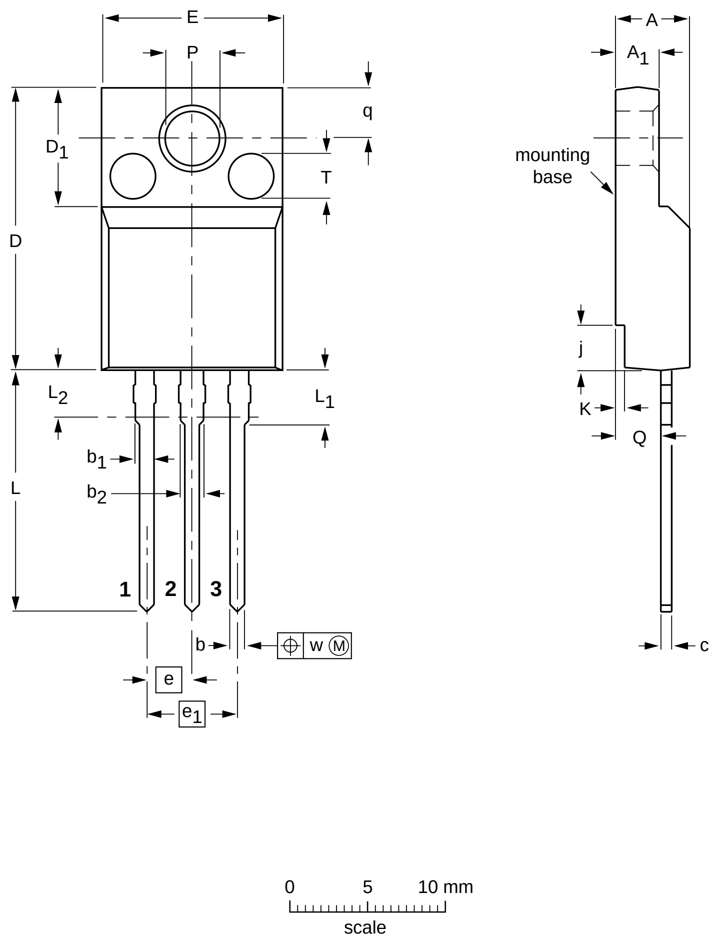
8. Package information

Epoxy meets requirements of UL94 V-0 at ⅛ inch.

9. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 'full pack'

SOT186A



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2(1) max.	P	Q	q	T(2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.0	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 1.7	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3-lead TO-220F				~~02-03-12~~ 02-04-09

Fig 13. Package outline.

10. Revision history

Table 7: Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
BT151X_SERIES_4	20040609	Product specification	-	9397 750 13162	BT151X_SERIES_3
Modifications:	• The format of this specification has be redesigned to comply with Philips Semiconductors' new presentation and information standard				
BT151X_SERIES_3	20030901	Product specification	-	-	BT151X_SERIES_2
BT151X_SERIES_2	19990601	Product specification	-	-	BT151X_SERIES_1
BT151X_SERIES_1	19970901	Product specification	-	-	-

11. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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15. Contents

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