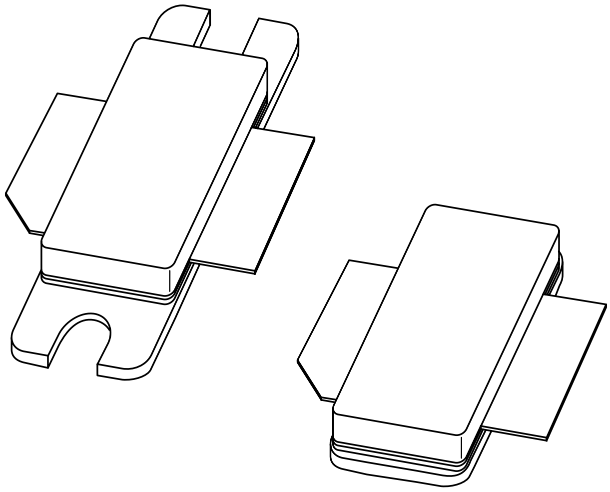
DATA SHEET



BLF900-110; BLF900S-110
Base station LDMOS transistors

Product specification
Supersedes data of 2003 Sep 22

2004 Feb 04

Philips Semiconductors

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FEATURES

- Typical CDMA IS95 performance at standard settings with a supply voltage of 27 V, frequency of 881.5 MHz and I_{DQ} of 700 mA; adjacent channel bandwidth is 30 kHz, adjacent channel at ± 750 kHz:
  - Output power = 24 W (AV)
  - Gain = 15 dB
  - Efficiency = 27%
  - ACPR = –45 dBc at 750 kHz and BW = 30 kHz.
- 110 W CW performance
- Easy power control
- Excellent ruggedness
- High power gain
- Excellent thermal stability
- Designed for broadband operation (800 to 1000 MHz)
- Internally matched for ease of use.

APPLICATIONS

- RF power amplifier for GSM, EDGE and CDMA base stations and multicarrier operations in the 800 to 1000 MHz frequency range.

DESCRIPTION

110 W LDMOS power transistor for base station applications at frequencies from 800 to 1000 MHz.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange

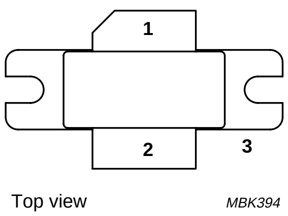
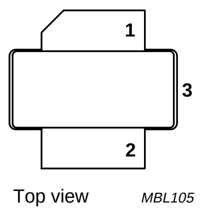


Fig.1 Simplified outline SOT502A (BLF900-110).

PINNING - SOT502B

PIN	DESCRIPTION
1	drain
2	gate
3	source; connected to flange



Leads are gold-plated.

Fig.2 Simplified outline SOT502B (BLF900S-110).

QUICK REFERENCE DATA

Typical RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_3 (dBc)	ACPR 750 (dBc)
2-tone, class-AB	f_1 = 890.0; f_2 = 890.1	27	100 (PEP)	17	38	–33	–
CDMA (IS95)	881.5	27	24 (AV)	15	27	–	–45

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BLF900-110	–	Flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF900S-110	–	Earless flanged LDMOST ceramic package; 2 leads	SOT502B

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	75	V
V_{GS}	gate-source voltage	–	±15	V
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	T_h = 25 °C, P_L = 160 W (AV), note 1	0.9	K/W

Note

1. Thermal resistance is determined under specified RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 3 mA	75	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 250 mA	4.5	–	5.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	3	μA
I_{DSX}	on-state drain current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	31	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	0.5	μA
g_{fs}	forward transconductance	V_{DS} = 20 V; I_D = 7.5 A	–	7	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 9 A	–	90	–	mΩ

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. V_{DS} = 27 V; f = 890 MHz; T_h = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Mode of operation: 2-tone CW, 100 kHz spacing, I_{DQ} = 700 mA						
G_p	power gain	P_L = 100 W (PEP)	16	17 (1)	–	dB
η_D	drain efficiency		35	38	–	%
IRL	input return loss		–	–9	<–6	dB
d_3	third order intermodulation distortion		–	–33	–27	dBc
	ruggedness	VSWR = 10 : 1 through all phases; P_L = 125 W (PEP)	no degradation in output power			
Mode of operation: CDMA, IS95 (pilot, paging, sync and traffic codes 8 to 13), I_{DQ} = 575 mA						
G_p	power gain	P_L = 24 W (AV)	–	15	–	dB
η_D	drain efficiency	P_L = 24 W (AV)	–	27	–	%
ACPR 750	adjacent channel power ratio	at BW = 30 kHz	–	–45	–	dBc

Note

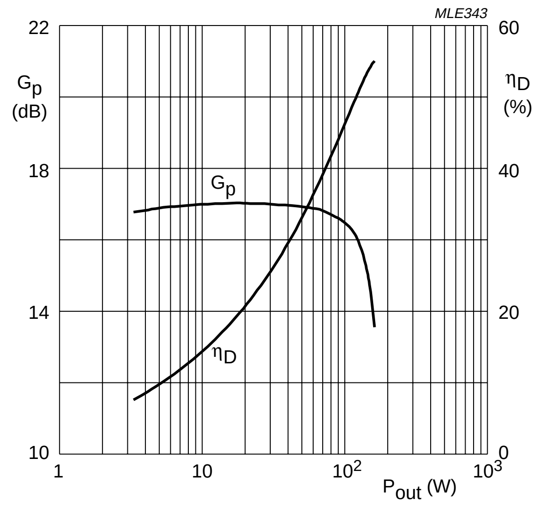
1. Refer to RF Gain grouping table.

RF Gain grouping

CODE(1)	GAIN(2) (dB)	
	MIN.	MAX.
B	16.0	16.5
C	16.5	17.0
D	17.0	17.5
E	17.5	18.0

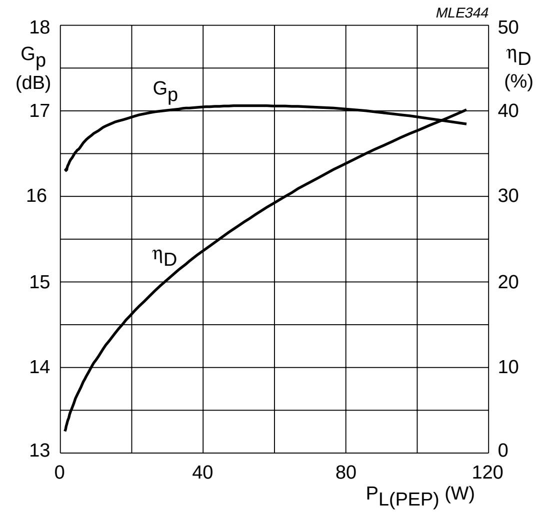
Notes

1. 0.2 dB overlap is allowed for measurement repeatability.
2. For 2-tone at f_1 = 890 MHz; f_2 = 890.1 MHz.



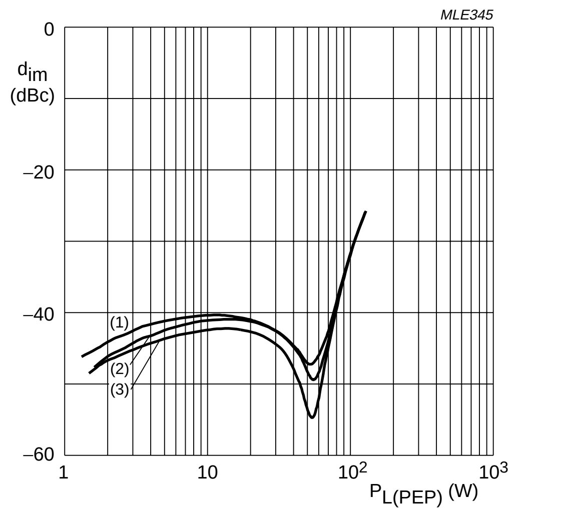
V_{DS} = 27 V; I_{DQ} = 700 mA; f = 890 MHz.

Fig.3 Power gain and efficiency as functions of load power; typical values.



V_{DS} = 27 V; I_{DQ} = 700 mA; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

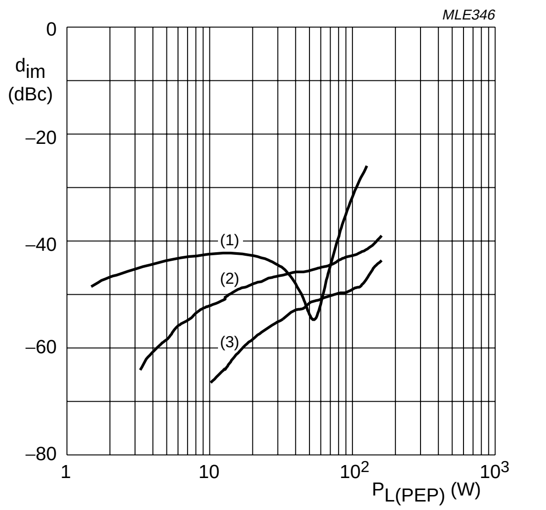
Fig.4 Power gain and efficiency as functions of peak envelope load power; typical values.



V_{DS} = 27 V; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

(1) I_{DQ} = 600 mA. (2) I_{DQ} = 800 mA. (3) I_{DQ} = 700 mA.

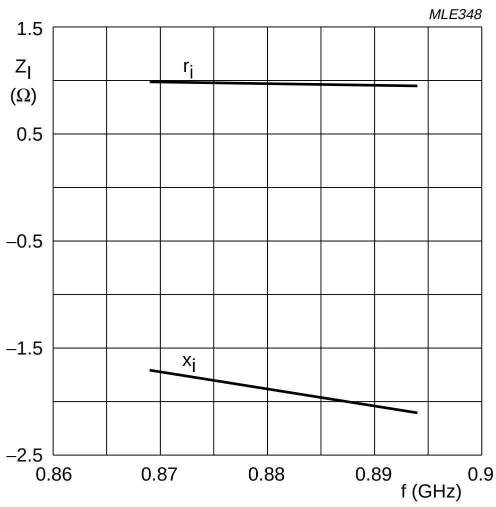
Fig.5 Third order intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 27 V; I_{DQ} = 700 mA; f_1 = 890.0 MHz; f_2 = 890.1 MHz.

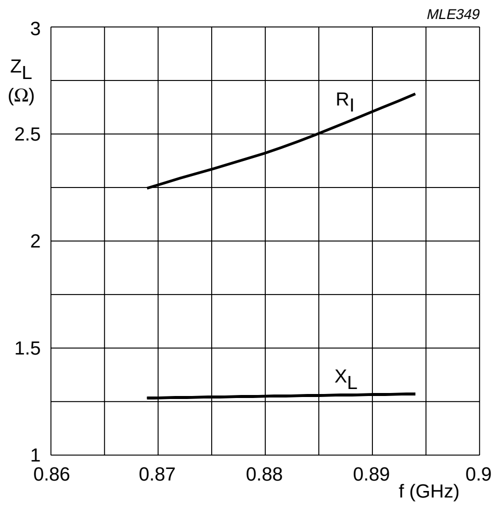
(1) d_3. (2) d_5. (3) d_7.

Fig.6 Third order intermodulation distortion as a function of peak envelope load power; typical values.



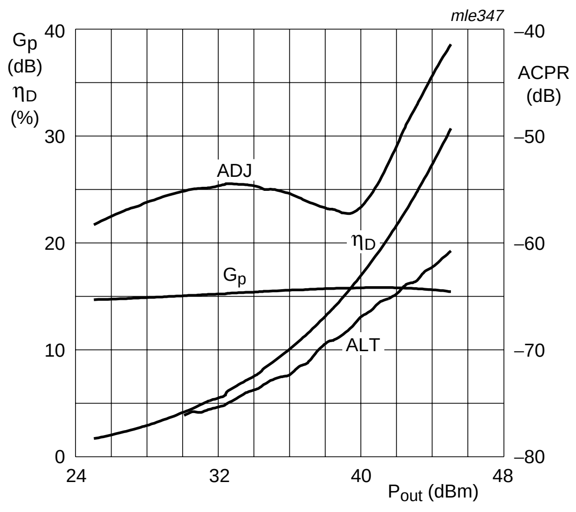
Class-AB operation; V_{DS} = 27 V; I_{DQ} = 700 mA; P_L = 100 W.
Values comprised for different parameters.

Fig.7 Input impedance as a function of frequency (series components); typical values.



Class-AB operation; V_{DS} = 27 V; I_{DQ} = 700 mA; P_L = 100 W.
Values comprised for different parameters.

Fig.8 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 27 V;I_{DQ} = 575 mA; f = 881.5 MHz.
Test signal: Single carrier IS-97 CDMA with PAR = 9.5 dB at 0.01 %
(pilot, paging, sync, 6 traffic channels with Walsh codes 8-13).
ADJ at 750 kHz offset in 30 kHz BW;
ALT at 1.98 MHz offset in 30 kHz BW.

Fig.9 Single carrier CDMA performance as a function of output power.

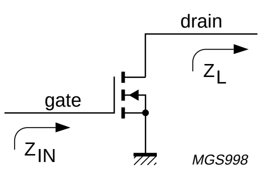


Fig.10 Definition of transistor impedance.

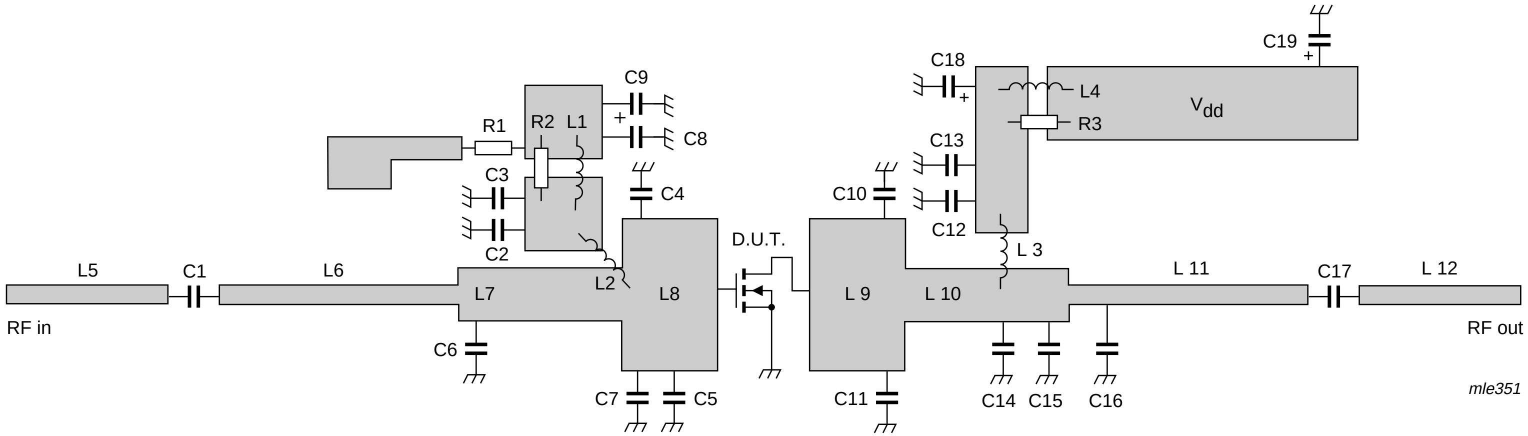
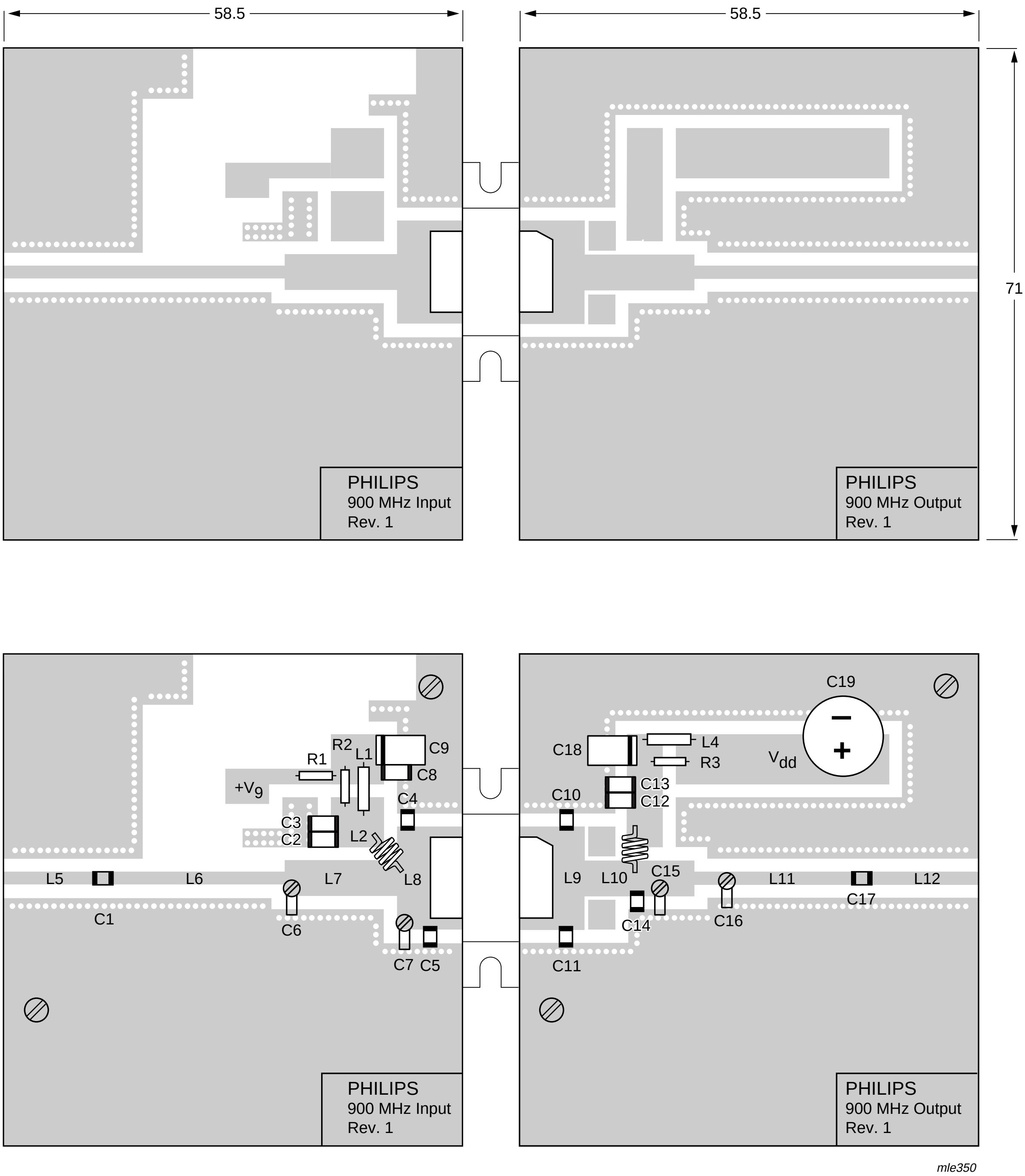


Fig.11 Test circuit for 860 to 900 MHz operation.



Dimensions in mm.

The components are situated on one side of the copper-clad Ultralam 2000 printed-circuit board (ε_r = 2.5); thickness = 31 mm.
The other side is unetched and serves as a ground plane.

Fig.12 Component layout for 860 to 900 MHz test circuit.

List of components (see Figs 11 and 12)

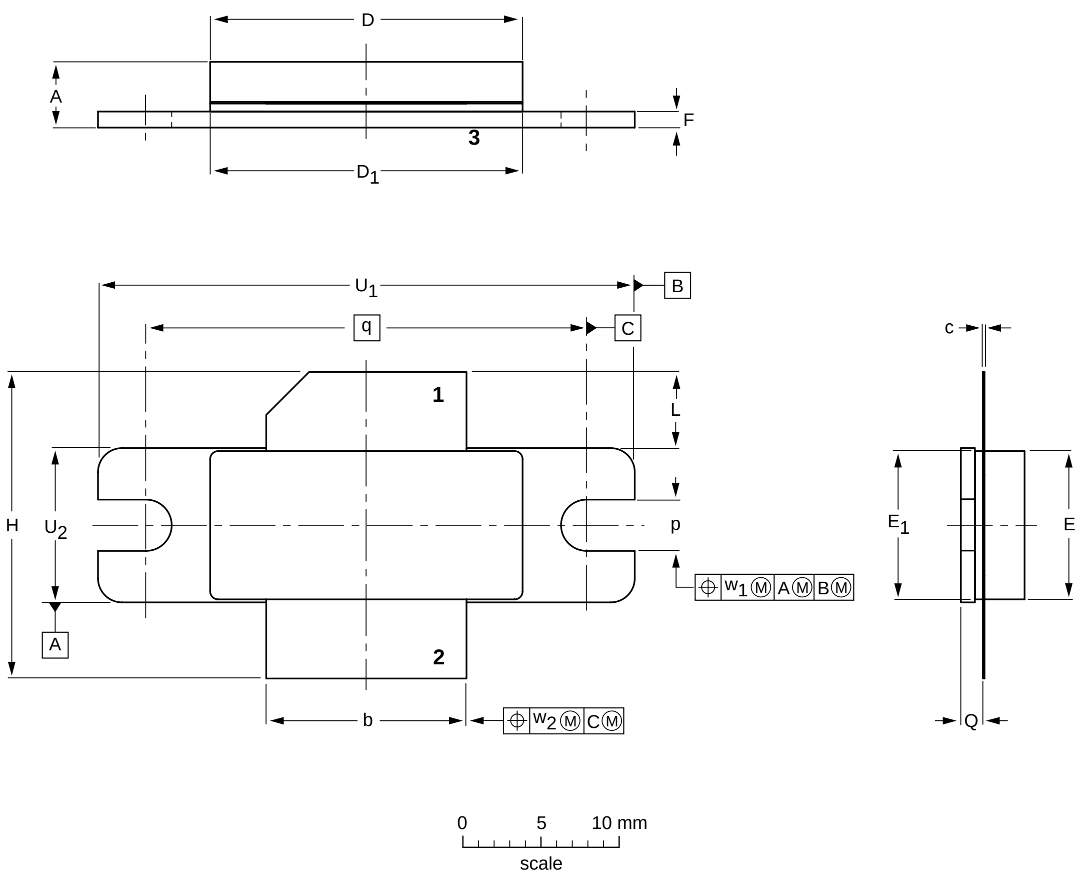
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS
C1	multilayer ceramic chip capacitor; note 1	30 pF	
C2, C12	multilayer ceramic chip capacitor; note 1	47 pF	
C3, C13	multilayer ceramic chip capacitor; note 1	300 pF	
C4	multilayer ceramic chip capacitor; note 1	10 pF	
C5	multilayer ceramic chip capacitor; note 1	3 pF	
C6, C7, C15	trimmer capacitors (Tekelec); note 2	0.8 to 8 pF	
C8	multilayer ceramic chip capacitor; note 1	20 nF	
C9	tantalum capacitor	10 μF; 35 V	
C10, C11	multilayer ceramic chip capacitor; note 1	13 pF	
C14	multilayer ceramic chip capacitor; note 1	8.2 pF	
C16	trimmer capacitor	0.5 to 4.5 pF	
C17	multilayer ceramic chip capacitor; note 1	56 pF	
C18	tantalum capacitor; low ESR	10 μF; 35 V	
C19	electrolytic capacitor	220 μF; 40 V	
L1	ferrite bead (long)	grade 4S2	
L2	3 turn ind. copper wire		1 mm; int dia = 4.5 mm
L3	4 turn ind. copper wire		1 mm; int dia = 3 mm
L4	ferrite bead (short)	grade 4S2	
L5	stripline; note 3	$Z_0 = 50\ \Omega$	2 x 17.2 mm
L6	stripline; note 3	$Z_0 = 50\ \Omega$	2 x 25.4 mm
L7	stripline; note 3	$Z_0 = 50\ \Omega$	5.6 x 17.4 mm
L8	stripline; note 3	$Z_0 = 50\ \Omega$	16 x 10.2 mm
L9	stripline; note 3	$Z_0 = 10\ \Omega$	16 x 10.2 mm
L10	stripline; note 3	$Z_0 = 25\ \Omega$	5.6 x 17.4 mm
L11	stripline; note 3	$Z_0 = 50\ \Omega$	2 x 25.4 mm
L12	stripline; note 3	$Z_0 = 50\ \Omega$	2 x 17.2 mm
R1	SMD resistor	8.2 Ω, 0.1 W	
R2	SMD resistor	4.7 Ω, 0.1 W	
R3	metal film resistor	10 Ω, 0.6 W	

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. Mounted flat.
3. Striplines are on a double copper-clad Ultralam 2000 printed-circuit board ($\varepsilon_r = 2.5$); thickness = 0.31 mm.

PACKAGE OUTLINES

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**

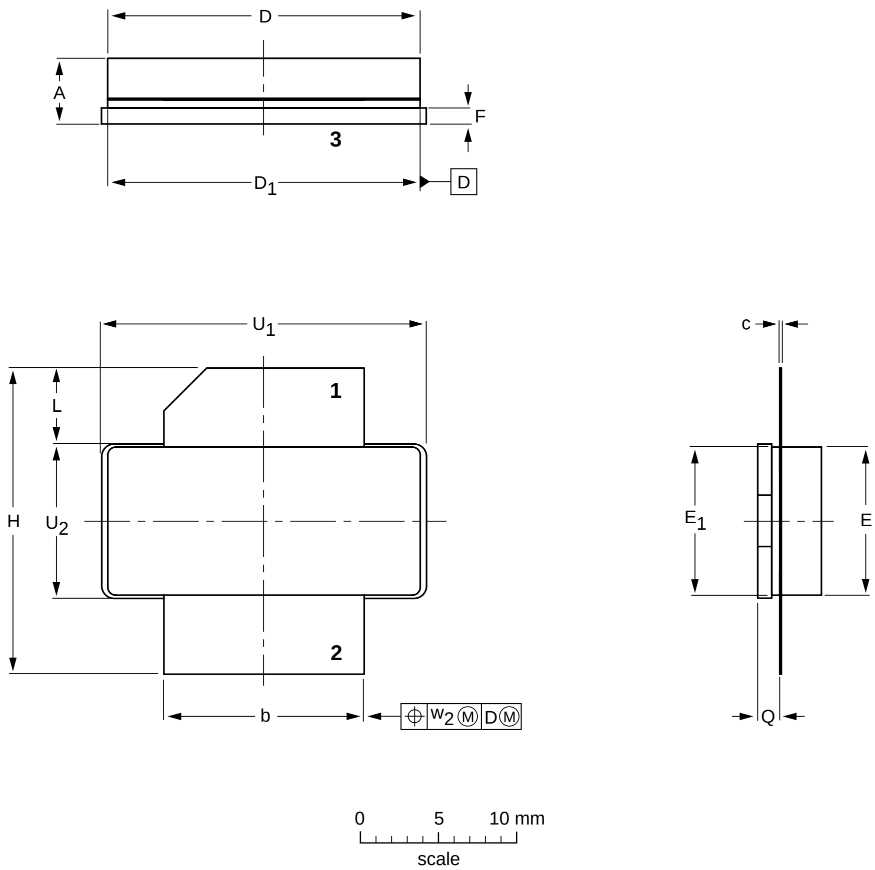


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~99-12-28~~ 03-01-10

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
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