Features

- **Advanced RISC Architecture, 130 Powerful Instructions, Most Single Clock Cycle Execution**
- **JTAG (IEEE Std. 1149.1 Compliant) Interface**
  - **Boundary-scan Capabilities According to the JTAG Standard**
  - **Extensive On-chip Debug Support**
- **Clock Generator Provides CPU Rates up to 48MHz**
- **Only One External Clock Crystal of 12 MHz Can Generate All the Required System Clocks:**
  - **Internal Clock for Standard UART Rates**
  - **A 48 MHz and 96 MHz Clock for USB Data Recovery**
  - **AVR Processor and System Clock**
  - **Full-speed USB Interface (12 Mbits per Second) 2.0 Compliant**
- **Two On-chip 16550 UARTs Supporting Baud Rates up to 921 Kbaud**
  - **Both UARTs Incorporate individual Transmit and Receive FIFOs of 16 Bytes**
  - **UART0 Supports Modem Control Signals**
  - **Programmable SPI Interface**
- **On-chip Bootstrap ROM Provides a Variety of Firmware Upgrade Modes**
  - **Device Firmware Upgrade Through USB for the internal Program SRAM (No External Non-volatile SPI Memory Required)**
  - **Device Firmware Upgrade Through USB for both the Internal Program SRAM and the External SPI DataFlash® or EEPROM**
  - **SPI Program Mode from the External DataFlash or EEPROM**
- **DMA Channels Allow Fast Data Transfers between Endpoint Buffers and Internal or External SRAM (DMA Transfer Rate is 12 MHz for All Channels)**
- **8K x 16 bits (up to 11K x 16 bits), In-System SRAM for Program Code (Program Memory)**
- **On-Chip 8 Kbytes SRAM for Data and Variables (2, 4, and 8 Kbytes can be Remapped for Program Storage in the Address Area Above the Program Memory)**
- **Two 8-bit Timer/Counters**
- **One 16-bit Timer/Counter**
- **Two External interrupts Through GPIOs**
- **Programmable Watchdog Timer**
- **Low voltage operation:**
  - **1.8V for the Core**
  - **1.8V or 3.3V for the Periphery**
  - **3.3V for the USB**
- **Low cost 64-pin TQFP Package, Suitable for USB-to-UART Bridge Applications**

High-speed (48 MHz) AVR®- based Bridging Device

AT76C712 Summary

Overview

Atmel's AT76C712 is a low-power USB peripheral that can connect various types of devices to a common USB port.

- The device is based on the AVR-enhanced RISC architecture core, which combines an advanced instruction set with 32 general-purpose working registers. By executing powerful instructions in a single clock cycle, the AT76C712 achieves throughputs approaching 1MIPS per MHz, allowing the system designer to optimize power consumption versus processing speed

- The clock generation circuit requires a clock input of 12 MHz and provides standard clock rates for the USB module and the on-chip UARTs, as well as several AVR CPU rates varying from 16 MHz up to 48 MHz

- Internal DMA channels allow fast data transfers between the USB buffers and the external and on-chip memory without processor interruption. USB DMA transfers use devoted data paths with a 12 Mbytes transfer rate

- An on-chip flexible memory controller allows dynamic memory mapping and provides the required timing for interfacing with slow or fast external memory devices, like SRAM or FIFOs

- Twenty-five multipurpose I/O pins provide the signals for the external interfaces. The device also offers two external interrupts, a programmable Watchdog Timer, flexible timer/counters with compare modes, and the support of various power-down modes

- On power-up, the bootstrap code is executed from the boot ROM. The purpose of the bootstrap code is to load the application code into the program memory. The application code is executed from the on-chip SRAM program memory contributing to the low-power consumption. Different programming modes are supported depending on the application (that is, the mode is selected externally by the PMODE0 and PMODE1 pins)

- In the slave programming mode, an external system (that is, the Host), operating as SPI master, can transfer the program image in a raw format to the program memory of the device. In this case, the device operates as an SPI slave and starts running from the internal boot ROM code, which switches to the start of program memory when it detects the end of a valid program transfer from the Host to the AT76C712 (see the "Slave Programmming Mode" on page 9)

- In a master programming mode, the AT76C712 reads the whole program image from an external SPI EEPROM or DataFlash and switches to the start of program memory when it completes the reading (see the "Master Programming Modes" on page 10). Alternatively, the AT76C712 reads only configuration parameters from a small serial non-volatile memory (EEPROM or DataFlash), enables the USB Controller, and executes the USB Device Firmware Upgrade (DFU) code that is stored in the boot ROM

- The USB Controller consists of a Serial Interface Engine (SIE), a Function Interface Unit (FIU), and a System Interface (SI). The SIE performs bit processing, line coding, packet generation and packet type recognition, serial-parallel data conversion, and packet delineation. The FIU consists of a protocol engine and a USB device with one Control Endpoint (EP0) and seven programmable Endpoints with up to 512 bytes maximum total size. All Endpoints support double buffering in order to provide the maximum performance specified for the USB

- The device supports two 16550 UART modules with 16 bytes FIFOs in each direction. UART0 serial interface provides full modem control functionality with the RTS/CTS, DTR/DSR, RI, and CD signals. These signals are provided by the general-purpose I/O pins of PORTD

• The AT76C712 AVR is supported with a full suite of program and system development tools including: C compiler, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits

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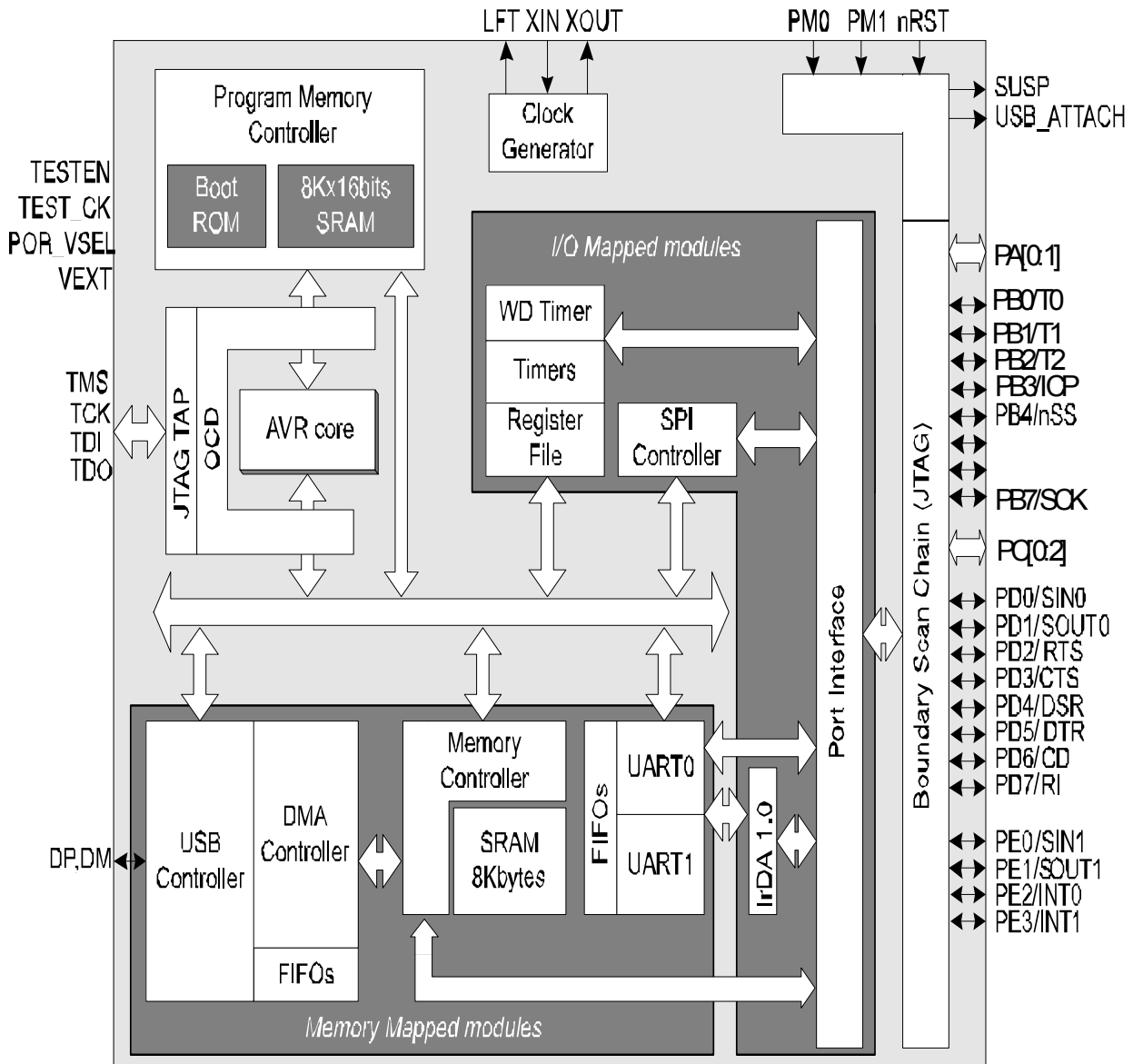
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