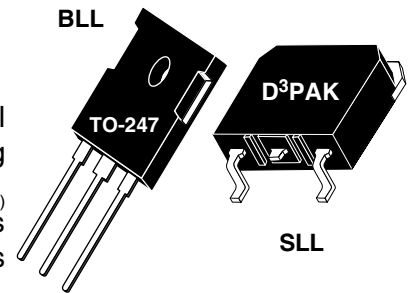
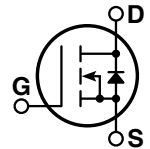


## POWER MOS 7® MOSFET

Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering  $R_{DS(ON)}$  and  $Q_g$ . Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge,  $Q_g$
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D<sup>3</sup>PAK Package




### MAXIMUM RATINGS

All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT6029BFL_SFL	UNIT
$V_{DSS}$	Drain-Source Voltage	600	Volts
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	21	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	84	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 30$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 40$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	300	Watts
	Linear Derating Factor	2.40	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	21	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	30	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	1210	

### STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	600			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 10V, I_D = 10.5A$ )			0.290	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = 600V, V_{GS} = 0V$ )			100	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 480V, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			500	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1mA$ )	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT6029BLL\_SLL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1 MHz		2615		pF
C <sub>oss</sub>	Output Capacitance			420		
C <sub>rss</sub>	Reverse Transfer Capacitance			47		
Q <sub>g</sub>	Total Gate Charge ③	V <sub>GS</sub> = 10V V <sub>DD</sub> = 300V I <sub>D</sub> = 21A @ 25°C		65		nC
Q <sub>gs</sub>	Gate-Source Charge			13		
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge			36		
t <sub>d(on)</sub>	Turn-on Delay Time	RESISTIVE SWITCHING V <sub>GS</sub> = 15V V <sub>DD</sub> = 300V I <sub>D</sub> = 21A @ 25°C R <sub>G</sub> = 1.6Ω		9		ns
t <sub>r</sub>	Rise Time			5		
t <sub>d(off)</sub>	Turn-off Delay Time			23		
t <sub>f</sub>	Fall Time			4		
E <sub>on</sub>	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 25°C V <sub>DD</sub> = 400V, V <sub>GS</sub> = 15V I <sub>D</sub> = 21A, R <sub>G</sub> = 5Ω		225		μJ
E <sub>off</sub>	Turn-off Switching Energy			90		
E <sub>on</sub>	Turn-on Switching Energy ⑥	INDUCTIVE SWITCHING @ 125°C V <sub>DD</sub> = 400V, V <sub>GS</sub> = 15V I <sub>D</sub> = 21A, R <sub>G</sub> = 5Ω		360		
E <sub>off</sub>	Turn-off Switching Energy			110		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Continuous Source Current (Body Diode)			21	Amps
I <sub>SM</sub>	Pulsed Source Current ① (Body Diode)			84	
V <sub>SD</sub>	Diode Forward Voltage ② (V <sub>GS</sub> = 0V, I <sub>S</sub> = -21A)			1.3	Volts
t <sub>rr</sub>	Reverse Recovery Time (I <sub>S</sub> = -21A, di <sub>S</sub> /dt = 100A/μs)		580		ns
Q <sub>rr</sub>	Reverse Recovery Charge (I <sub>S</sub> = -21A, di <sub>S</sub> /dt = 100A/μs)		7.92		μC
dv/dt	Peak Diode Recovery dv/dt ⑤			8	V/ns

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction to Case			0.42	°C/W
R <sub>θJA</sub>	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T<sub>J</sub> = +25°C, L = 5.49mH, R<sub>G</sub> = 25Ω, Peak I<sub>L</sub> = 21A

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I<sub>S</sub> ≤ -I<sub>D</sub>21A di/dt ≤ 700A/μs V<sub>R</sub> ≤ V<sub>DSS</sub> T<sub>J</sub> ≤ 150°C

⑥ Eon includes diode reverse recovery. See figures 18, 20.

APT Reserves the right to change, without notice, the specifications and information contained herein.

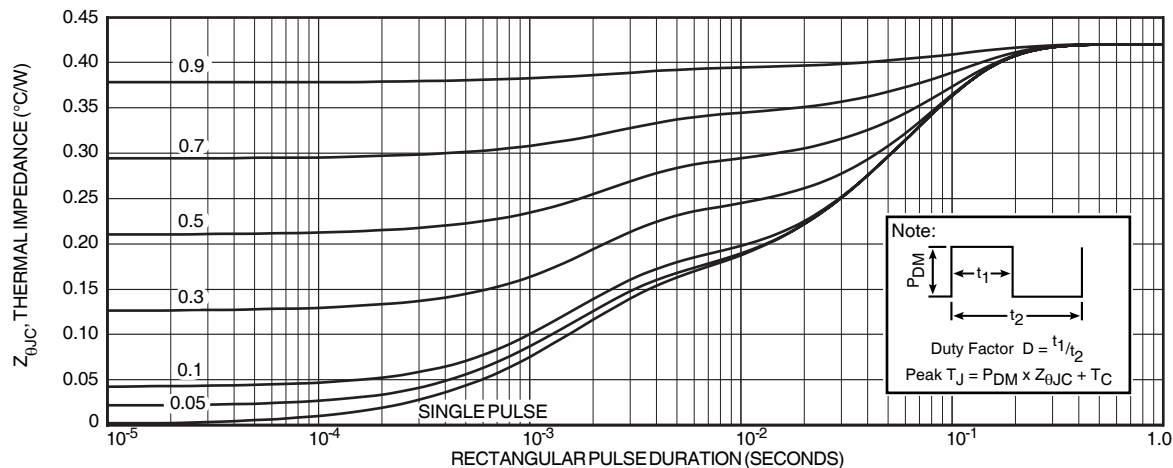


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

# Typical Performance Curves

APT6029BLL\_SLL

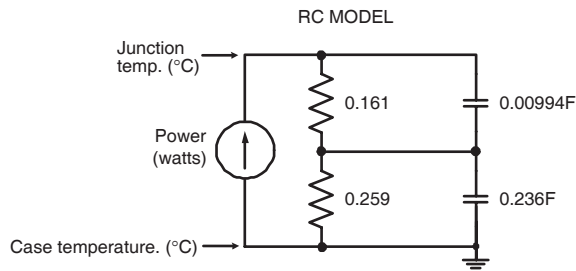


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

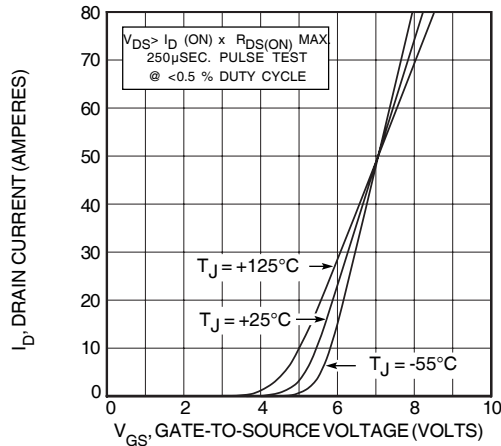


FIGURE 4, TRANSFER CHARACTERISTICS

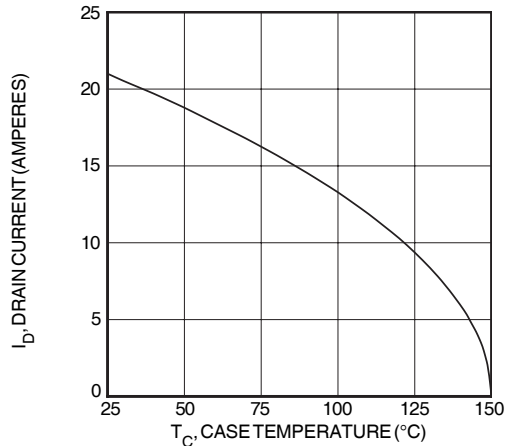


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

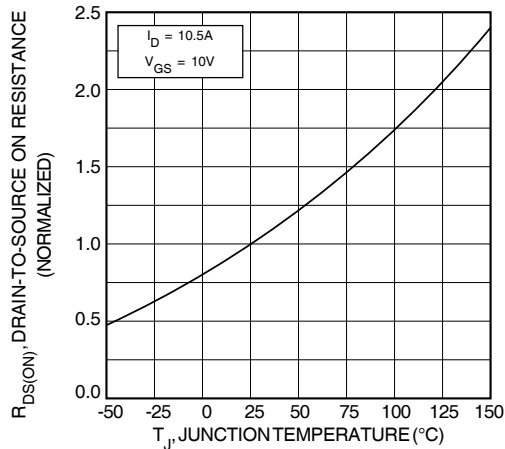


FIGURE 8,  $R_{DS(ON)}$  vs. TEMPERATURE

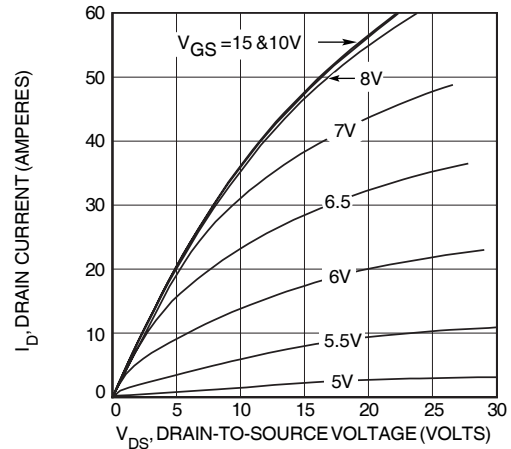


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

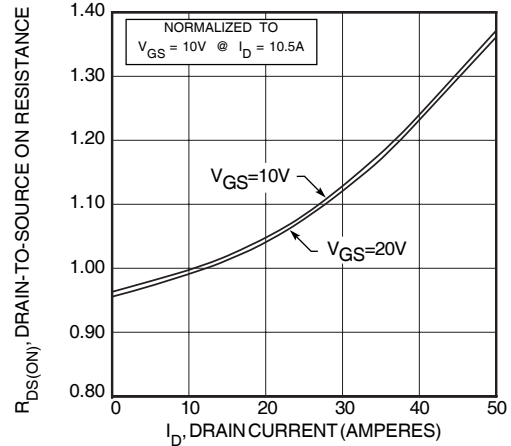


FIGURE 5,  $R_{DS(ON)}$  vs DRAIN CURRENT

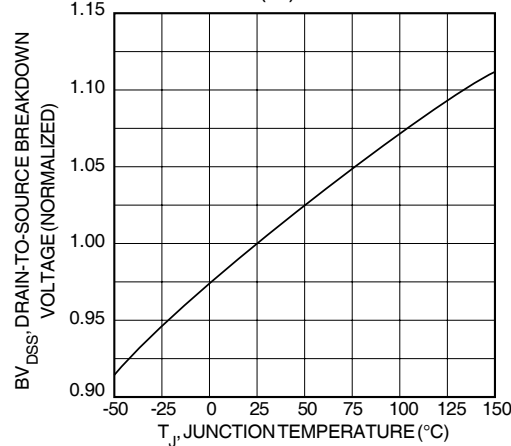


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

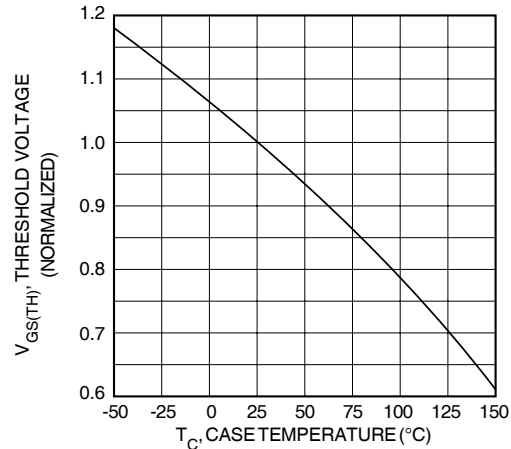


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

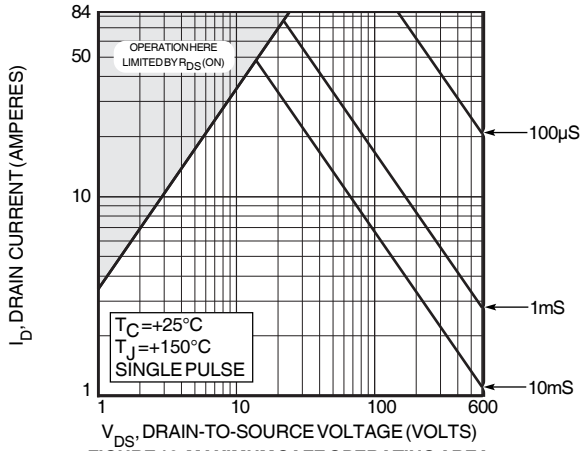


FIGURE 10, MAXIMUM SAFE OPERATING AREA

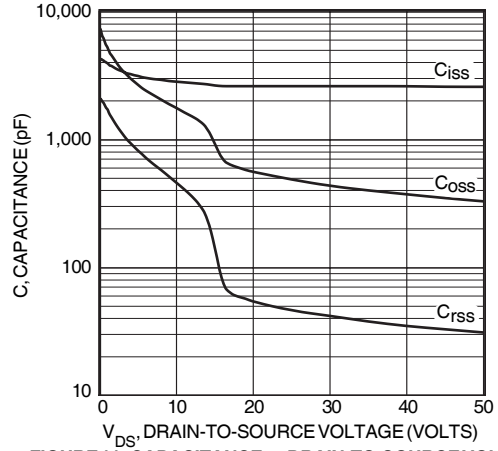


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

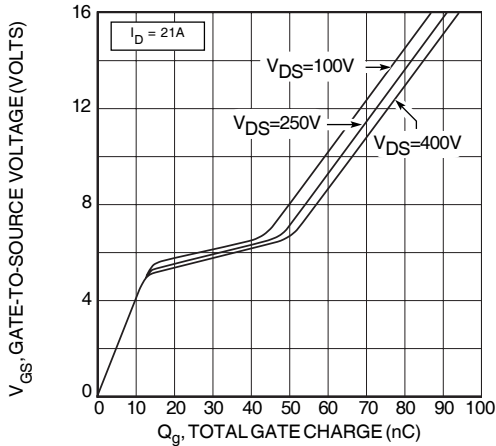


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

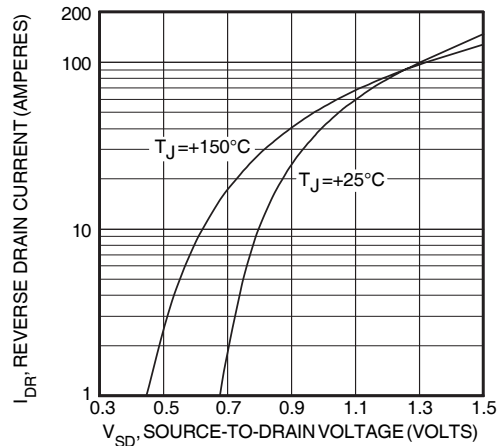


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

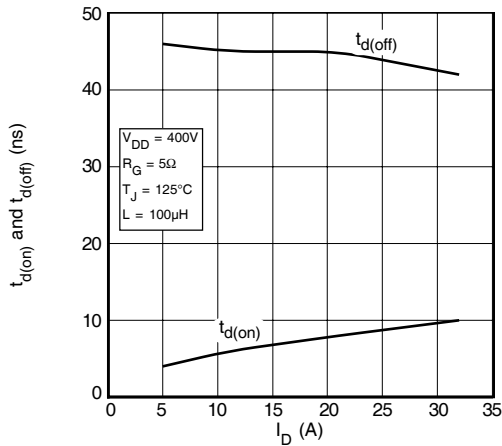


FIGURE 14, DELAY TIMES vs CURRENT

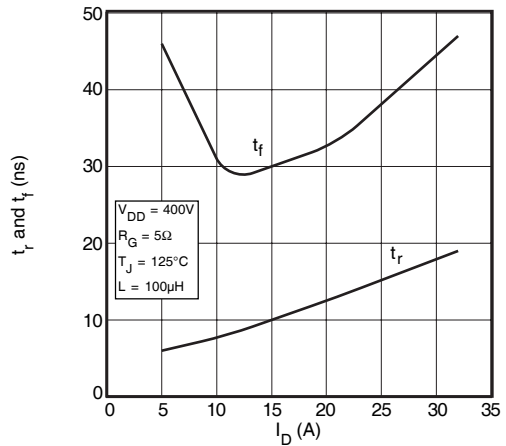


FIGURE 15, RISE AND FALL TIMES vs CURRENT

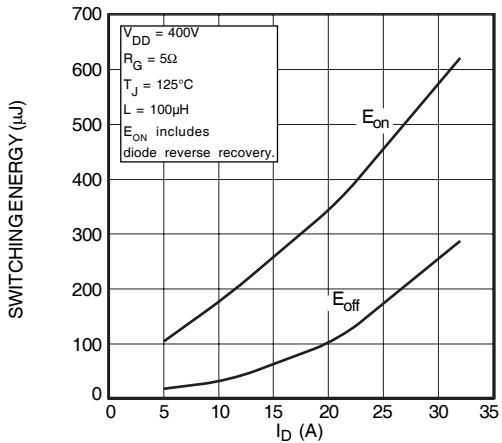


FIGURE 16, SWITCHING ENERGY vs CURRENT

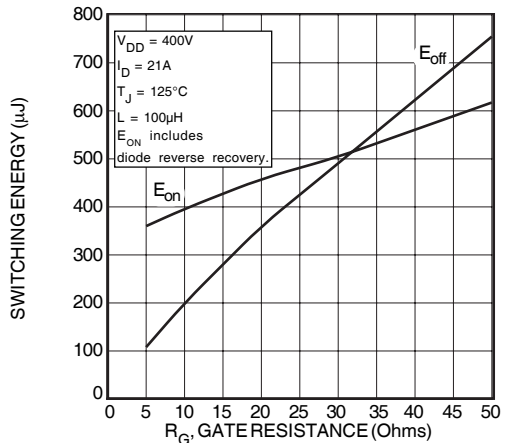


FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE

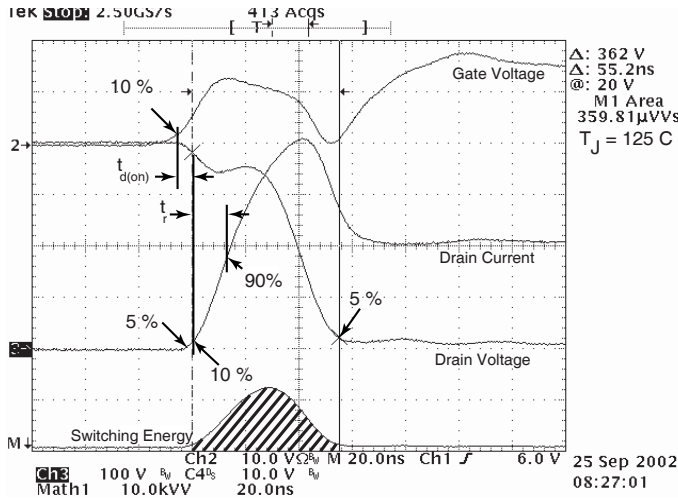


Figure 18, Turn-on Switching Waveforms and Definitions

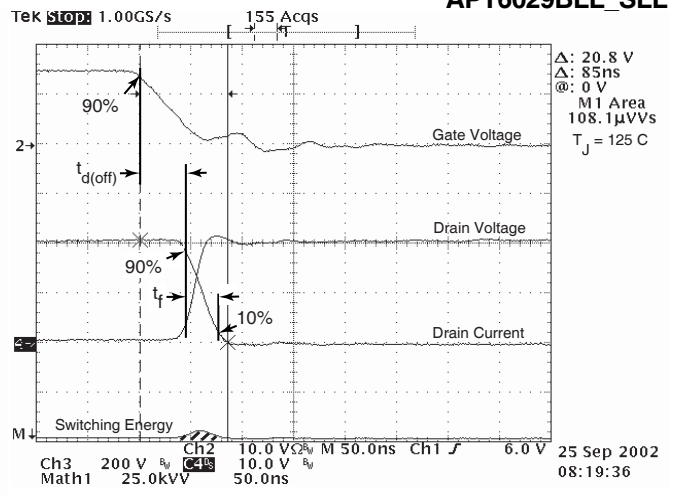


Figure 19, Turn-off Switching Waveforms and Definitions

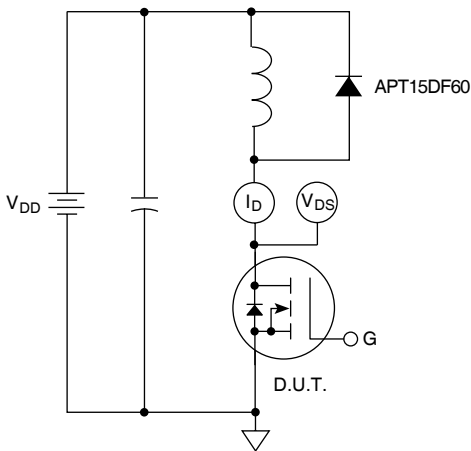
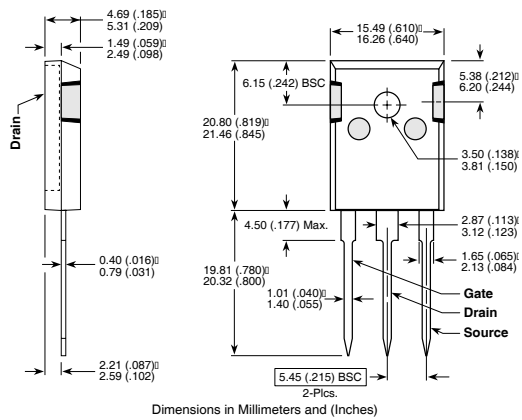
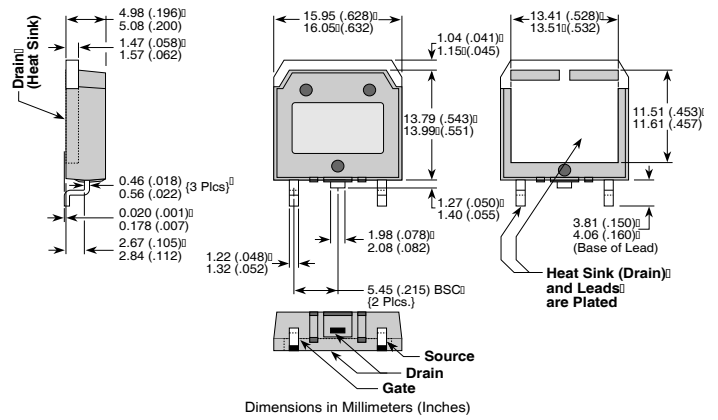


Figure 20, Inductive Switching Test Circuit

TO-247 Package Outline



D<sup>3</sup>PAK Package Outline



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