ADVANCE INFORMATION

Am29LV065M

64 Megabit (8 M x 8-Bit) MirrorBit™ 3.0 Volt-only Uniform Sector Flash Memory with VersatileI/O™ Control

DISTINCTIVE CHARACTERISTICS

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - 3 volt read, erase, and program operations
- **Enhanced VersatileI/O™ control**
  - Device generates data output voltages and tolerates data input voltages as determined by the voltage on the V_{IO} pin; operates from 1.65 to 3.6 V
- **Manufactured on 0.23 µm MirrorBit process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - 256-byte sector for permanent, secure identification through an 16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - One hundred twenty-eight 64 Kbyte sectors
- **Compatibility with JEDEC standards**
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - 90 ns access time
  - 25 ns page read times
  - 0.4 s typical sector erase time
  - 3.0 µs typical write buffer byte programming time: 32-byte write buffer reduces overall programming time for multiple-byte updates
  - 8-byte read page buffer
  - 32-byte write buffer
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - 30 mA typical active read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- **Package options**
  - 48-pin TSOP
  - 63-ball FBGA

SOFTWARE & HARDWARE FEATURES

- **Software features**
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - Unlock Bypass Program command reduces overall multiple-byte programming time
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - Sector Group Protection: hardware method of preventing write operations within a sector group
  - Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
  - ACC (high voltage) pin accelerates programming time for higher throughput during system production
  - Hardware reset pin (RESET#) resets device
  - Ready/Busy# pin (RY/BY#) detects program or erase cycle completion

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GENERAL DESCRIPTION

The Am29LV065M is a 64 Mbit, 3.0 volt single power supply flash memory devices organized as 8,388,608 bytes. The device has an 8-bit wide data bus, and can be programmed either in the host system or in standard EPROM programmers.

An access time of 90, 100, 110, or 120 ns is available. Note that each device has a specific operating voltage range (V_{CC}) and an I/O voltage range (V_{IO}), as specified in the Product Selector Guide and the Ordering Information sections. The device is offered in a 48-pin TSOP or 63-ball FBGA package. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0 volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** input provides shorter programming times through increased current. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

The **VersatileI/O™** (V_{IO}) control allows the host system to set the voltage levels that the device generates at its data outputs and the voltages tolerated at its data inputs to the same voltage level that is asserted on the V_{IO} pin. This allows the device to operate in a 1.8 V or 3 V system environment as required.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

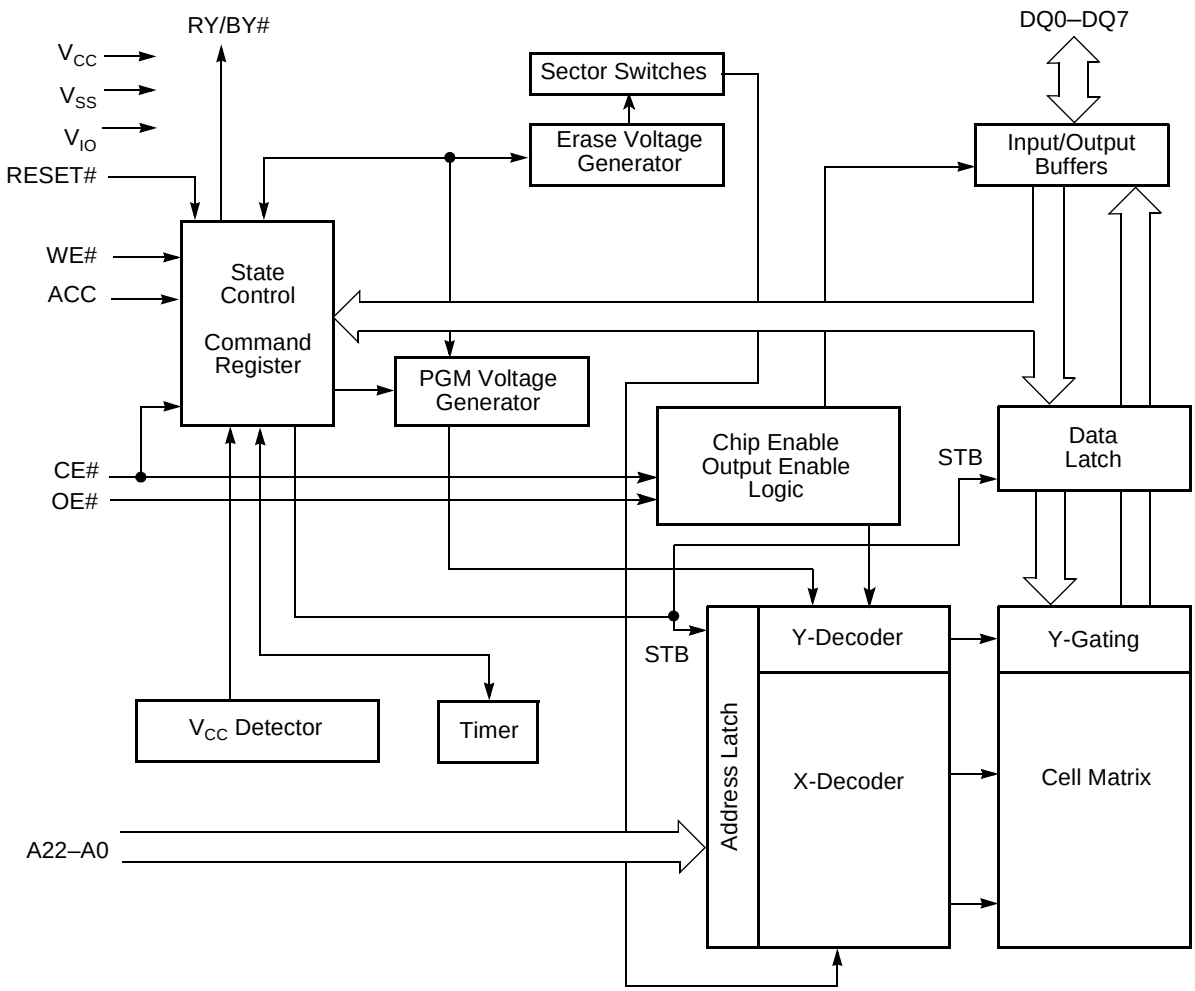
The **SecSi™ (Secured Silicon) Sector** provides a 256 byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

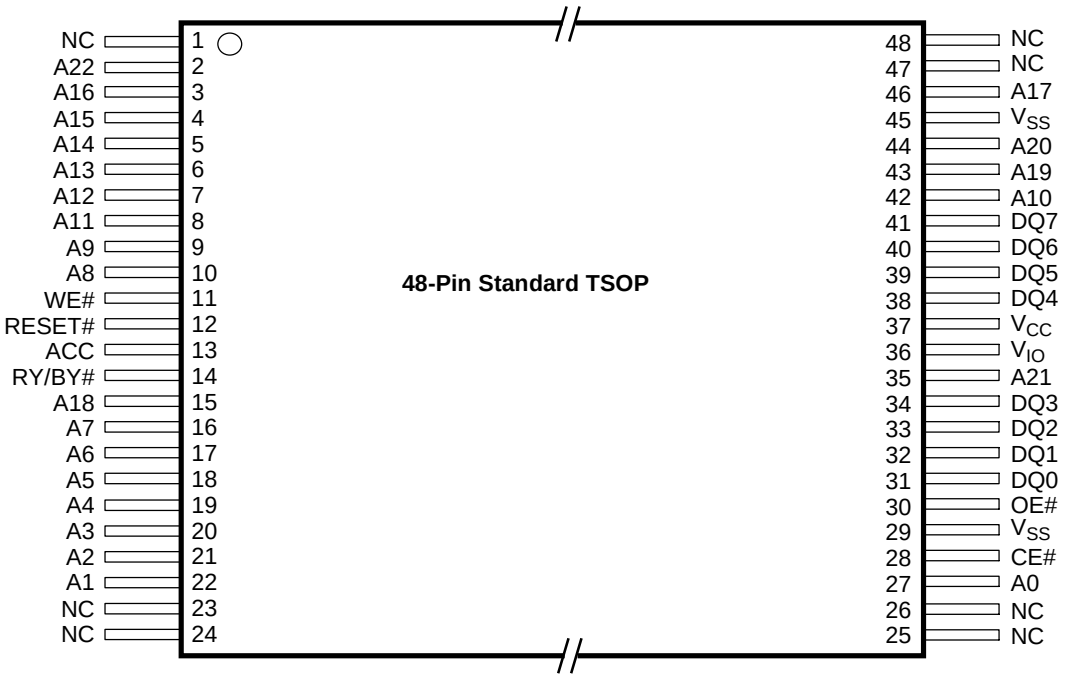
PRODUCT SELECTOR GUIDE

Part Number		Am29LV065M			
Speed Option	V_{CC} = 3.0–3.6 V	**90R** (V_{IO} = 3.0–3.6 V)			
	V_{CC} = 2.7–3.6 V		**101** (V_{IO} = 2.7–3.6 V)	**112** (V_{IO} = 1.65–3.6 V)	**120** (V_{IO} = 1.65–3.6 V)
Max. Access Time (ns)		90	100	110	120
Max. CE# Access Time (ns)		90	100	110	120
Max. Page access time (t_{PACC})		25	30	40	40
Max. OE# Access Time (ns)		25	30	40	40

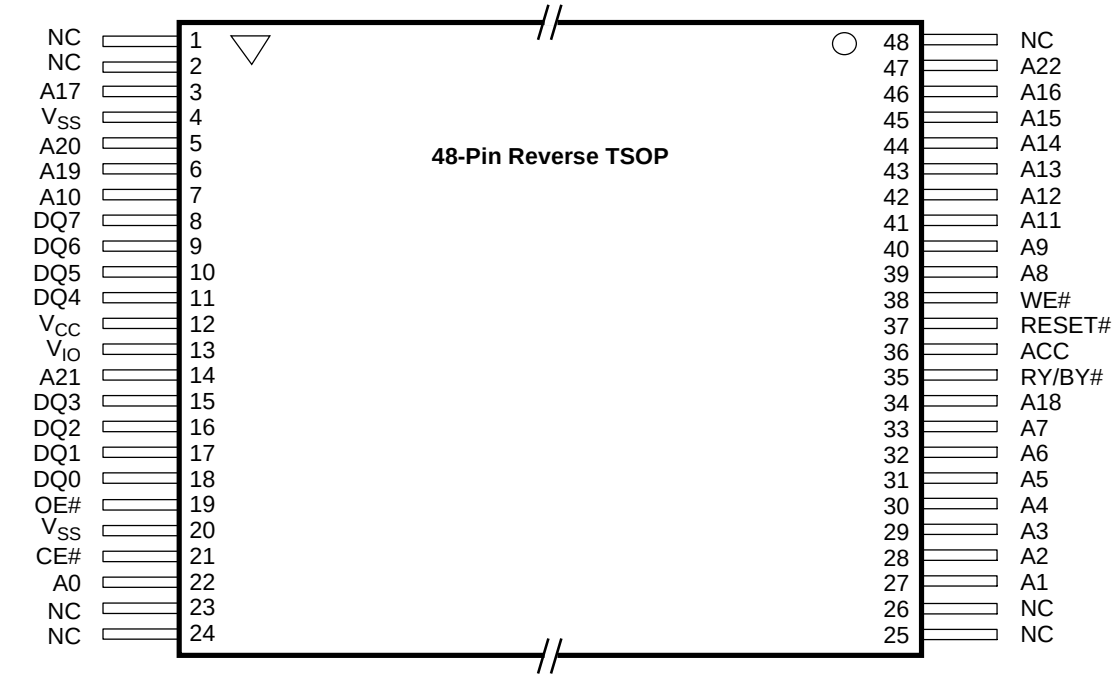
BLOCK DIAGRAM



CONNECTION DIAGRAMS



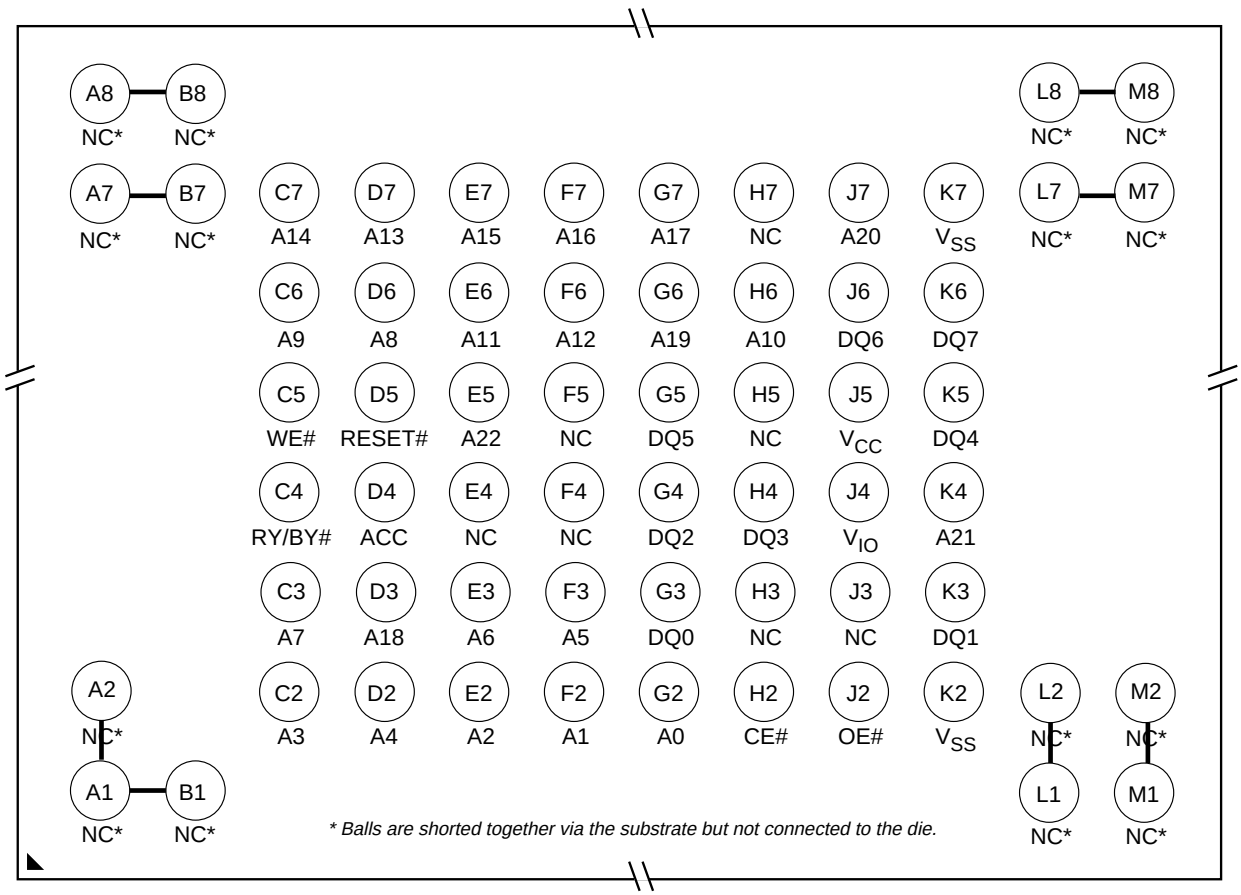
48-Pin Standard TSOP



48-Pin Reverse TSOP

CONNECTION DIAGRAMS

63-Ball FBGA
Top View, Balls Facing Down



Special Handling Instructions for FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

A22–A0 = 23 Address inputs

DQ7–DQ0 = 8 Data inputs/outputs

CE# = Chip Enable input

OE# = Output Enable input

WE# = Write Enable input

ACC = Acceleration input

RESET# = Hardware Reset Pin input

RY/BY# = Ready/Busy output

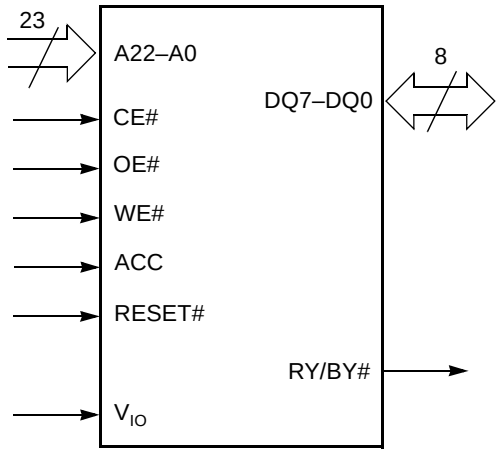
V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{IO} = Output Buffer power

V_{SS} = Device Ground

NC = Pin Not Connected Internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

Am29LV065M U 90R WH I

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
E = 48-Pin Standard Pinout Thin Small Outline Package (TS 048)
F = 48-Pin Reverse Pinout Thin Small Outline Package (TSR048)
WH = 63-Ball Fine-Pitch Ball Grid Array (FBGA)
0.80 mm pitch, 11 x 12 mm package (FBE063)

SPEED OPTION
See Product Selector Guide and Valid Combinations

SECTOR ARCHITECTURE
U = Uniform sector device

DEVICE NUMBER/DESCRIPTION
Am29LV065M
64 Megabit (8 M x 8-Bit) MirrorBit™ Uniform Sector Flash Memory with VersatileIO™ Control
3.0 Volt-only Read, Program, and Erase

Valid Combinations for TSOP Package		Speed (ns)	V_{IO} Range	V_{CC} Range
Am29LV065MU90R	EI, FI	90	3.0–3.6 V	3.0–3.6 V
Am29LV065MU101		100	2.7–3.6 V	2.7–3.6 V
Am29LV065MU112		110	1.65–3.6 V	
Am29LV065MU120		120	1.65–3.6 V	

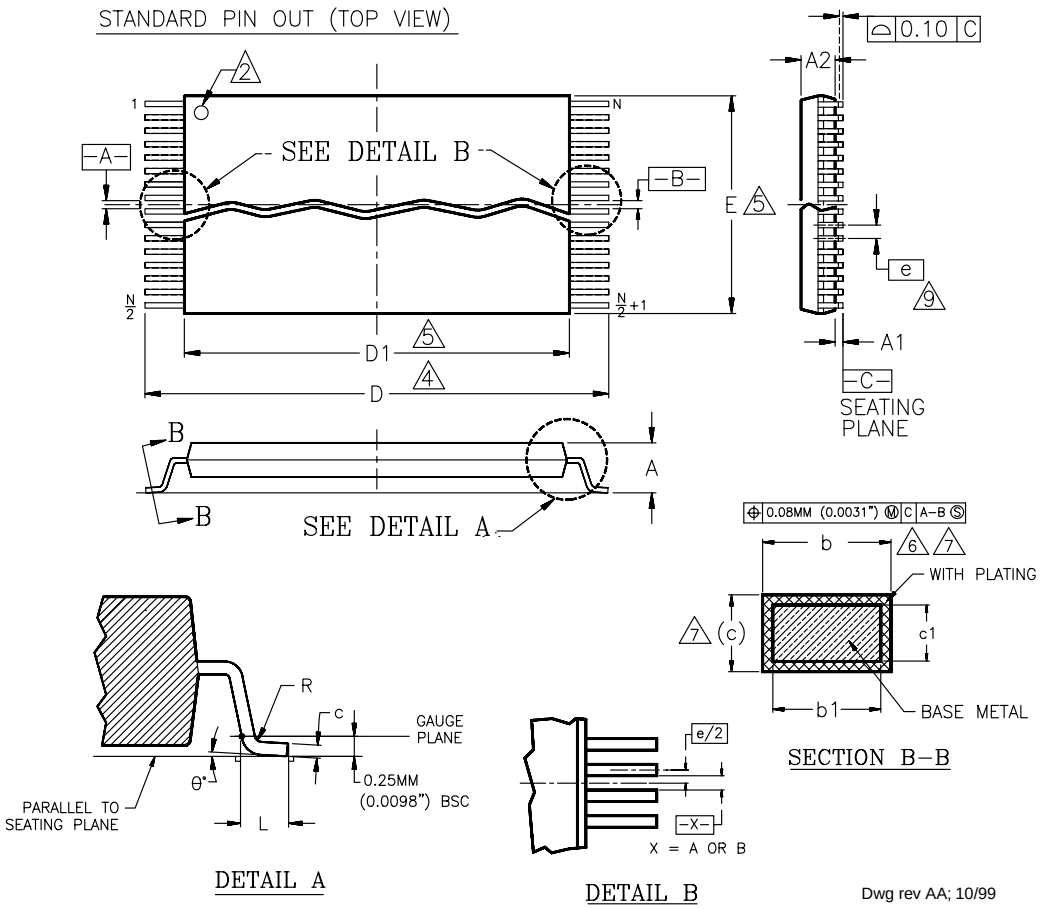
Valid Combinations for Fine-Pitch BGA Package				Speed (ns)	V_{IO} Range	V_{CC} Range
Order Number		Package Marking				
Am29LV065MU90R	WHI	L065MU90R	I	90	3.0–3.6 V	3.0–3.6 V
Am29LV065MU101		L065MU01V		100	2.7–3.6 V	2.7–3.6 V
Am29LV065MU112		L065MU11V		110	1.65–3.6 V	
Am29LV065MU120		L065MU12V		120	1.65–3.6 V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PHYSICAL DIMENSIONS

TS 048—48-Pin Standard Thin Small Outline Package



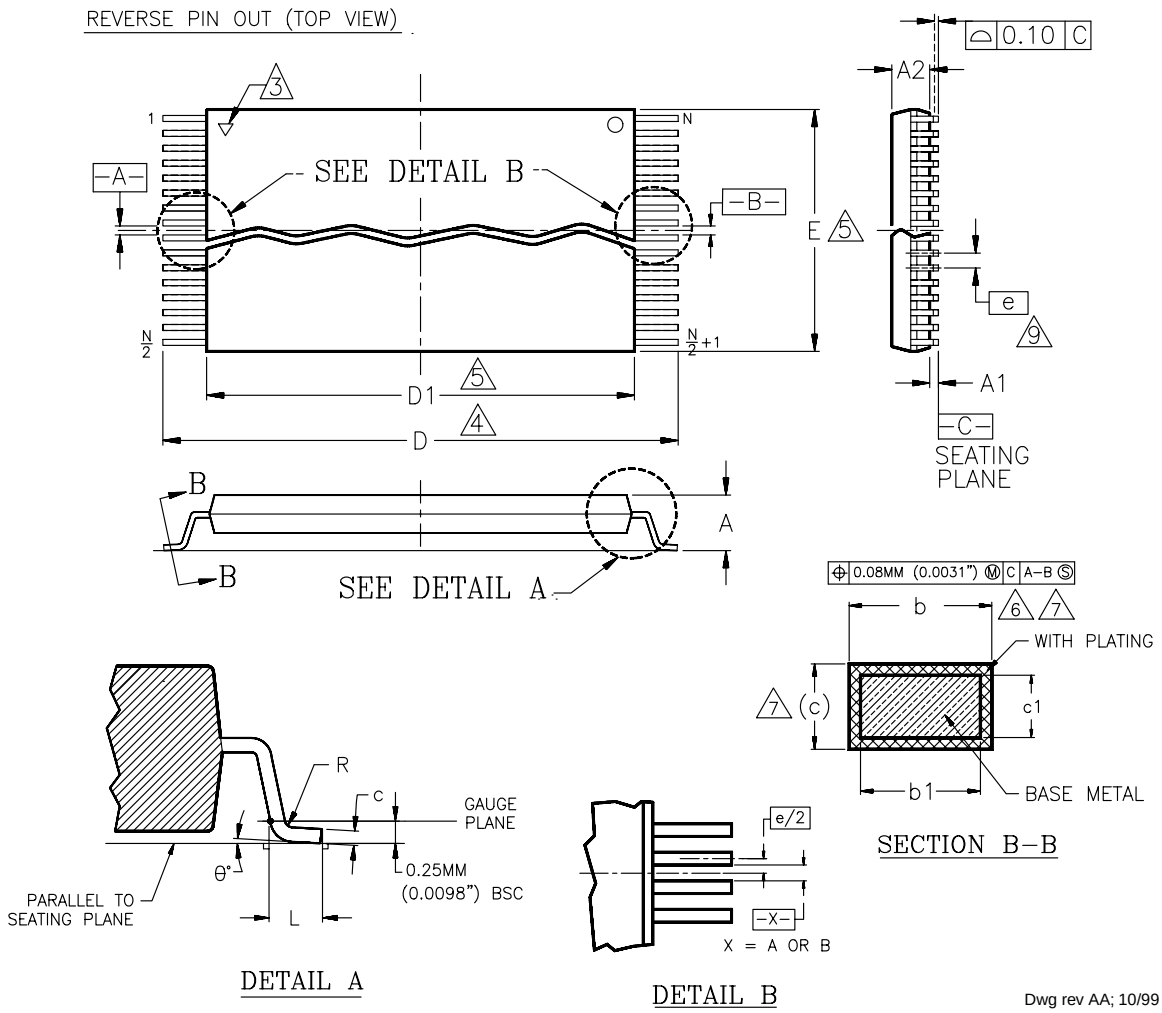
Package	TS 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS

TSR048—48-Pin Reverse Thin Small Outline Package



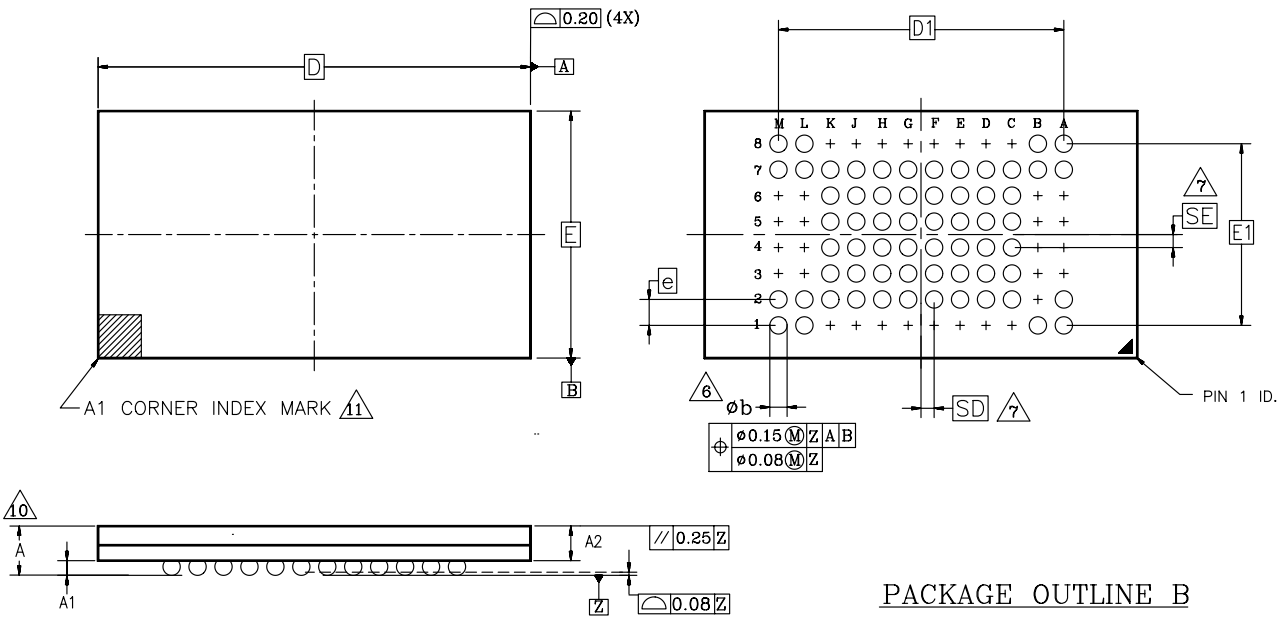
Package	TSR 48		
Jedec	MO-142 (B) DD		
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	48		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

PHYSICAL DIMENSIONS

FBE063—63-Ball Fine-Pitch Ball Grid Array, 12 x 11 mm Package



PACKAGE OUTLINE B

Dwg rev AF; 10/99

PACKAGE	xFBE 063			
JEDEC	N/A			
	12.00mmx11.00mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	OVERALL THICKNESS
A1	0.20	–	–	BALL HEIGHT
A2	0.84	–	0.94	BODY THICKNESS
D	12.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	8.80 BSC			BALL FOOTPRINT
E1	5.60 BSC			BALL FOOTPRINT
MD	12			ROW MATRIX SIZE D DIRECTION
ME	8			ROW MATRIX SIZE E DIRECTION
N	63			TOTAL BALL COUNT
b	0.25	0.30	0.35	BALL DIAMETER
e	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A3–A6,B2–B6 L3–L6, M3–M6 C1–K1,C8–K8			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE MAXIMUM NUMBER OF SOLDER BALLS FOR MATRIX SIZE MD x ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000 WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" IN THE PACKAGE DRAWING INDICATE THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. FOR PACKAGE THICKNESS A IS THE CONTROLING DIMENSION.
11. A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTION OR OTHER MEANS.

REVISION SUMMARY

Revision A (August 3, 2001)

Initial release as abbreviated Advance Information data sheet.

Revision A+1 (October 3, 2001)

Global

Added 120 ns device, changed 100 ns, V_{IO} = 1.65–2.7 V device to 110 ns, changed 90 ns operating range to 3.0–3.6 V.

Physical Dimensions

Added section.