AKD4702
Evaluation board Rev.A for AK4702

GENERAL DESCRIPTION

AKD4702 is an evaluation board for quickly evaluating the AK4702 , 2ch DAC with AV SCART switch. Evaluation requires a audio/video analog analyzer, an analog video signal source, a digital audio signal source, and a power supply. AKM's ADC evaluation board can be also used for the audio source. Also included is a AK4112B digital audio interface receiver which receives SPDIF compatible audio data. The digital audio data is available via optical connector or BNC.

AKD4702 --- Evaluation board for AK4702
(Cable for connecting with printer port of IBM-AT compatible PC and control software are enclosed with board.)

FUNCTION

- BNC connectors for analog audio input/output
- BNC connectors for analog video input/output
- On-board clock generator
- BNC connector for an external clock input
- Compatible with 2 types of digital interface
  1. Serial interface: Direct interface with evaluation boards for AKM's A/D converter evaluation boards.
  2. S/PDIF: On-board AK4112BVF as DIR that accepts optical input or BNC input
- 10pin header for serial control interface

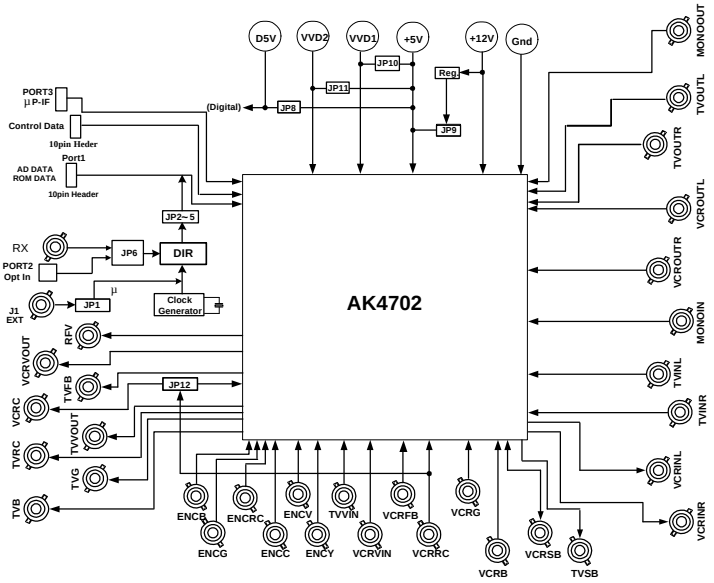


Figure 1. AKD4702 Block Diagram

- Circuit diagram and PCB layout are attached at the end of this manual.

■ Operation sequence

1) Set up the power supply lines. (Note 1)

[+12V]	(Orange)	= +11.4 ~ +12.6V
[+5V]	(Red)	= +4.75 ~ +5.25V (Note 2)
[D5V]	(Red)	= +4.75~ +5.25V (Note 3)
[VVD1]	(Red)	= +4.75~ VVD2 (Note 4)
[VVD2]	(Blue)	= VDD1~ +5.25V (Note 4)
[AGND]	(Black)	= 0V
[DGND]	(Black)	= 0V
[VVSS2]	(Black)	= 0V

Note: 1. Each supply line should be distributed from the power supply unit.
2. JP9 (REG) should be open when the "+5V" jack is used.
3. JP8 (D-A) should be open when the "D5V" jack is used.
4. JP10 (VDD1) / JP11 (VDD2) should be open when the "VDD1" jack / "VDD2" jack are used respectively.

2) Set-up the evaluation modes, jumper pins and DIP-switches. (Refer following sections.)

3) Connect the PORT3 (=µP-I/F) with PC by the enclosed 10-wire flat cable.

4) Set up the PC and execute the enclosed control software. (See "CONTROL SOFTWARE MANUAL".)

5) Turn the power on.

6) Reset the AK4702 once by bringing the SW1 (PDN) "L", and turn it to "H".

■ Evaluation mode

1) S/PDIF mode (Optical Link or BNC: default)

When the CM0 (DIP-switch S1_1 on board) is "L", the AK4112B (DIR) generates MCLK, BICK, LRCK and SDATA from the received bitstream through PORT2 (TORX176: optical link) or J2 (BNC). This mode is used for the evaluation using CD test disk. The PORT1 (EXT) should be open.

1)-1. DIP-switch set-up

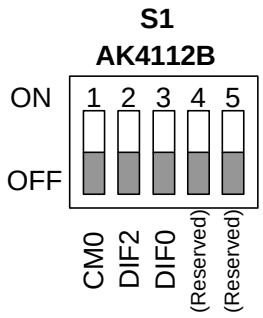
No.	CM0	DIF1	DIF0	Audio Data Format of AK4112B	Notes
1	"L"	"L"	"L"	16bit LSB justified	1
2	"L"	"L"	"H"	18bit LSB justified	2
3	"L"	"H"	"L"	MSB justified	3
4	"L"	"H"	"H"	I^2S	4

Table 1. DIP-switch set-up

Please match the data format of AK4702 via I^2C-bus control as following notes.

Note 1. 16bit LSB justified

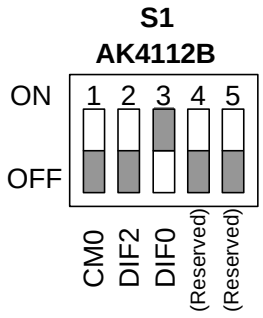
Set up the DIP-switch as follows.



Set up the control registers DIF1/0 of AK4702 by enclosed software as follows.

Note 2. 18bit LSB justified

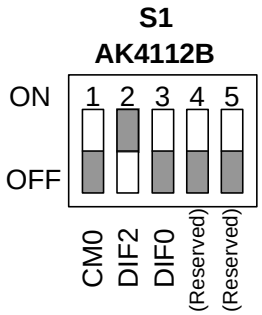
Set up the DIP-switch as follows.



Set up the control registers DIF1/0 of AK4702 by enclosed software as follows.

Note 3. MSB justified

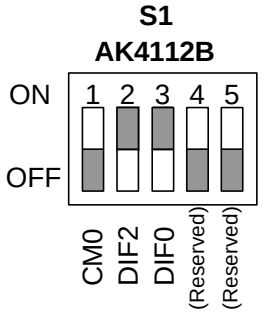
Set up the DIP-switch as follows.



Set up the control registers DIF1/0 of AK4702 by enclosed software as follows.

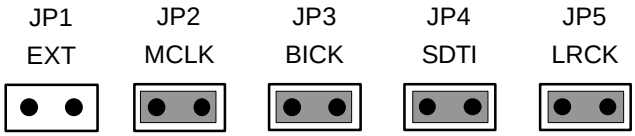
Note 4. I^2S

Set up the DIP-switch as follows.

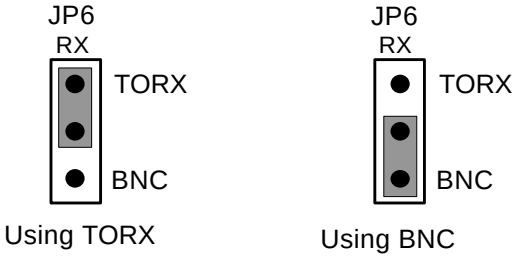


Set up the control registers DIF1/0 of AK4702 by enclosed software as follows.

1)-2. Jumper pins set up



The JP6 selects the input port of S/P DIF bitstream form Port2 (TOTX176) or J2 (BNC RX).



2) On-board X'tal mode/ Feeding external MCLK via BNC

When the CM0 (DIP-switch S1_1 on board) is "H", the AK4112B generates MCLK, BICK and LRCK from on-board X'tal or external clock form J1. SDATA should be fed via PORT1.

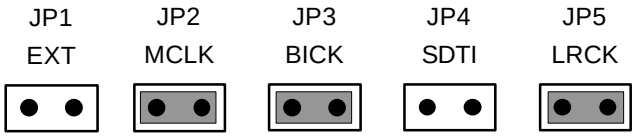
2)-1. DIP-switch set-up

No.	CM0	DIF1	DIF0
1	"H"	Don't care	Don't care

Table 2. DIP-switch set-up

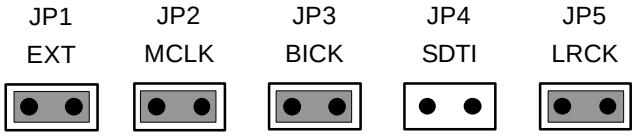
2)-2. Jumper pins set up

2)-2-a. Using on-board X'tal



JP6: Don't care.

2)-2-b. Using external clock via BNC connector J1



JP6: Don't care.
Remove the on-board X'tal.

3) Feeding all clocks from external

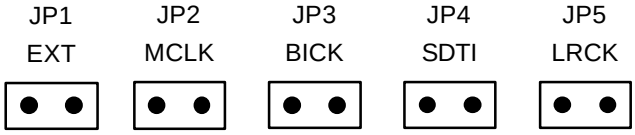
Under the following set-up, all external signals can be fed to AK4702 through POTR1 (EXT).
The AKM's evaluation board for ADC can be used.

3)-1. DIP-switch set-up

No.	CM0	DIF1	DIF0
1	Don't care	Don't care	Don't care

Table 3. DIP-switch set-up

3)-2. Jumper pins set up



JP6: Don't care.

■ Other jumper pins set up

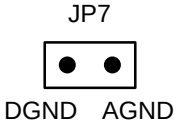
[JP12](VCRRC): Input Jack selection for the VCRRC pin of AK4702

When the VCRC pin of AK4702 outputs 0V by setting CIO bit to "1", the signal can be fed through the J27 (VCRCOUT) to VCRRC pin.

"I": The signal is fed through the J18(VCRRC) to VCRRC pin. (Default)
"I/O": The signal is fed through the J27(VCRCOUT) to VCRRC pin. The CIO bit of AK4702 should be set to "1".

[JP7](GND): Analog ground and digital ground

Open: separated. (Default)
Short: connected. (The jack "DGND" can be open.)



■ DIP-switch (S1) List

No.	Switch Name	Default	Function
1	CM0	OFF	Refer the "■ **Evaluation mode**"
2	DIF0	OFF	
3	DIF2	OFF	
4	-	OFF	(Reserved)
5	-	OFF	(Reserved)

Table 4. DIP-switch list

■ Jumper List

No.	Jumper Name	Function
1	EXT	MCLK source set-up when CM0="H". Short: X'tal (default). Open: External clock via BNC (J1). Remove the on-board X'tal.
2,3, 4,5	MCLK, BICK, LRCK, SDTI	Clock source set-up Short: Connect the DIR (AK4112B). (default) Open: Separate the DIR. Supply clocks via Port1.
6	RX	S/PDIF's port set-up when CM0="L". TORX: Optical connector PORT2. (default) BNC: BNC connector J2.
7	GND	Analog ground and digital ground Open: separated (default). Short: connected (The connector "DGND" can be open.).
8	D-A	Power supply source set-up for digital section of AKD4702. Open: from the "D5V" Jack. (default) Short: from the regulator or the "+5V" Jack. Don't connect anything to the "D5V" Jack.(default)
9	REG	Power supply source set-up for VD of AK4702. Open: from the "+5V" Jack. Short: from the regulator. Don't connect anything the "+5V" Jack. (default)
10	VVD1	Power supply source set-up for VVD1 of AK4702. Open: from the "VVD1" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "VVD1" Jack. (default)
11	VVD2	Power supply source set-up for VVD1 of AK4702. Open: from the "VVD2" Jack. Short: from the regulator or the "+5V" Jack. Don't connect anything to the "VVD2" Jack. (default)
12	VCRRC	Input Selection for VCRRC "I" side: Input to VCRRC from VCRRC jack. "I/O" side: Input to VCRC from VCRC jack. (Note: Refer CIO bit of AK4702)

Table 5. Jumper list

■ Serial Control

The AK4702 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT3 (µP-IF) with PC by 10 wire flat cable packed with the AKD4702.

Be careful connector direction. Flat cable should be connected 10-pin header, red line put on 10pin header 5 and 6 pin.

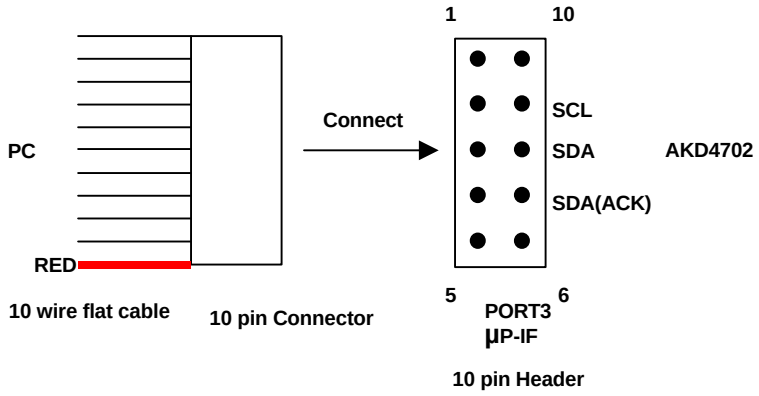


Figure 2. Connection of 10 pin flat cable for PORT3

■ Input/Output port List

Table 6. Input/Output port List

		Signal Name	Notes
Audio	Input	J5 (VCRINL), J3 (VCRINR), J9 (TVINL), J8 (TVINR)	Max: 2Vrms
		J11 (MONOIN)	Max: 1Vrm
	Output	J12 (VCROUTL), J10 (VCROUTR), J6 (TVOUTL), J7 (TVOUTR), J4 (MONOOUT)	Max: 3Vrm
Digital	Input	Port2 (TORX176) or J2 BNC (RX)	Max: D5V+0.3V
Video	Input	J13 (ENCB), J15 (ENCG), J17 (ENCRC), J19 (ENCC), J21 (ENCV), J23(ENCY), J25(TVVIN), J14(VCRVIN), J18(VCRRC; Note), J20(VCRG), J22(VCRB)	Max: 1.5Vp-p
	Output	J27 (VCRCOUT; Note), J29 (TVVOUT), J30 (TVRC), J31 (TVG), J32 (TVB), J33 (RFV), J34 (VCRVOUT)	Max: 3Vp-p
Slow Blanking	Input	J24 (VCRSB)	Max: VP+0.3V
	Output	J24 (VCRSB) , J28 (TVSB)	Max: VP
Fast Blanking	Input	J16 (VCRFB)	Max: VVD1+0.3V
	Output	J26 (TVFB)	Max: VVD2

Note: Refer JP12 and CIO bit of AK4702.

■ The indication content for LED

LED turns on during each output is “H”.

[LE1] (Unlock and Parity Error on S/P DIF): ERF of DIR (AK4112B). Normally off.

[LE2] (Validity Flag): V of DIR (AK4112B). Normally off.

■ Toggle switch (SW1 on board) operation

“H”: AK4702 is Active.

“L”: AK4702 is Powered Down .

(Note; When the power of AKD4702 is ON at first, SW1 should be switched from “L” to “H”.)

MEASUREMENT RESULTS

■ Audio

[Measurement condition]

- Measurement unit: Audio Precision System two Cascade
- MCLK : 256fs
- BICK : 64fs
- fs : 48kHz
- BW : 10Hz~20kHz
- Bit : 18bit
- Power Supply : VD=5V, VDD1=5V, VDD2=5V, VP=12V
- Interface : DIR
- Temperature : Room
- Volume#0=Volume#1=0dB
- Measurement signal line path: DAC → Volume#0 → Volume#1 → TVOUTL/R

Parameter	Input signal	Measurement filter	Results [dB]
S/(N+D) at 2Vrms Output	1kHz, 0dBFS	20kLPF	91.5
DR	1kHz, -60dBFS	22kLPF, A-weighted	96.0
S/N	"0" data	22kLPF, A-weighted	96.0

Plots

Figure 1-1. FFT (1kHz, 0dBFS input) at 2Vrms output
Figure 1-2. FFT (1kHz, -60dBFS input)
Figure 1-3. FFT (Noise floor)
Figure 1-4. FFT (Out-of band noise)
Figure 1-5. THD+N vs. Input Level (fin=1kHz)
Figure 1-6. THD+N vs. fin (Input Level=0dBFS)
Figure 1-7. Linearity (fin=1kHz)
Figure 1-8. Frequency Response (Input Level=0dBFS)
Figure 1-9. Crosstalk (Input Level=0dBFS)

■ Video

[Measurement condition]

- Signal Generator : Sony Tectonics TG2000
- Measurement unit: Sony Tectonics VM700T
- Power Supply : VD=5V, VDD1=5V, VDD2=5V, VP=12V
- Interface : BNC
- Temperature : Room
- Measurement signal line path: ENCV → TVVOUT, ENCRC → TVRC

Parameter	Measurement conditions	Results	Unit
S/N	Input = 0% flat field Filter = Uni-weighted, BW= 15kHz to 5MHz	75.8	dB
Crosstalk	Input = 100%red(ENCRC), Measured at TVVOUT	-52	dB
DG	Input = Modulated Lamp	-0.1 to +0.24	%
DP	Input = Modulated Lamp	0 to +0.40	deg.

Plots

Figure 2-1. Noise spectrum (Input=0%flat field, BW=15kHz to 5MHz, uni weighted)
Figure 2-2. Frequency Response (Input= Multi Burst)
Figure 2-3 Crosstalk (Input= 100% red (ENCRC), measured at TVVOUT)
Figure 2-4 DG, DP (Input= Modulated Lamp)

Plots (Audio)

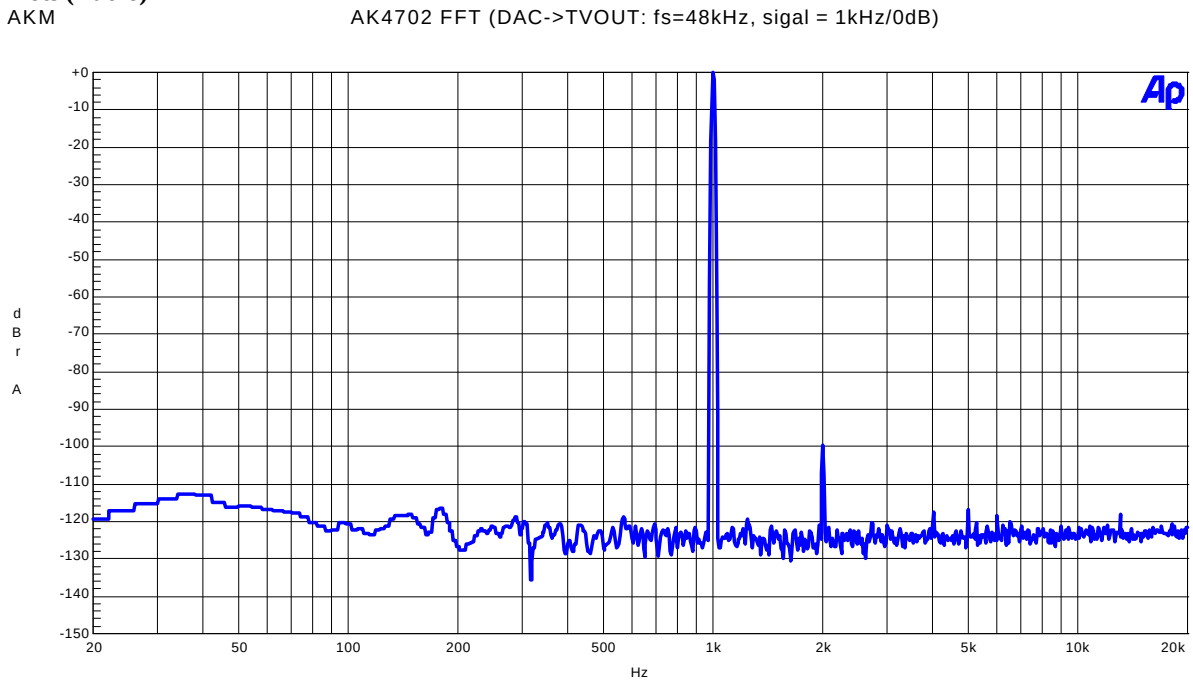


Figure1-1. FFT (fin=1kHz Input Level=0dBFS)

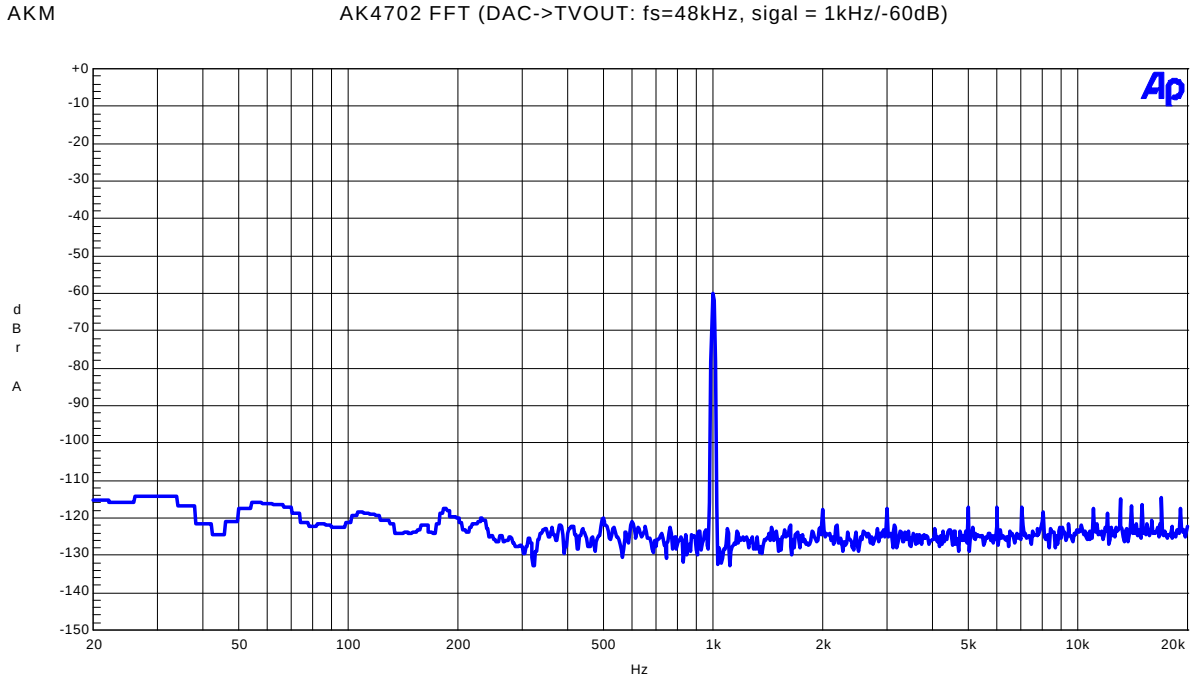


Figure-1-2. FFT (fin=1kHz Input Level=-60dBFS)

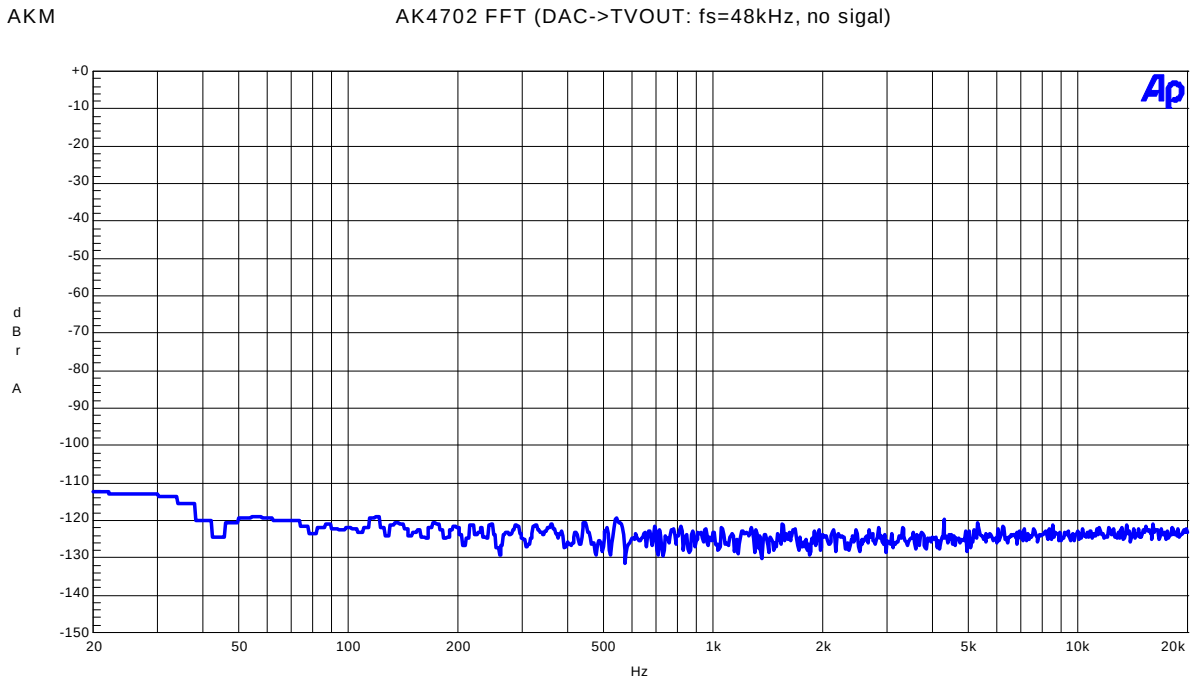


Figure1-3. FFT (Noise Floor)

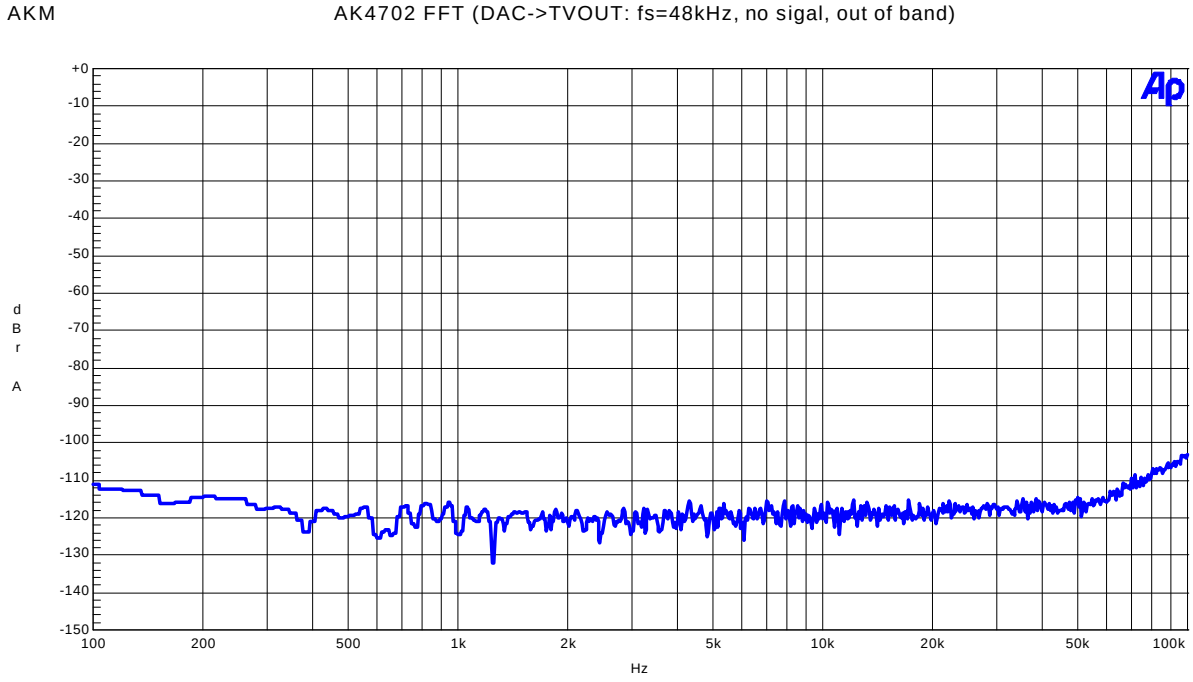


Figure1-4. FFT (Outband Noise)

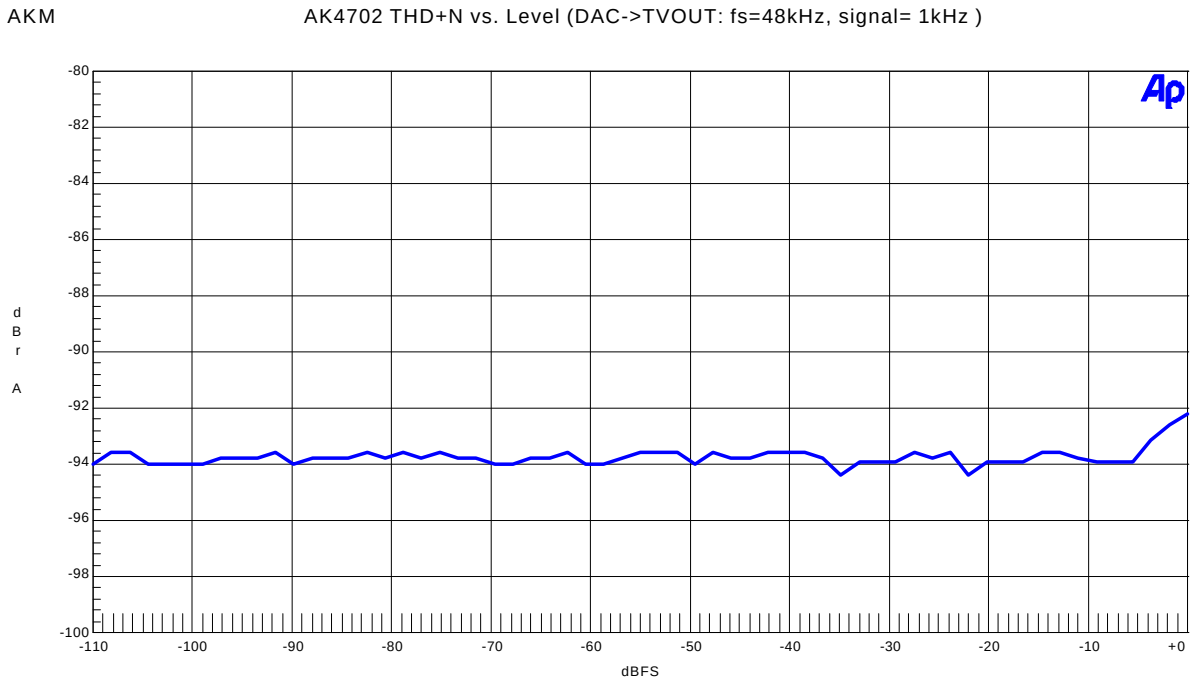


Figure1-5. THD+N vs. Input level (fin=1kHz)

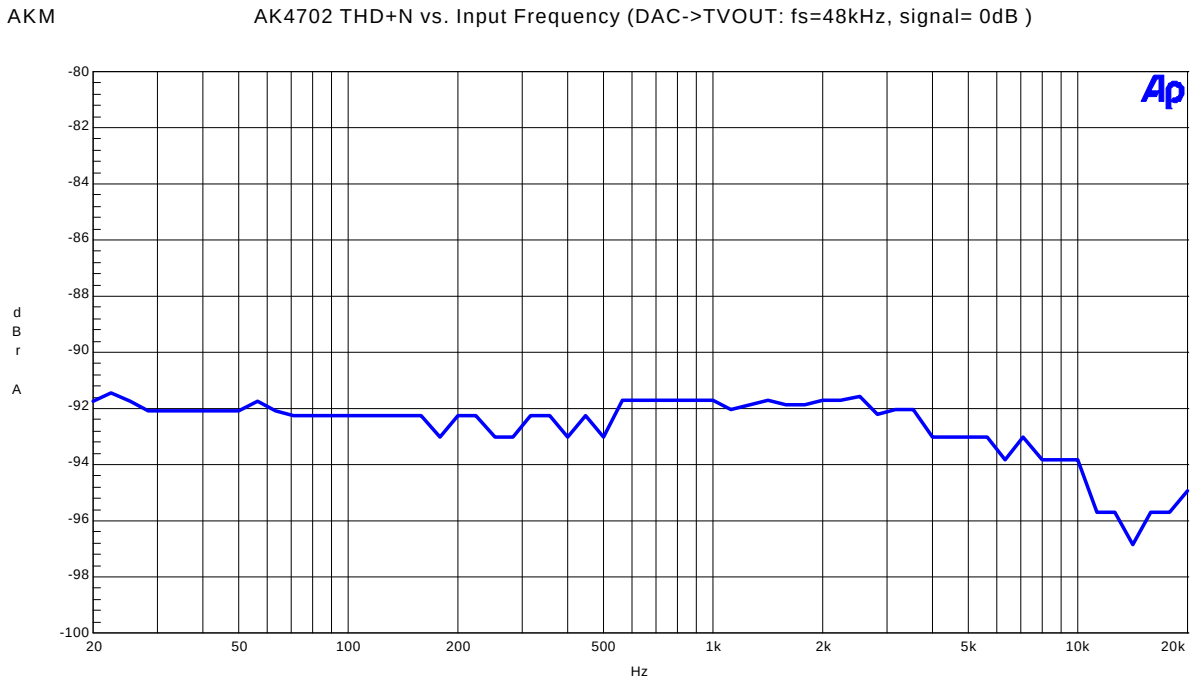


Figure1-6. THD+N vs. Input Frequency (Input level=0dBFS)

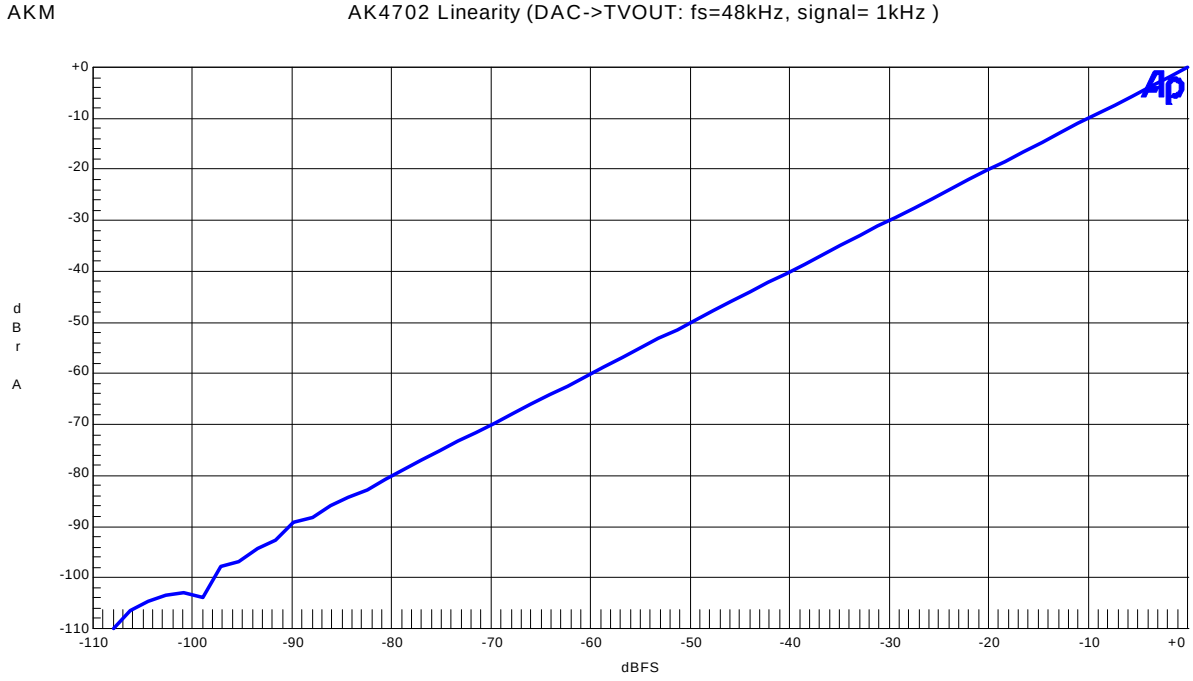


Figure1-7.Linearity (fin=1kHz)

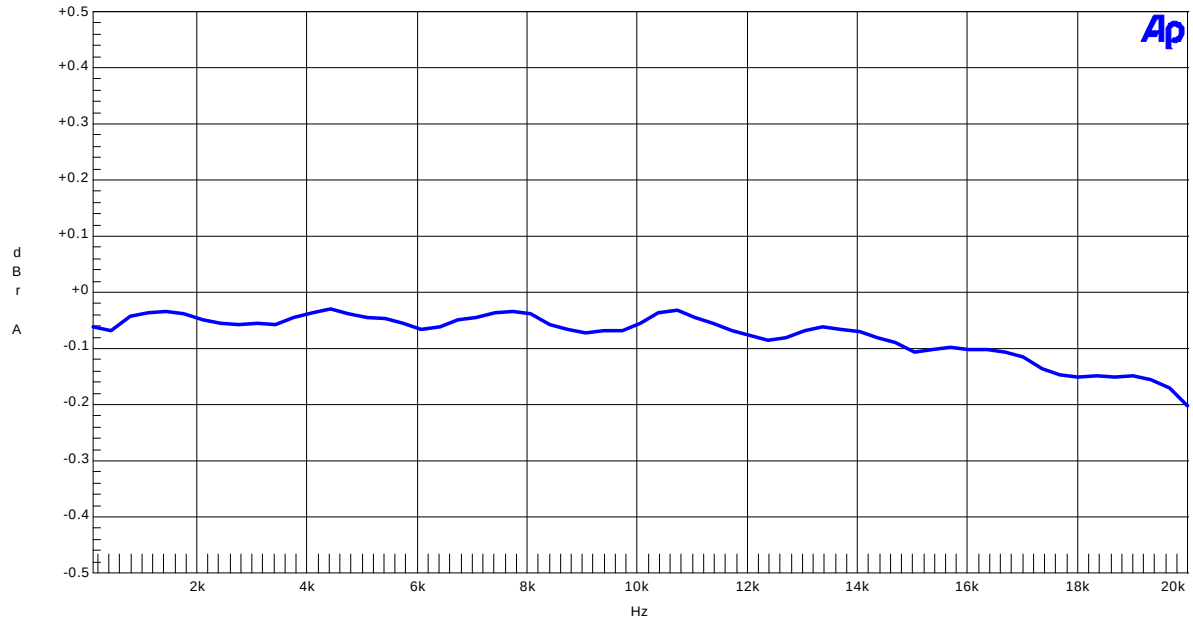


Figure1-8. Frequency Response (Input level=0dBFS)

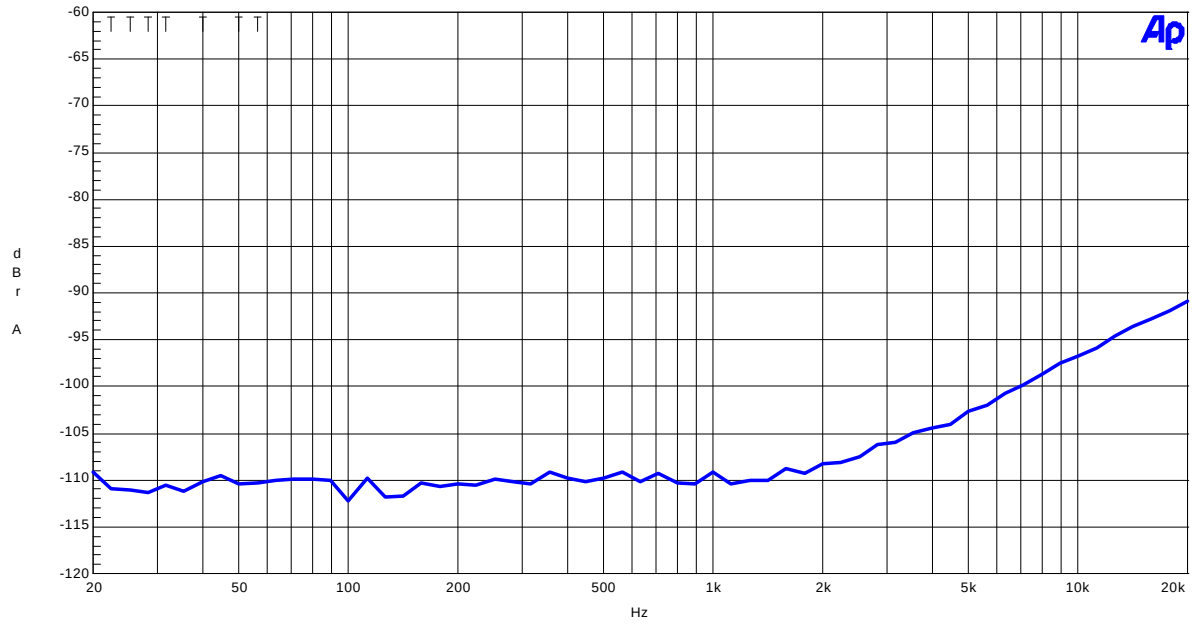


Figure1-9. Crosstalk (Input level=0dBFS)

Plots(Video)

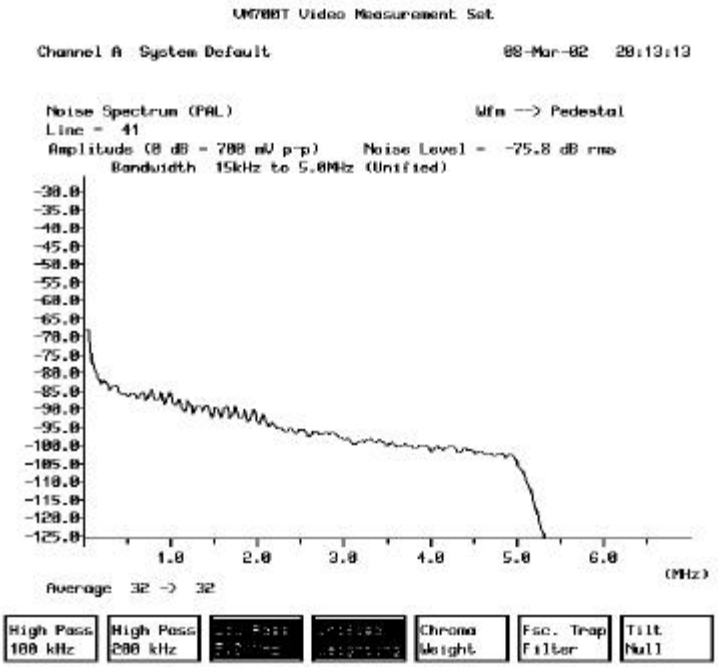


Figure 2-1. Noise spectrum (Input=0%flat field, BW=15kHz to 5MHz, uni weighted)

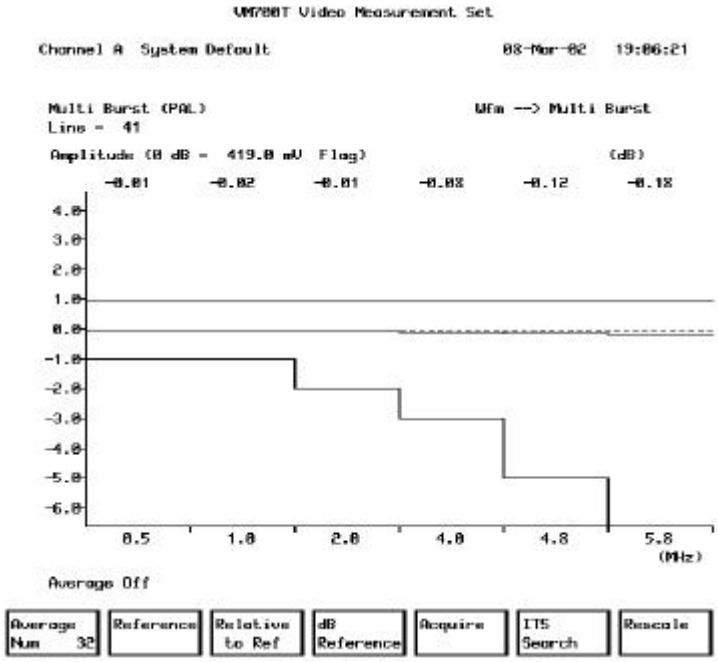


Figure 2-2. Frequency Response (Input= Multi Burst)

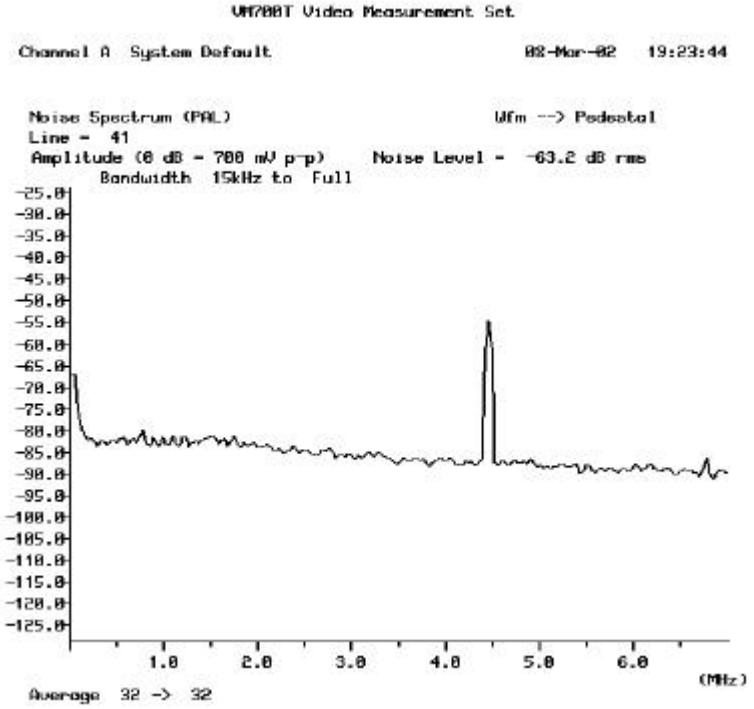


Figure 2-3 Crosstalk (Input= 100% red (ENCRC), measured at TVVOUT)

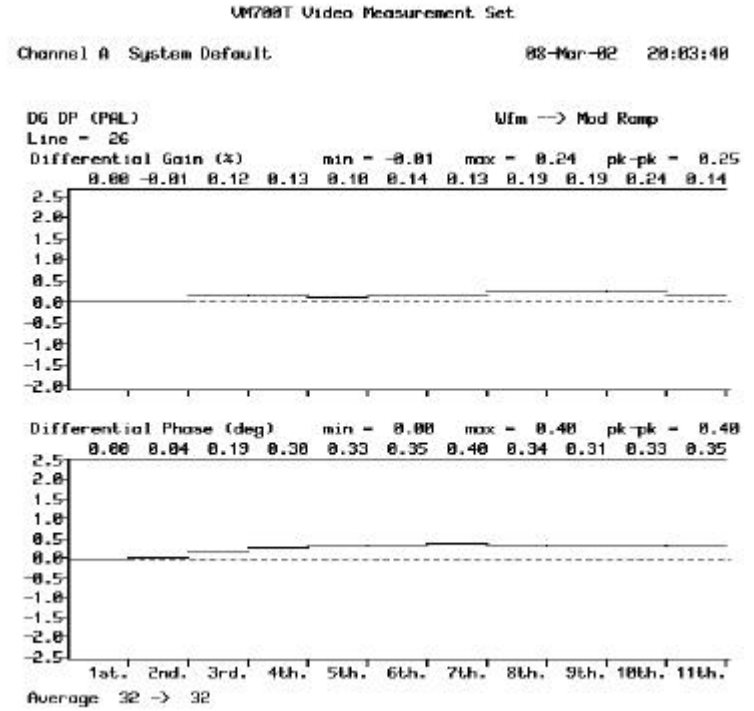


Figure 2-4 DG, DP (Input= Modulated Lamp)

CONTROL SOFTWARE MANUAL

■ Introduction

This is a manual of software that controls the AK4702, 2ch DAC with AV SCART switch.
The enclosed software AKD4702.exe can control the registers of AK4702 using I2C control I/F.

■ System Requirements

To use this software, the followings are required for PC.:

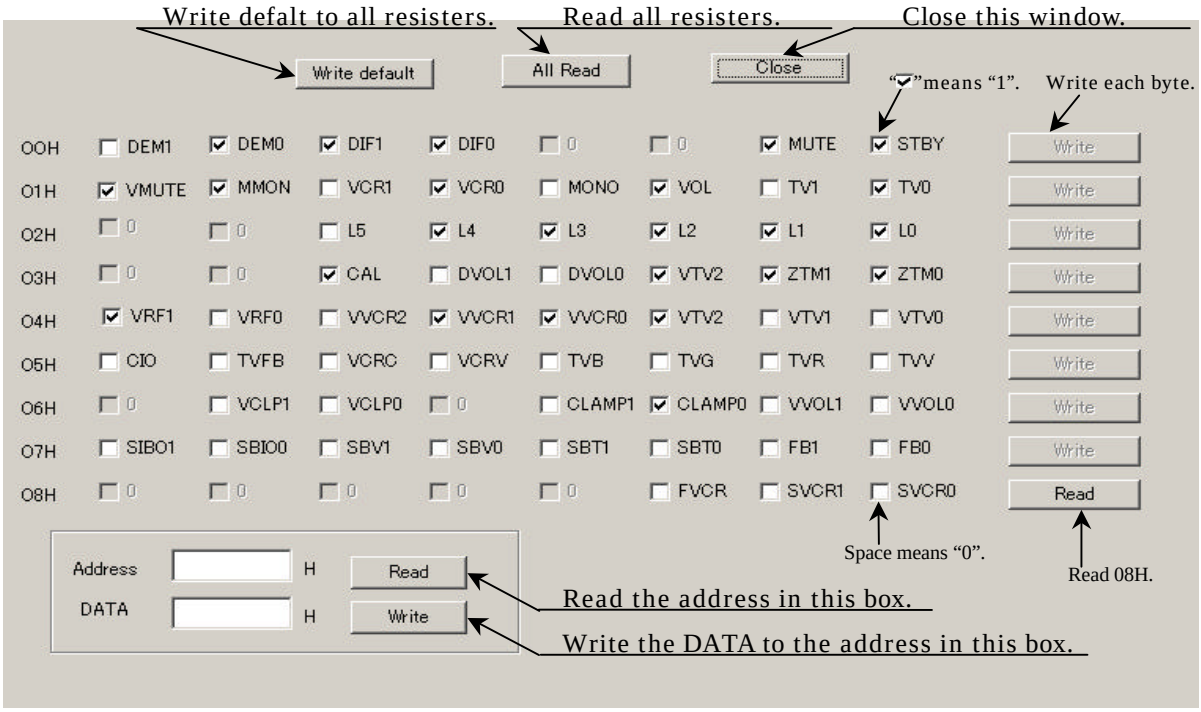
- Windows 95/98/ME/2000/XP. (This software does not operate on Windows NT.)
- Printer port

■ Set-up of evaluation board and control software

1. Set up the AKD4702.
2. Insert Connect IBM-AT compatible PC with AKD4702 by 10-line type flat cable (packed with AKD4702). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM disk when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)
3. The CD-ROM disk labeled "AKD4702 Control Program ver 1.0" into the CD-ROM disk drive.

■ Operations

[1] Execute the AKD4702.exe. Then the following window opens. The function of each button is shown below. Clicking the button does each operation in the alone.



[2] Write/Read Register

There are two ways to Write/Read register.

(1) Check box

After checking each box of each bit, click the “Write” or “Read” button in the right end. “☑” in each check box means “1” and no check means “0”. Each check mark toggles by clicking. The address 08H is Read-only.

(2) Edit box

There is an edit box in the left bottom. All register can be written and read using the edit box.
When writing register, input the DATA and the Address in the box and click “Write” button.
When reading register, input the Address in the box and click “Read” button.

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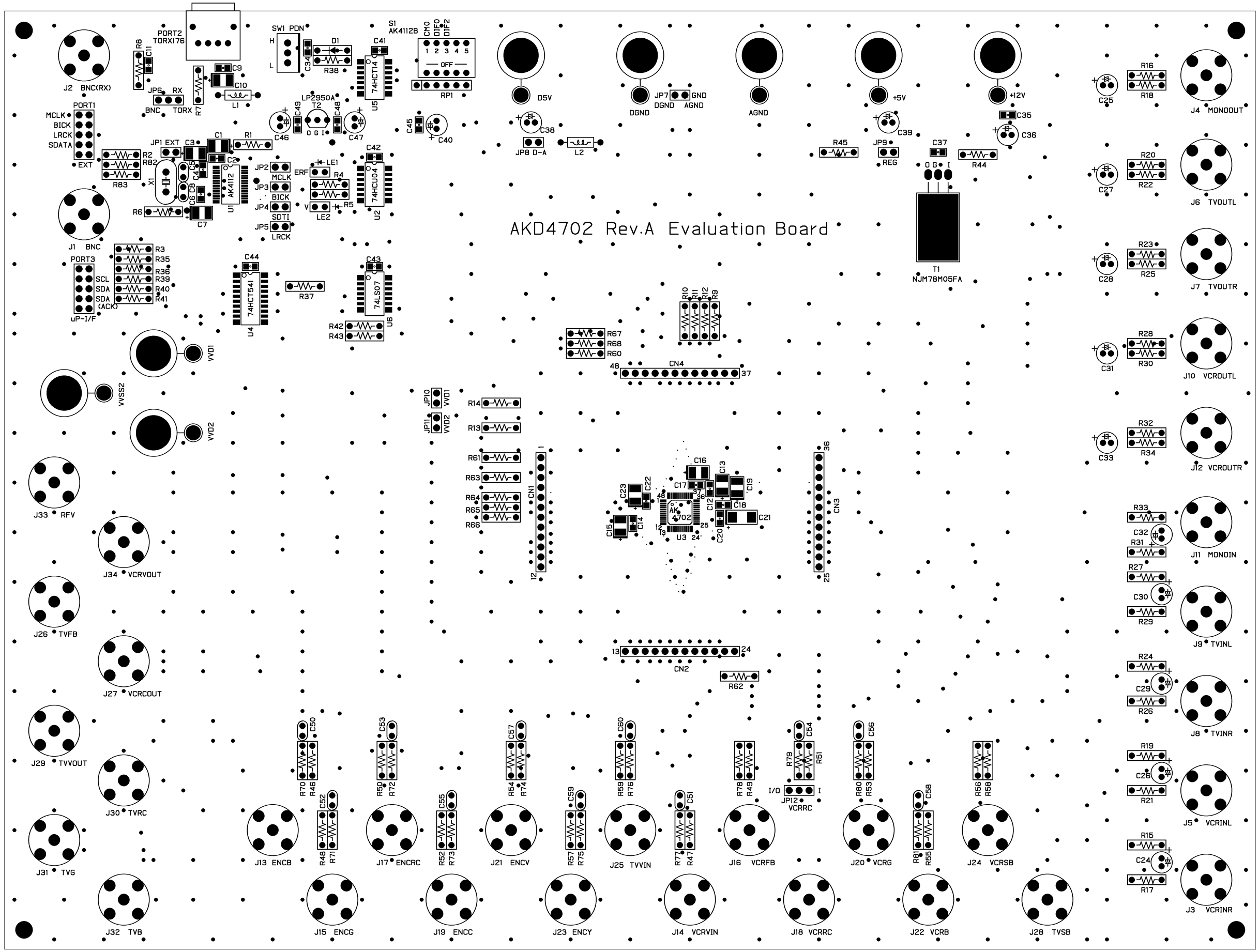
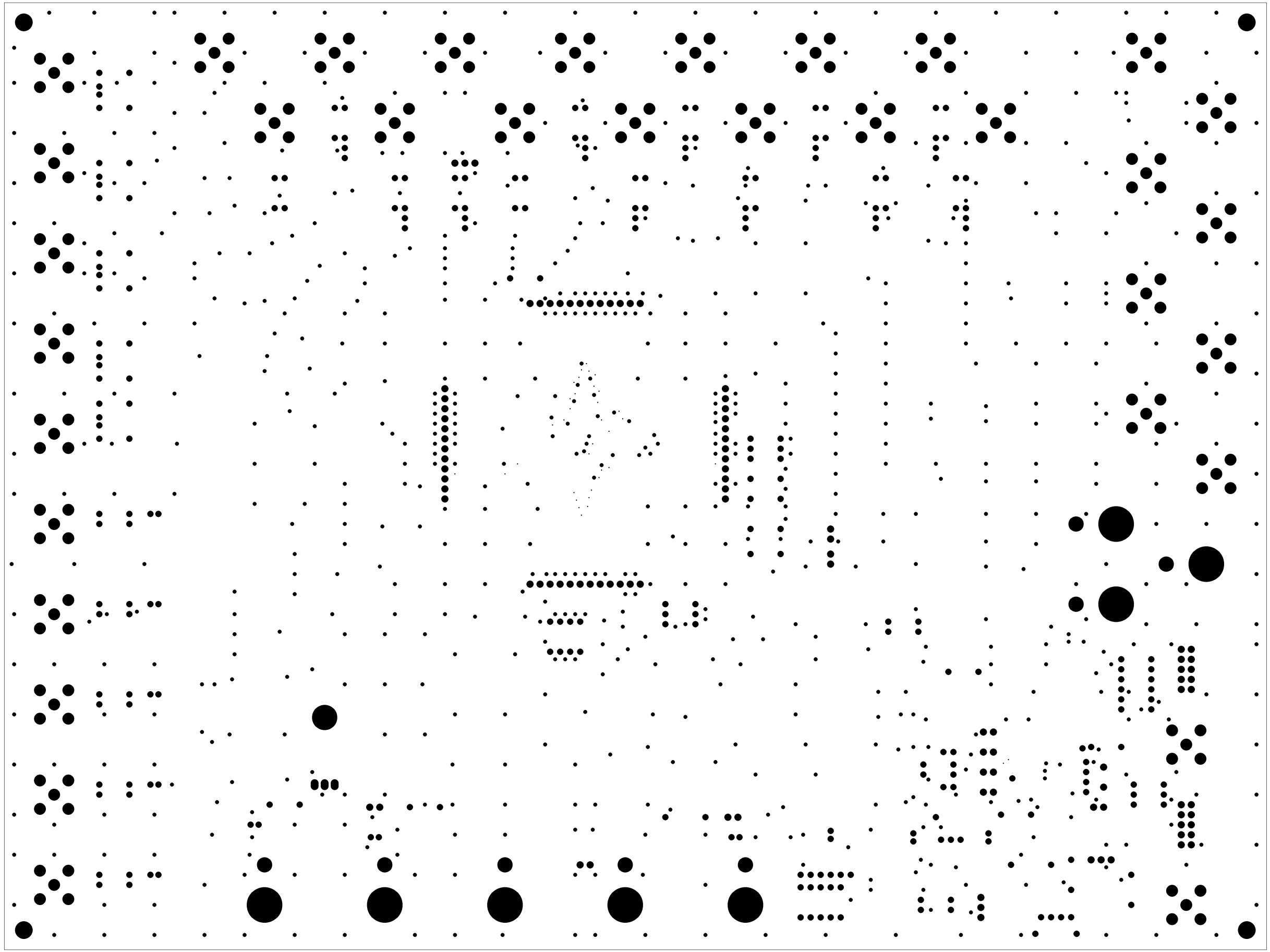
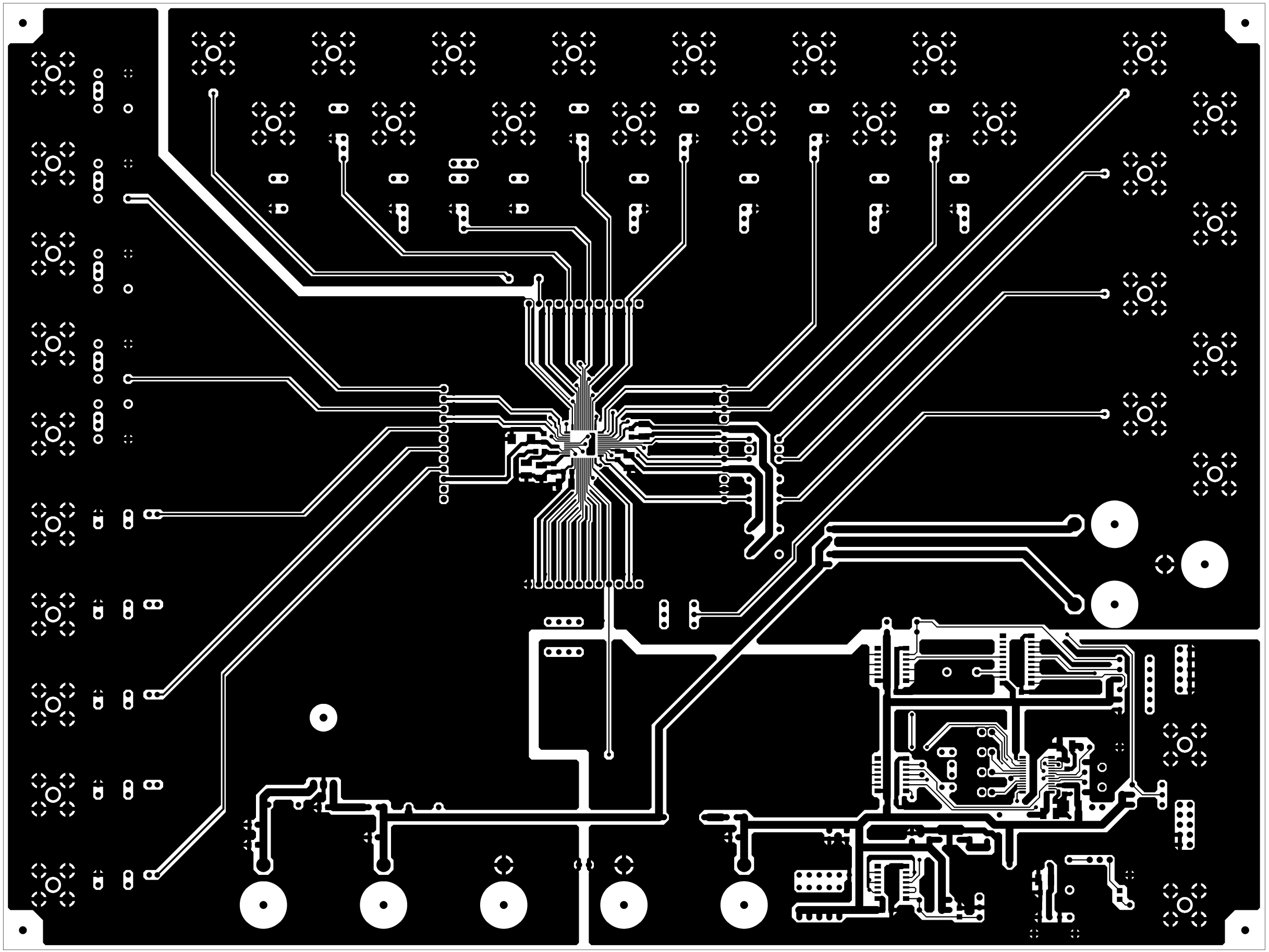
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.


AKD4702 Rev.A Evaluation Board
PORT2 TORX176
J2 BNC(RX)
PORT1
MCLK
BICK
LRCK
SDATA
EXT
J1 BNC
PORT3
uP-I/F
SCL
SDA
SDA (ACK)
SW1 PDN
S1 AK4112B
CM0
DIF0
DIF1
DIF2
OFF
RP1
LP2950A
T2
74HCT14
74HCU04
74HCT541
74LS07
AK4112
AK4702
U1
U2
U3
U4
U5
U6
D5V
DGND
AGND
+5V
+12V
JP7 DGND AGND
JP8 D-A
JP9 REG
T1
NJM78M05FA
J4 MONOOUT
J6 TVOUTL
J7 TVOUTR
J10 VCROUTL
J12 VCROUTR
J11 MONOIN
J9 TVINL
J8 TVINR
J5 VCRINL
J3 VCRINR
VVD1
VVD2
VSS2
CN1
CN2
CN3
CN4
J33 RFV
J34 VCRVOUT
J26 TVFB
J27 VCRCOUT
J29 TVVOUT
J30 TVRC
J31 TVG
J32 TVB
J13 ENCB
J15 ENCG
J17 ENCRC
J19 ENCC
J21 ENCV
J23 ENCY
J25 TVVIN
J14 VCRVIN
J16 VCRFB
J18 VCRRC
J20 VCRG
J22 VCRB
J24 VCRSB
J28 TVSB
JP12 VCRRC

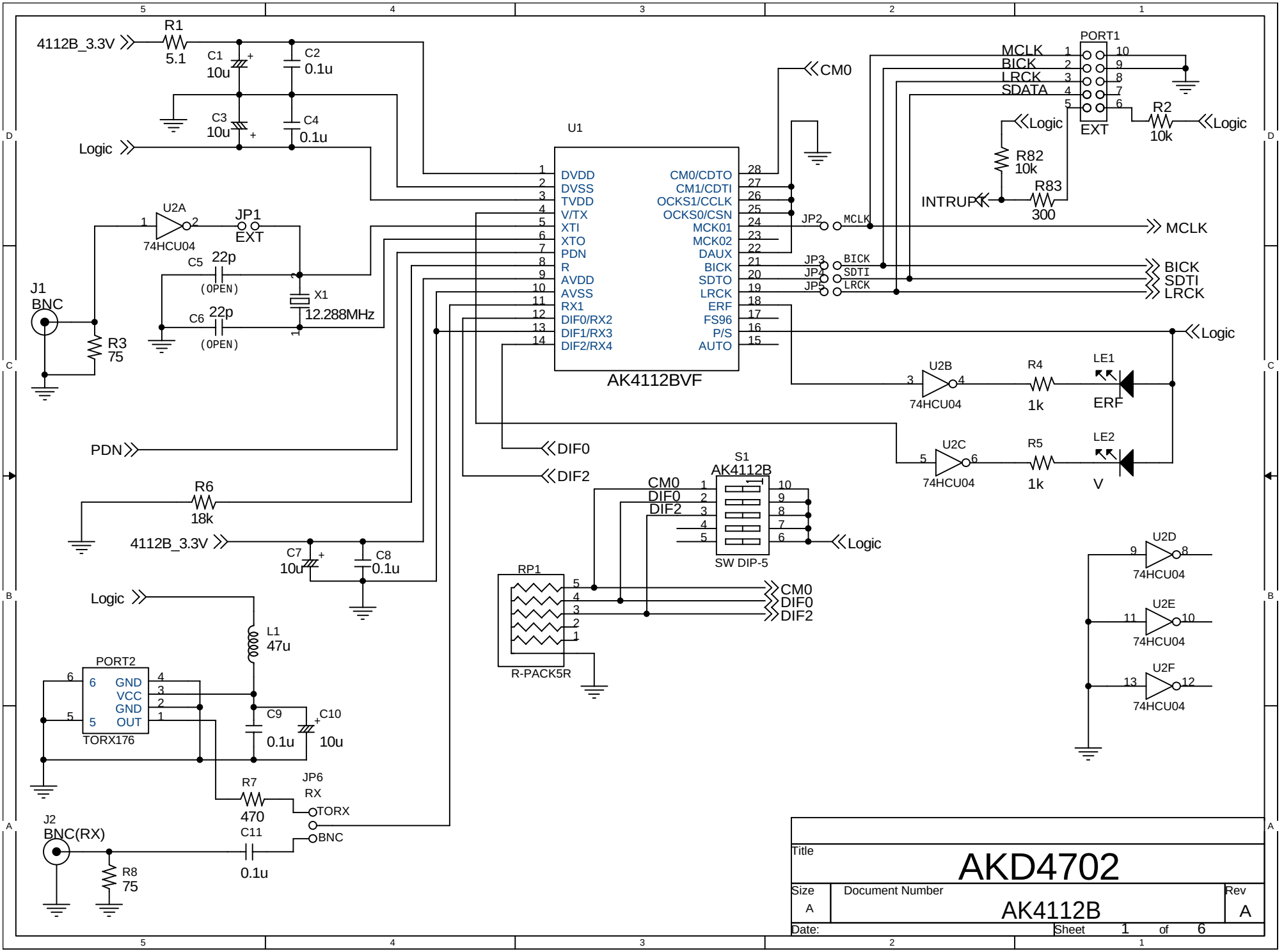
L1 SRSILK

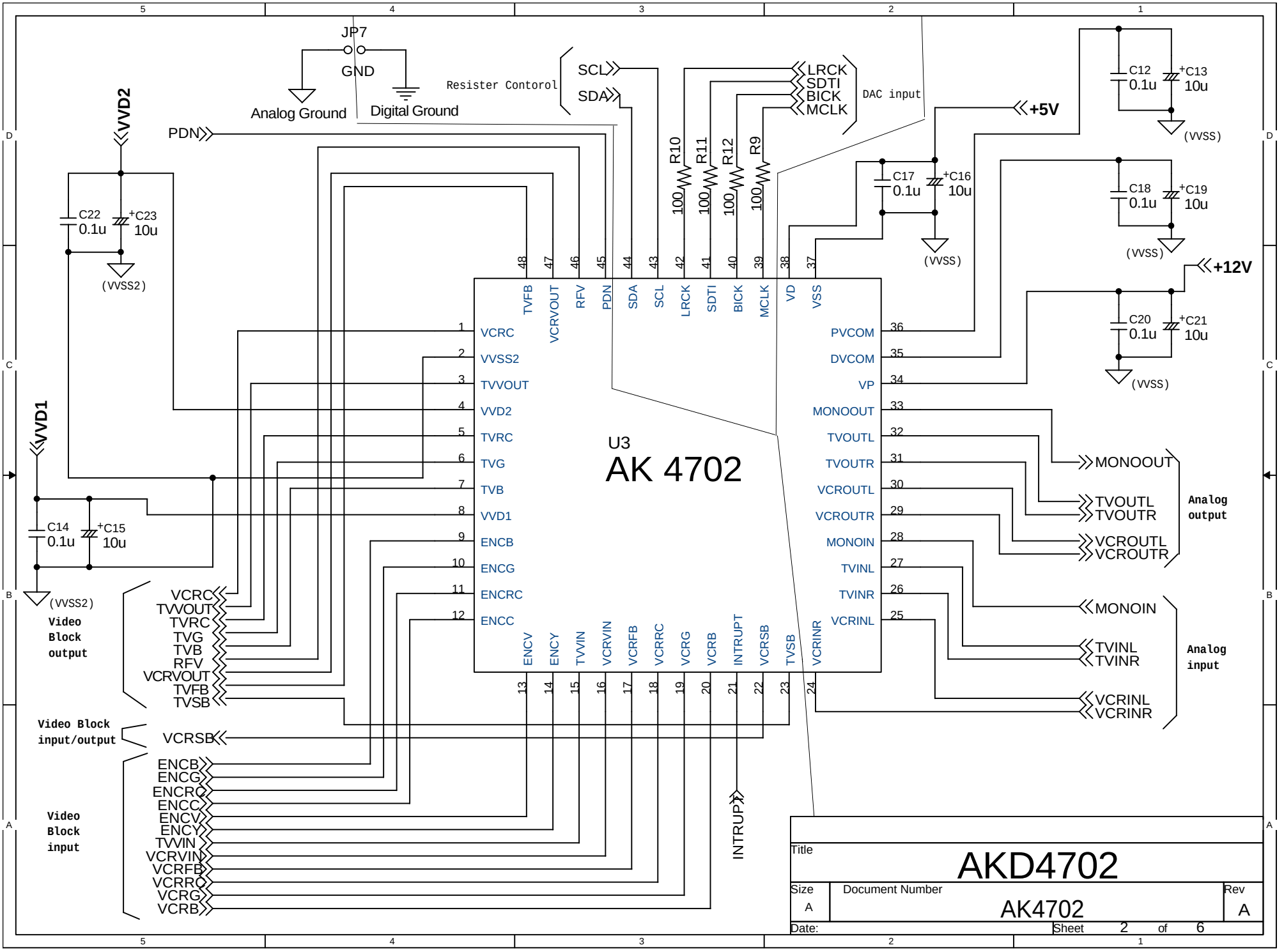
L2 SR

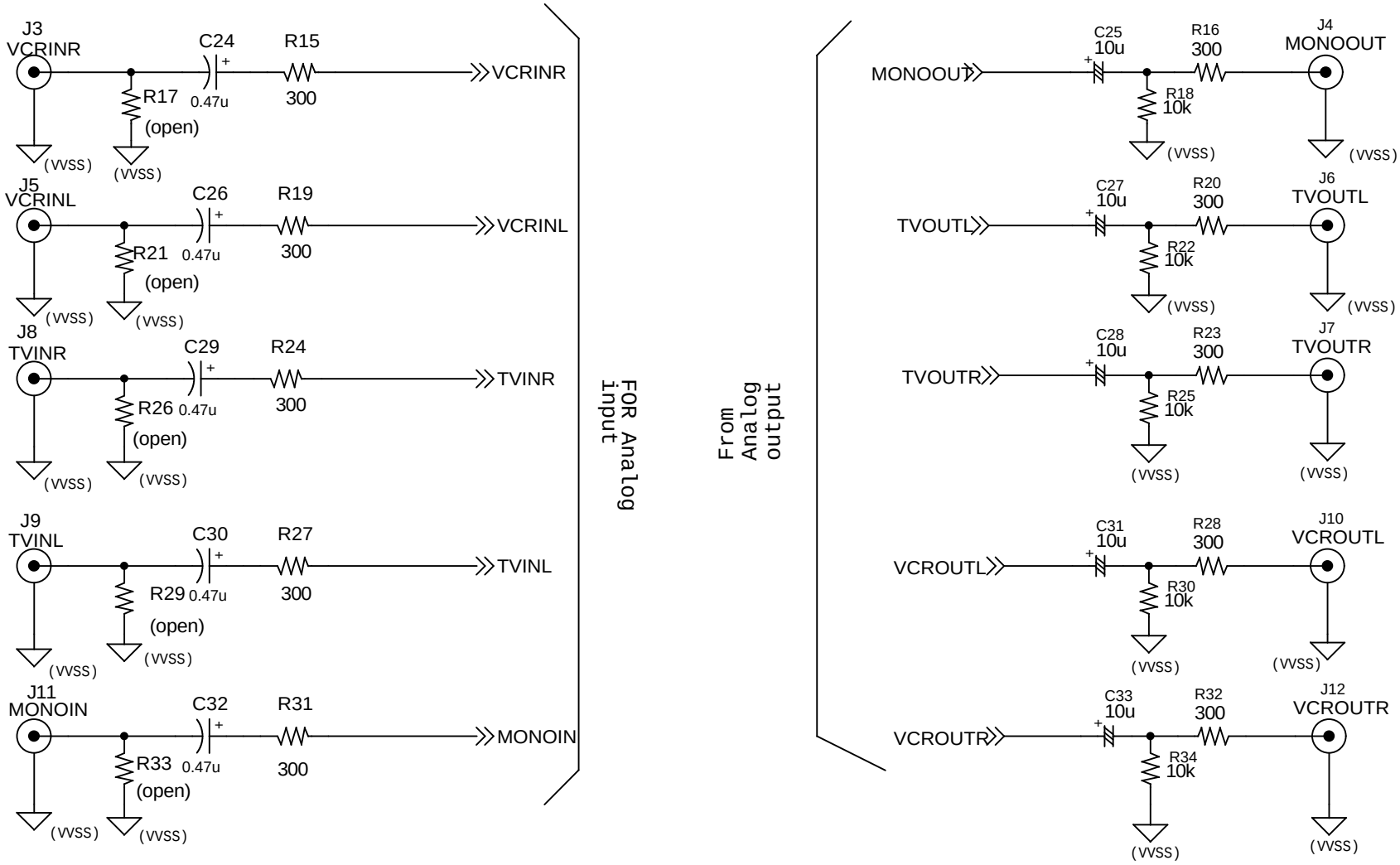




L2 ١٤٥-٧


4112B_3.3V
R1
5.1
C1
10u
C2
0.1u
C3
10u
C4
0.1u
Logic
U1
AK4112BVF
DVDD
DVSS
TVDD
V/TX
XTI
XTO
PDN
R
AVDD
AVSS
RX1
DIF0/RX2
DIF1/RX3
DIF2/RX4
CM0/CDTO
CM1/CDTI
OCKS1/CCLK
OCKS0/CSN
MCK01
MCK02
DAUX
BICK
SDTO
LRCK
ERF
FS96
P/S
AUTO
CM0
PORT1
MCLK
BICK
LRCK
SDATA
EXT
R2
10k
Logic
R82
10k
INTRUPT
R83
300
JP2
MCLK
JP3
BICK
JP4
SDTI
JP5
LRCK
U2A
74HCU04
JP1
EXT
C5
22p
(OPEN)
C6
22p
(OPEN)
X1
12.288MHz
J1
BNC
R3
75
U2B
74HCU04
R4
1k
LE1
ERF
U2C
74HCU04
R5
1k
LE2
V
PDN
DIF0
DIF2
S1
AK4112B
SW DIP-5
RP1
R-PACK5R
R6
18k
C7
10u
C8
0.1u
L1
47u
PORT2
TORX176
GND
VCC
OUT
C9
0.1u
C10
10u
R7
470
JP6
RX
TORX
BNC
J2
BNC(RX)
C11
0.1u
R8
75
U2D
74HCU04
U2E
74HCU04
U2F
74HCU04
Title
AKD4702
Size
A
Document Number
AK4112B
Rev
A
Date:
Sheet 1 of 6


JP7
GND
Analog Ground
Digital Ground
Resister Contorol
SCL
SDA
LRCK
SDTI
BICK
MCLK
DAC input
+5V
+12V
VVD2
VVD1
PDN
C22 0.1u
C23 10u
C14 0.1u
C15 10u
C12 0.1u
C13 10u
C17 0.1u
C16 10u
C18 0.1u
C19 10u
C20 0.1u
C21 10u
(VVSS)
(VVSS2)
R10 100
R11 100
R12 100
R9 100
U3
AK 4702
1 VCRC
2 VVSS2
3 TVVOUT
4 VVD2
5 TVRC
6 TVG
7 TVB
8 VVD1
9 ENCB
10 ENCG
11 ENCRC
12 ENCC
13 ENCV
14 ENCY
15 TVVIN
16 VCRVIN
17 VCRFB
18 VCRRC
19 VCRG
20 VCRB
21 INTRUPT
22 VCRSB
23 TVSB
24 VCRINR
25 VCRINL
26 TVINR
27 TVINL
28 MONOIN
29 VCROUTR
30 VCROUTL
31 TVOUTR
32 TVOUTL
33 MONOOUT
34 VP
35 DVCOM
36 PVCOM
37 VSS
38 VD
39 MCLK
40 BICK
41 SDTI
42 LRCK
43 SCL
44 SDA
45 PDN
46 RFV
47 VCRVOUT
48 TVFB
MONOOUT
TVOUTL
TVOUTR
VCROUTL
VCROUTR
Analog output
MONOIN
TVINL
TVINR
VCRINL
VCRINR
Analog input
VCRC
TVVOUT
TVRC
TVG
TVB
RFV
VCRVOUT
TVFB
TVSB
Video Block output
Video Block input/output
VCRSB
ENCB
ENCG
ENCRC
ENCC
ENCV
ENCY
TVVIN
VCRVIN
VCRFB
VCRRC
VCRG
VCRB
Video Block input
INTRUPT
Title
AKD4702
Size
A
Document Number
AK4702
Rev
A
Date:
Sheet 2 of 6



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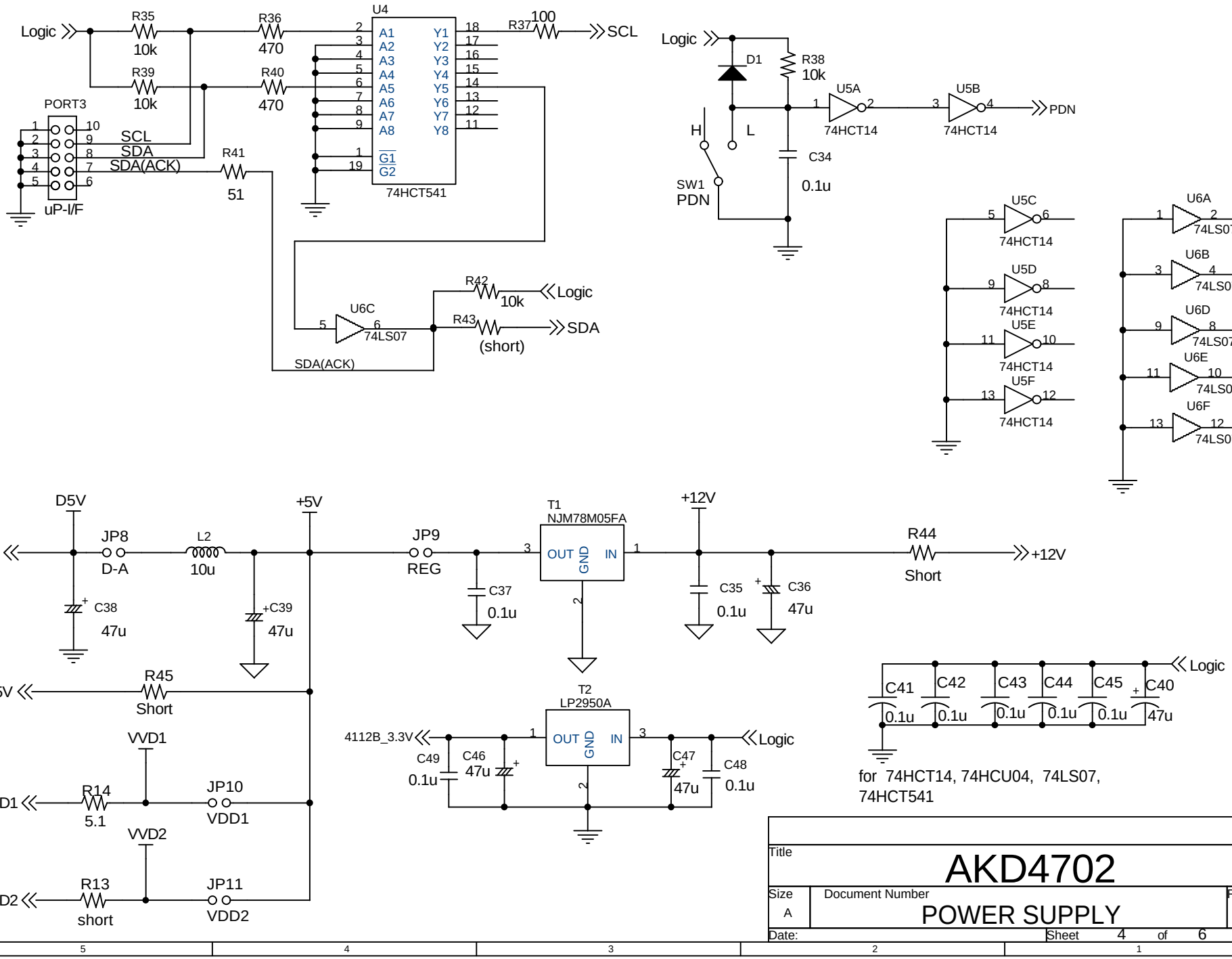
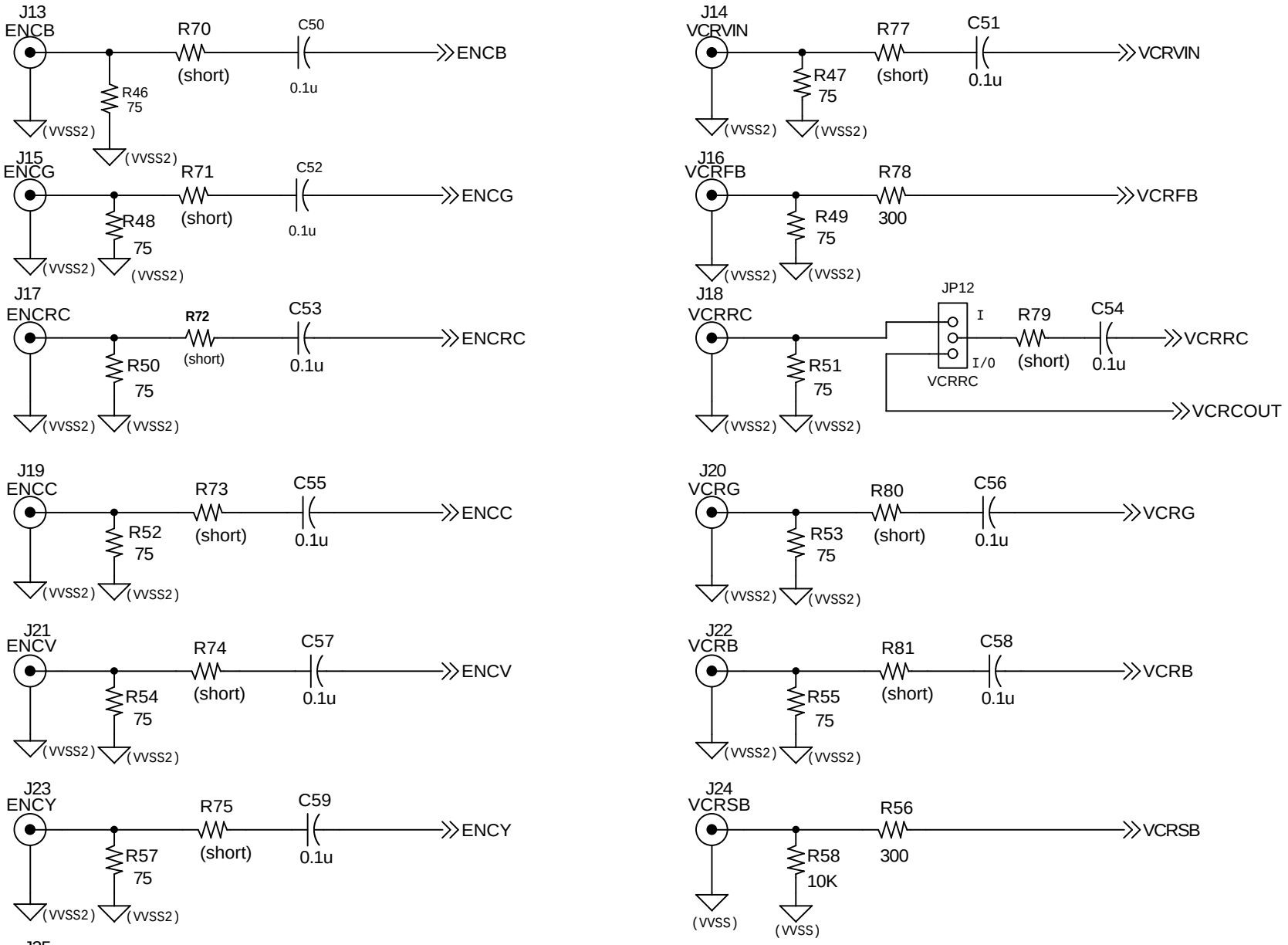
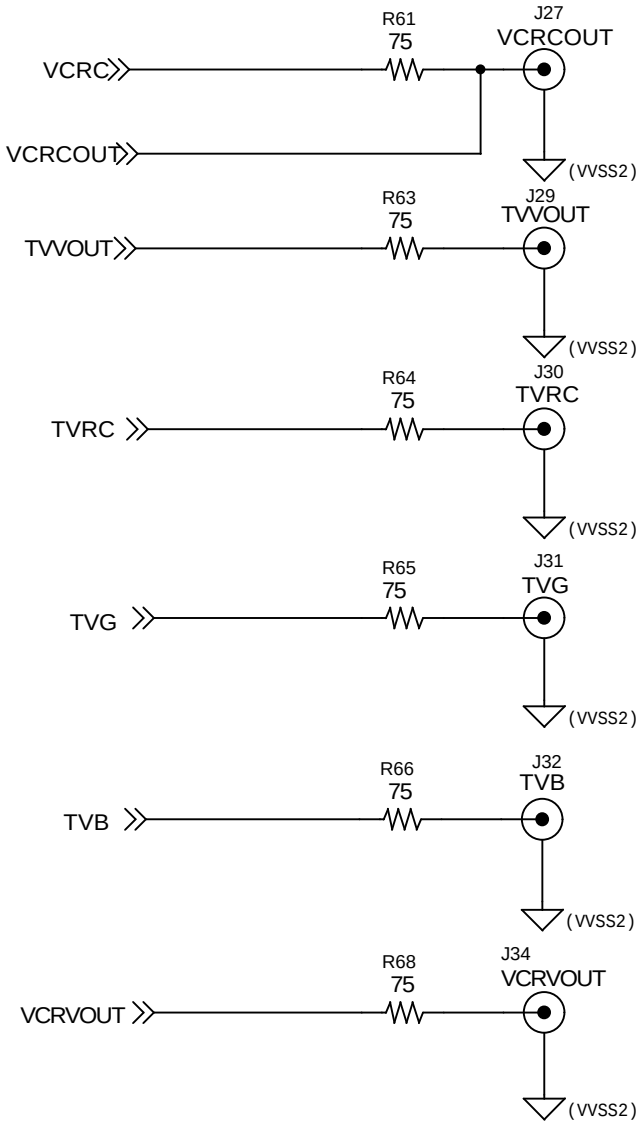
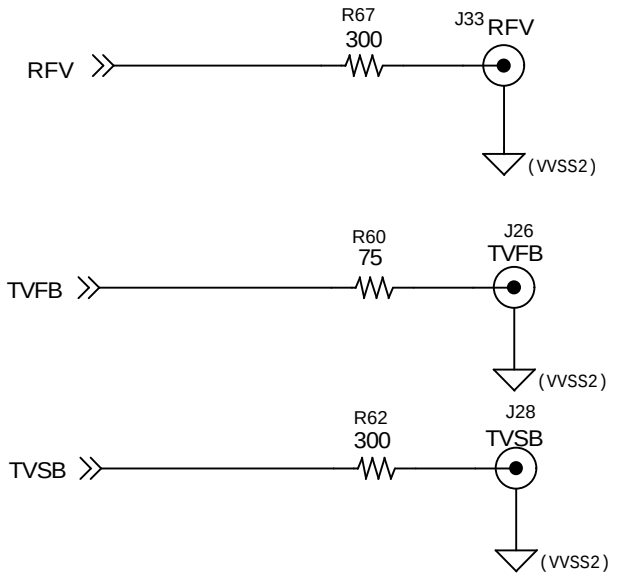
Size: A	Document Number: Analog Input/Output Circuit	Rev: A
Date: Friday, April 11, 2003	Sheet 3 of 6	


Logic
R35
10k
R36
470
R37
100
SCL
R39
10k
R40
470
U4
A1 A2 A3 A4 A5 A6 A7 A8
Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8
G1 G2
74HCT541
PORT3
uP-I/F
SCL
SDA
SDA(ACK)
R41
51
U6C
74LS07
R42
10k
R43
(short)
SDA
SDA(ACK)
Logic
D1
R38
10k
U5A
74HCT14
U5B
74HCT14
PDN
H
L
C34
0.1u
SW1
PDN
U5C
U5D
U5E
U5F
74HCT14
U6A
U6B
U6D
U6E
U6F
74LS07
D5V
+5V
Logic
JP8
D-A
L2
10u
C38
47u
+C39
47u
JP9
REG
T1
NJM78M05FA
OUT GND IN
C37
0.1u
+12V
C35
0.1u
C36
47u
R44
Short
+12V
+5V
R45
Short
VVD1
R14
5.1
JP10
VDD1
VVD2
R13
short
JP11
VDD2
4112B_3.3V
T2
LP2950A
C49
0.1u
C46
47u
C47
47u
C48
0.1u
Logic
C41
C42
C43
C44
C45
C40
0.1u
47u
Logic
for 74HCT14, 74HCU04, 74LS07,
74HCT541
Title
AKD4702
Size
A
Document Number
POWER SUPPLY
Rev
A
Date:
Sheet 4 of 6



Title	AKD4702	
Size: A	Document Number: Video Block Input Circuit	Rev: A
Date:	Sheet 5 of 6	





Title	AKD4702	
Size: A	Document Number: Video Block Output Circuit	Rev: A
Date:	Sheet 6 of 6	