Ordering number : ENA0466

SANYO Semiconductors
DATA SHEET

Bi-CMOS LSI

LV24010LP — Compact Portable Equipment 1-Chip FM+RDS Tuner IC

Overview

The LV24010LP is single-chip FM radio with RDS tuner IC that requires absolutely no external components. This design was achieved by combining Sanyo BiCMOS process technology, Sanyo packaging technology, and filtering circuit technology developed by Semiconductor Ideas to the Market (ItoM) B.V.

Functions

- FM FE.
- FM IF.
- MPX stereo decoder.
- Tuning.
- Standby.
- RDS.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage	V_{CC} max	Analog block supply voltage	5.0	V
	V_{DD} max	Digital block supply voltage	4.5	V
Maximum input voltage	$V_{IN}1$ max	Clock, Data, NR-W	V_{DD}+0.3	V
	$V_{IN}2$ max	Extenal_clk_in	V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta≤70°C *	140	mW
Storage temperature	Tstg		-40 to +125	°C
Operating temperature	Topr		-20 to +70	°C

*: With 40 × 50× 0.8mm^3, glass epoxy substrate

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	unit
Recommended supply voltage	V_{CC}	Analog block supply voltage	3.0	V
	V_{DD}	Digital block supply voltage	3.0	V
Operating supply voltage range	$V_{CC\ op}$		2.7 to 5.0	V
	$V_{DD\ op}$		2.5 to 4.0	V
	$V_{IO\ op}$	Interface voltage	1.8 to 4.0	V

Note: The application voltage of V_{IO} to be used must be either equal to V_{DD} or the V_{DD} value or less ($V_{IO} \leq V_{DD}$).

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Electrical Characteristics at Ta = 25°C, V_{CC} = 3.0V, V_{DD} = 3.0V, in the measuring circuit specified, Soft Mute/Stereo = off

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Current drain (in operation)	$I_{CC}A$	Measurement at pin 23 with 60 dBμ input in the analog block, Monaural input		15	19	mA
	$I_{CC}D$	Measurement at pins 27 and 40 with 60 dBμ input in the digital block	0.2	0.4	0.8	mA
Current drain (in standby)	$I_{CC}A$	Measurement at pin 23 in the standby mode of the analog block		3	30	μA
	$I_{CC}D$	Measurement at pins 27 and 40 in the standby mode of the digital block.		3	30	μA
FM receive band	F_range		76		108	MHz
FM receive characteristics;MONO: fc = 80MHz,fm = 1kHz, 22.5kHzdev. Note that Soft_stereo,Soft_and mute functions are OFF.						
3dB sensitivity	-3dB LS	60dBμV, 22.5kHzdev output standard, -3dB input -3dB.		13	20	dBμV EMF
Practical sensitivity 1	QS1	Input level with S/N = 30dB, Deemphasis = 75μs SG open display		10	17	dBμV EMF
Practical sensitivity 2 (Reference)	QS2	Input level with S/N = 26dB, Deemphasis = 75μs, SG terminal display		1.25		μV
Demodulation output	Vo	60dBμV, pin 11 output	50	70	110	mV
Channel balance	CB	60dBμV, pin 11 output / pin 12 output	-2	0	2	dB
Signal-to-noise ratio	S/N	60dBμV, pin 11 output	48	58		dB
Total harmonic distortion 1(MONO)	THD1	60dBμV, pin 11 output, 22.5kHdev		0.4	1.5	%
Total harmonic distortion 2(MONO)	THD2	60dBμV, pin 11 output, 75kHdev		1.3	3	%
Field intensity display level	FS	Input level at which FS1 changes to FS2	6	16	26	dBμ
Mute attenuation	Mute-Att	60dBμV, pin 11 output	60	70		dB
FM receive characteristics; STEREO: fc = 80MHz, fm = 1kHz, V_{IN} = 60dBμV, L+R = 30% (22.5kHz), Pilot = 10% (7.5kHzdev)						
Separation	SEP	L-mod, pin 11 output / pin 12 output	20	35		dB
Total harmonic distortion (Main)	THD-ST	Main-mod (for L+R input), pin 11 / pin 12 output, IHF_BPF		0.6	1.8	%
RDS characteristics						
RDS_center frequency	f_{cen}	Adjustment accuracy of RDS_VCO DAC value. (Adjustment accuracy of free_run frequency)	56.5	57.0	57.5	kHz
-3dB bandwidth	BW-3dB	Bandwidth of BPF to 57KHZ Center frequency. Set Block4 register 06h of Bit3-2 (RDSBW) to “11” ( ) is not guarantee value. Just for Reference value	(3.0)	5.5	(7.0)	kHz
RDS Current drain	I_{rds}	RDS current value at RDS Enable/Disable		2	4	mA

The output level is set to the VOL = 14 when the block 2, register 09h of control register map has the bit 3,2,1,0 = “0010”
In other cases:

- The IF_OSC frequency must be adjust to 140kHz with DAC of block 1, register 05h.
- The IF_CENTER set bit value (block 2, register 03h) applies to same DAC value of IF_OSC.
- The IF_BW set bit value (block2, register 05h) applies to the setting of the value 65% of the IF_OSC set bit value.
- The RDS_OSC frequency must be adjust to 114kHz with DAC of block 4, register 07h.
- The RDS_FLTDAC (block 4, register 03h) set bit value applies to the setting of value 95% of RDS_OSC set bit value.

Interface Block Allowable Operation Range at Ta = -20 to +70°C, V_{SS} = 0V

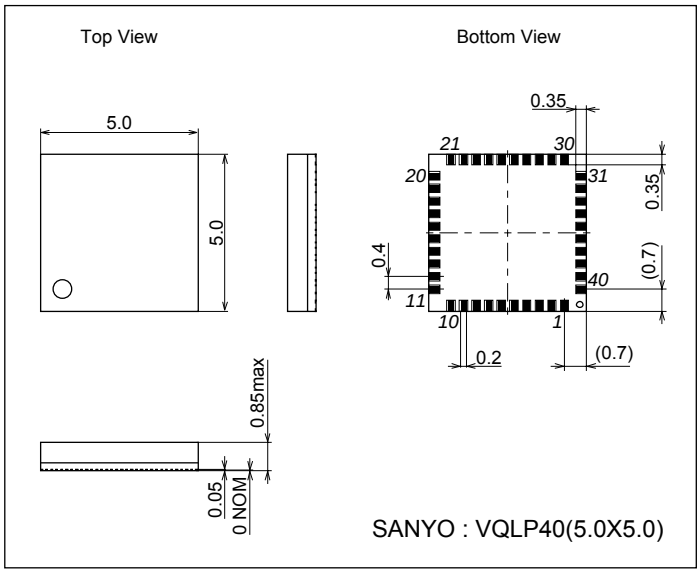
Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Supply voltage	V_{DD}		2.5		4.0	V
Digital block input	V_{IH}	High-level input voltage range	$0.7V_{DD}$		V_{DD}	V
	V_{IL}	Low-level input voltage range	0		0.6	V
Digital block output	I_{OL}	Output current at Low level	2.0			mA
	V_{OL}	Output voltage at Low level I_{OL} = 2mA			0.6	V
Clock input operating frequency	fclk	(Pin 29) clock frequency for 3wire_bus			0.7	MHz
External clock operating frequency	fclk_ext	(Pin 31) clock frequency for external input	32k		14M	Hz

Note: External clock input (pin 31) allows also input of the sine wave signal.

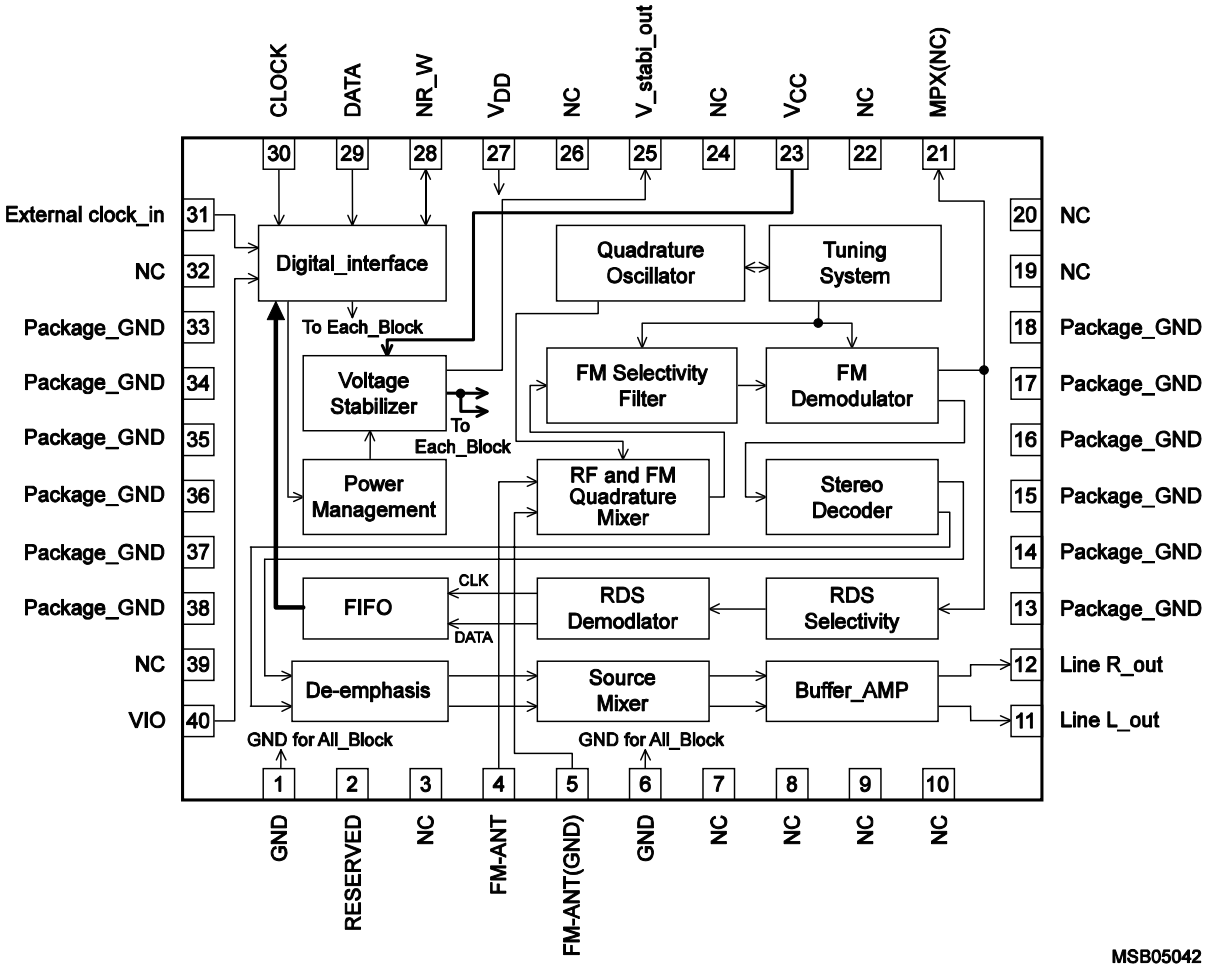
Package Dimensions

unit : mm

3302A



Block Diagram

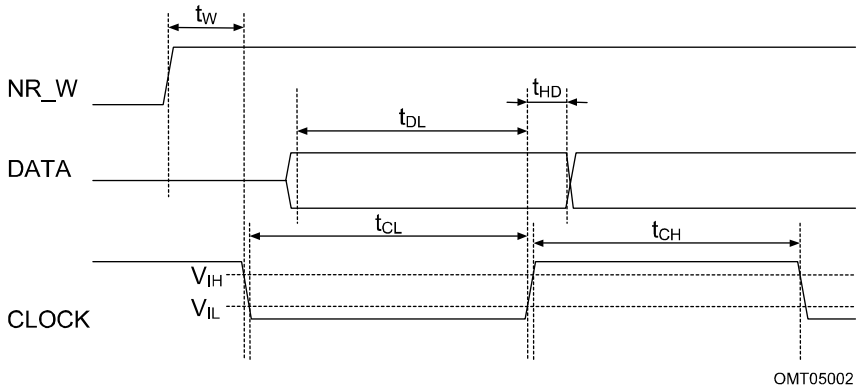


Pin Function

Pin No.	Pin name	Description	DC_bias	Remark
1	GND	GND (Analog and Digital GND)		
2	NC			Do not connect.
3	NC			Do not connect.
4	FM-ANT1	Antenna input		
5	FM-ANT2	Antenna GND		Connect to GND.
6	GND	GND (Analog and Digital GND)		
7	NC			Do not connect.
8	NC			Do not connect.
9	NC			Do not connect.
10	NC			Do not connect.
11	LINE-OUT-L	Radio Lch Line-output	1.2V	
12	LINE-OUT-R	Radio Rch Line-output	1.2V	
13	Package-GND	GND for Package-shied		
14	Package-GND	GND for Package-shied		
15	Package-GND	GND for Package-shied		
16	Package-GND	GND for Package-shied		
17	Package-GND	GND for Package-shied		
18	Package-GND	GND for Package-shied		
19	NC			Do not connect.
20	NC			Do not connect.
21	MPX	MPX-signal output	V_{CC}-0.3V	
22	NC			Do not connect.
23	V_{CC}	Analog supply voltage		
24	NC			Do not connect.
25	Vstabi.	Stabilizer voltage	2.7V	
26	NC			Do not connect.
27	V_{DD}	Digital supply voltage		
28	NR_W	Digital interface Read/Write		
29	DATA	Digital interface DATA		
30	CLOCK	Digital interface Clock		
31	CLK_IN	Reference clock-source input for measurement		Connect to GND if not used.
32	NC			Do not connect.
33	Package-GND	GND for Package-shied		
34	Package-GND	GND for Package-shied		
35	Package-GND	GND for Package-shied		
36	Package-GND	GND for Package-shied		
37	Package-GND	GND for Package-shied		
38	Package-GND	GND for Package-shied		
39	NC			Do not connect.
40	VI/O	Digital interface supply voltage		

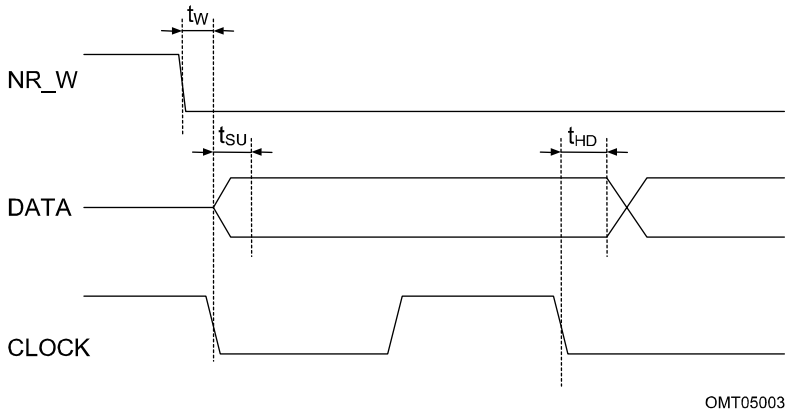
Timing Diagram

Write timing



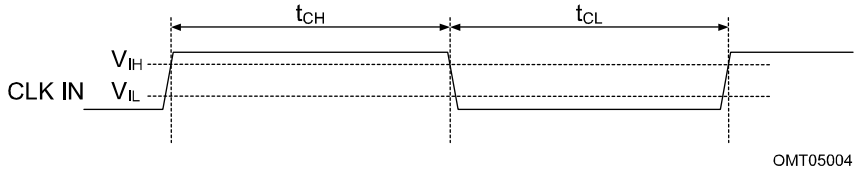
Symbol	Parameter	Ratings			unit
		min	typ	max	
t_W	Delay from command to data	750			ns
t_{DL}	Delay from data stable to data latch time	750			ns
t_{HD}	Data Hold time	750			ns
t_{CH}	Clock High-level time	750			ns
t_{CL}	Clock Low-level time	750			ns

Read timing



Symbol	Parameter	Ratings			unit
		min	typ	max	
t_W	Delay from command to 1st data bit	350			ns
t_{SU}	Data Setup time			350	ns
T_{HD}	Data hold time			350	ns

External clock timing (Pin 31)



Symbol	Parameter	Ratings			unit
		min	typ	max	
t_{CH}	Clock High-level time	35			ns
t_{CL}	Clock Low-level time	35			ns

Digital interface specification (Interface specification: reference)

(1) 3-wire bus (For communication line)

Access to the LV24010 is done through the 3-wire bus:

CLOCK Data strobe, input to the LV24010

NR_W Command (Write or read data), input to the LV24010

DATA Bi-directional pin: input to the LV24010 when NR_W is high, output from the LV24010 when NR_W is low.

The LV24010 can be configured to generate interrupt through the DATA-line. When interrupt mode is selected, care should be taken that the DATA-line connection to the application micro-controller also supports interrupt.

When the required timing window for frequency measurements is not generated by the application micro-controller, an external clock must be connected to CLK_IN pin of the LV24010

(2) Register map (For register map)

The LV24020 registers are divided in 2 blocks:

Block 01h	Status and measurement
Block 02h	Radio Control
Block 04h	RDS control

To access a register in a block, the block must be first selected by writing the block number to the BLK_SEL register. Block selection can be skipped for subsequent accesses to other registers in the same block.

The mapping is as follows:

Block	Address	Register name	Access	Operation
01h	00h	CHIP_ID	R	Chip identification
	01h	BLK_SEL	W	Block Select
	02h	MSRC_SEL	W	Measure source select
	03h	FM_OSC	W	DAC control for FM-RF oscillator
	04h	SD_OSC	W	DAC control for stereo decoder oscillator
	05h	IF_OSC	W	DAC control for IF oscillator
	06h	CNT_CTRL	W	Counter control
	07h	NA	-	
	08h	IRQ_MSK	W	Interrupt mask
	09h	FM_CAP	W	CAP bank control for RF-frequency
	0Ah	CNT_L	R	Counter value low byte
	0Bh	CNT_H	R	Counter value high byte
	0Ch	CTRL_STAT	R	Control status
	0Dh	RADIO_STAT	R	Radio station status
	0Eh	IRQ_ID	R	Interrupt identify
	0Fh	IRQ_OUT	W	Set Interrupt on DATA-line
02h	01h	BLK_SEL	W	Access register 01h of block 1
	02h	RADIO_CTRL1	W	Radio control 1
	03h	IF_CENTER	W	IF Center Frequency
	04h	NA	W	
	05h	IF_BW	W	IF Bandwidth
	06h	RADIO_CTRL2	W	Radio Control 2
	07h	RADIO_CTRL3	W	Radio control 3
	08h	STEREO_CTRL	W	Stereo Control
	09h	AUDIO_CTRL1	W	Audio Control 1
	0Ah	AUDIO_CTRL2	W	Audio Control 1
	0Bh	PW_SCTRL	W	Power and soft control
04h	01h	BLK_SEL	W	Access register 01h of block 1
	03h	RDS_FLTDAC	W	DAC control for RDS filter
	04h	RDAT_L	R	Demodulated RDS data - low byte
	05h	RDAT_H	R	Demodulated RDS data – high byte
	06h	RDS_CTRL	W	RDS control
	07h	RDS_OSC	W	DAC control for RDS PLL oscillator
	08h	NA	-	
	09h	RDS_INPS	W	RDS input setting

Registers with blank colum are not defined and should not be accessed.

(3) Register description (For each register content)

Block x, Register 01h - BLK_SEL - Block Select register (Write Only)

7	6	5	4	3	2	1	0
BN[7:0]							

bit 7-0: **BN[7:0]:** 8-bit block number. For LV24010, the following numbers are valid:
01h.
02h.
04h.

Note: This register can be accessed from any block.

Block 1, Register 00h - CHIP_ID - Chip identify register (Read Only)

7	6	5	4	3	2	1	0
ID[7:0]							

bit 7-0: **ID[7:0]:** 8-bit chip ID. The following ID's are defined:
0Bh for LV24010.

Block 1, Register 02h - MSRC_SEL - Measurement Source Select Register (Write-only)

7	6	5	4	3	2	1	0
MSR_O	AFC_LVL	AFC_SPD	Reserved	Reserved	MSS_SD	MSS_FM	MSS_IF

bit 7: **MSR_O:** Output measure source to DATA-pin.
0 = Measuring source not available at DATA-pin (normal operation).
1 = Measuring source available at DATA-pin (test mode).

bit 6: **AFC_LVL:** AFC trigger level.
0 = AFC is always active (trigger at 0dBμV).
1 = AFC is only active when field strength is above 20dBμV.

bit 5: **AFC_SPD:** AFC speed.
0 = AFC adjusts with 3Hz speed.
1 = AFC adjusts with 8kHz speed (test mode).

bit 4: **Reserved:** Must be programmed with 0.

bit 3: **Reserved:** Must be programmed with 0.

bit 2: **MSS_SD:** Stereo decoder oscillator measurement.
0 = Disable stereo decoder oscillator measurement.
1 = Enable stereo decoder oscillator measurement.

bit 1: **MSS_FM:** FM RF oscillator measurement.
0 = Disable FM RF oscillator measurement.
1 = Enable FM RF oscillator measurement.

bit 0: **MSS_IF:** IF oscillator measurement.
0 = Disable IF oscillator measurement.
1 = Enable IF oscillator measurement.

Note:
- Only one of the measurement source MSS_xx bits may be set at a time.
- The FM RF frequency is divided by 256 before it goes to the measuring circuitry.

Block 1, Register 03h - FM_OSC - FM RF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
FMOSC[7:0]							

bit 7-0: **FMOSC[7:0]:** DAC value to control the FM RF oscillator (fine step)

Note:
- Positive DAC control (i.e. the frequency increases with the register's value).
- See also FM_CAP register.

Block 1, Register 04h - SD_OSC - Stereo Decoder Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
SDOSC[7:0]							

bit 7-0: **SDOSC[7:0]:** DAC value to control the stereo decoder oscillator.

Note: Positive DAC control (i.e. the frequency increases with the register's value)

Block 1, Register 05h - IF_OSC - IF Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
IFOSC[7:0]							

bit 7-0: **IFOSC[7:0]:** DAC value to control the IF oscillator.

Note: Positive DAC control (i.e. the frequency increases with the register's value).

Block 1, Register 06h - CNT_CTRL - Counters Control Register (Write-only)

7	6	5	4	3	2	1	0
CNT1_CLR	CTAB2	CTAB1	CTAB0	SWP_CNT_L	CNT_EN	CNT_SEL	CNT_SET

bit 7: **CNT1_CLR:** Clear counter 1 bit.
0 = Normal mode.
1 = Clear and keep counter 1 in reset mode.

bit 6-4: **CTAB[2:0]:** Tab select for counter 2 measuring interval bits.

Value	Dec.	Stop value
000b	0	Stop after 2 counts.
001b	1	Stop after 8 counts .
010b	2	Stop after 32 counts.
011b	3	Stop after 128 counts.
100b	4	Stop after 512 counts.
101b	5	Stop after 2048 counts.
110b	6	Stop after 8192 counts.
111b	7	Stop after 32768 counts.

bit 3: **SWP_CNT_L:** Swap counter 1 and counter 2 bit (Active low).
0 = Clock source 1 to counter 2, clock source 2 to counter 1 (swapping)
1 = Clock source 1 to counter 1, clock source 2 to counter 2 (no swap)

bit 2: **CNT_EN:** Enable the currently selected counter bit.
0 = Disable counter (stop counting).
1 = Enable counter (counting mode).

bit 1: **CNT_SEL:** counter select bit.
0 = Select counter 1 for measurement.
1 = Select counter 2 for measurement.

bit 0: **CNT_SET:** Set counters bit.
0 = Normal mode.
1 = Set both counter 1 and counter 2 to FFFFh and keep them set.

Block 1, Register 08h - IRQ_MSK - Interrupt Mask Register (Write-only)

7	6	5	4	3	2	1	0
Reserved	IM_MS	Reserved	Reserved	IRQ_LVL	IM_AFC	IM_FS	IM_CNT2

bit 7: **Reserved:** Must be programmed with 0.

bit 6: **IM_MS:** Mono/Stereo interrupt mask bit.
0 = Disable mono/stereo change interrupt.
1 = Enable mono/stereo change interrupt.

bit 5: **Reserved:** Must be programmed with 0.

bit 4: **Reserved:** Must be programmed with 0.

bit 3: **IRQ_LVL:** Interrupt level select bit.
0 = Drive DATA-line from low to high when interrupt occurs (active high).
1 = Drive DATA-line from high to low when interrupt occurs (active low).

bit 2: **IM_AFC:** AFC out of range interrupt mask bit.
0 = Disable AFC out of range interrupt.
1 = Enable AFC out of range interrupt.

bit 1: **IM_FS:** Field strength change interrupt mask bit.
0 = Disable field strength change interrupt.
1 = Enable field strength change interrupt.

bit 0: **IM_CNT2:** Counter 2 counting done interrupt mask bit.
0 = Disable counter 2 counting done interrupt.
1 = Enable counter 2 counting done interrupt.

Block 1, Register 09h - FM_CAP - FM RF Capacitor Bank Register (Write-only)

7	6	5	4	3	2	1	0
FMCAP[7:0]							

bit 7-0: **FMCAP[7:0]:** CAP bank value to control the FM RF frequency (coarse steps)

Note:
- 7½ bit CAP value (Bit[7:6]: Combination 10b and 01b results in the same CAP-range).
- Negative control: de RF frequency decreases when increasing the register's value.
- See also FM_OSC register.

Block 1, Register 0Ah - CNT_L - Counter Value Low Register (Read-only)

7	6	5	4	3	2	1	0
CNT_LSB[7:0]							

bit 7-0: **CNT_LSB[7:0]:** Lower 8-bit value of the 16 bit counter

Block 1, Register 0Bh - CNT_H - Counter Value High Register (Read-only)

7	6	5	4	3	2	1	0
CNT_MSB[7:0]							

bit 7-0: **CNT_MSB[7:0]:** Upper 8-bit value of the 16 bit counter

Block 1, Register 0Ch - CTRL_STAT - Control Status Register (Read-only)

7	6	5	4	3	2	1	0
REV3	REV2	REV1	REV0	Reserved	Reserved	COV_FLG	AFC_FLG

bit 7-4: **REV[3:0]:** should be read as 0Dh.

bit 3-1: **Reserved[1:0]:** should be read as all 1

bit 1: **COV_FLG:** counter overflow flag.
0 = No overflow of the internal counter.
1 = The last counting loop causes overflow of the internal counter.

bit 0: **AFC_FLG:** AFC out of range bit
0 = AFC is within control range.
1 = AFC is out of control range.

Note:
- Reading this register will clear AFC, count 2 done interrupt.
- COV_FLG is clear when CLR_CNT1 bit of CNT_CTRL register is high.

Block 1, Register 0Dh - RADIO_STAT - Radio Station Status Register (Read-only)

7	6	5	4	3	2	1	0
RSS_MS	RSS_FS						

bit 7: **RSS_MS:** Radio station mono/stereo state bit.
0 = Mono.
1 = Stereo.

bit 6-0: **RSS_FS[6:0]:** Radio station field strength bits.
1111111b = Field strength less then 10dBμV.
0111111b = Field strength between 10 to 20dBμV.
0011111b = Field strength between 20 to 30dBμV.
0001111b = Field strength between 30 to 40dBμV.
0000111b = Field strength between 40 to 50dBμV.
0000011b = Field strength between 50 to 60dBμV.
0000001b = Field strength between 60 to 70dBμV.
0000000b = Field strength above 70dBμV.

Note: Reading this register will clear field strength and mono/stereo interrupt.

Block 1, Register 0Eh - IRQ_ID - Interrupt Identify Register (Read-only)

7	6	5	4	3	2	1	0
Reserved	II_RDS	II_CNT2	Reserved	II_AFC	Reserved	Reserved	II_FS_MS

bit 7: **Reserved:** should be read as 1.

bit 6: **II_RDS:** RDS data available interrupt.
0 = No counting 2 counting done interrupt.
1 = Measuring with counter 2 is done.

bit 5: **II_CNT2:** Counter 2 counting done flag.
0 = No counting 2 counting done interrupt.
1 = Measuring with counter 2 is done.

bit 4: **Reserved:** should be read as 0.

bit 3: **II_AFC:** AFC out of range interrupt bit.
0 = No AFC interrupt.
1 = AFC fails to hold the RF-frequency in range.

bit 2: **Reserved:** should be read as 0.

bit 1: **Reserved:** should be read as 0.

bit 0: **II_FS_MS:** Field strength and Mono/stereo interrupt bit.
0 = No change in either the field strength or the mono/stereo mode.
1 = Change in field strength bits detected or mono/stereo mode has changed.

Block 1, Register 0Fh - IRQ_OUT - Set Interrupt Out Register (Write Only)

7	6	5	4	3	2	1	0
IRQO_VAL[7:0]							

bit 7-0: **IRQO_VAL[7:0]:** Write any value to this register will select the interrupt as output on the DATA-line of the LV24010 (the DATA-line can then be used as interrupt pin)

Block 2, Register 02h - RADIO_CTRL1 - Radio Control 1 Register (Write-only)

7	6	5	4	3	2	1	0
EN_MEAS	EN_AFC	Reserved	Reserved	DIR_AFC	RST_AFC	Reserved	Reserved

bit 7: **EN_MEAS:** Enable measurement bit.
0 = Normal mode.
1 = Measurement mode.

bit 6: **EN_AFC:** Enable AFC bit.
0 = Disable AFC.
1 = Enable AFC.

bit 5: **Reserved:** should be written with 0.

bit 4: **Reserved:** should be written with 1.

bit 3: **DIR_AFC:** AFC direction bit .
0 = AFC normal direction.
1 = AFC reverse direction (for test purpose).

bit 2: **RST_AFC:** Reset AFC bit.
0 = Normal operation.
1 = Reset AFC to the middle of the control range.

bit 1: **Reserved:** should be written with 1.

bit 0: **Reserved:** should be written with 1.

Block 2, Register 03h - IF_CENTER - IF Center Frequency Register (Write-only)

7	6	5	4	3	2	1	0
IFCOSC[7:0]							

bit 7-0: **IFCENT[7:0]:** Value for centering the IF frequency .

Block 2, Register 05h - IF_BW - IF Bandwidth Register (Write-only)

7	6	5	4	3	2	1	0
IFBW[7:0]							

Bit 7-0: **IFBW[7:0]:** Value for IF bandwidth.

Block 2, Register 06h - RADIO_CTRL2 - Radio Control 2 Register (Write-only)

7	6	5	4	3	2	1	0
VREF2	VREF	STABI_BP	IF_PM_L	Reserved	Reserved	AGCSP	AM_ANT_BSW

bit 7: **VREF2:** V_{REF2} control bit.
0 = V_{REF2} is ON.
1 = V_{REF2} is OFF.

bit 6: **VREF:** VREF control bit.
0 = V_{REF} is ON.
1 = V_{REF} is OFF.

bit 5: **STABI_BP:** Stabi Bypass bit.
0 = Internal voltage is V_{stabi} (normal operation).
1 = Internal voltage is V_{CC} (stabi bypassed).

bit 4: **IF_PM_L**: IF PLL mute bit.
0 = IF PLL mute on (presetting IF mode).
1 = IF PLL mute off (normal operation mode).

bit 3: **Reserved:** should be written with 0.

bit 2: **Reserved:** should be written with 0.

bit 1: **AGCSP**: AGC speed control bit.
0 = Normal speed.
1 = High speed.

Note: Turn on this bit will speed up the field strength measurement (fast tuning).

bit 0: **Reserved:** should be written with 0.

Block 2, Register 07h - RADIO_CTRL3 - Radio Control 3 Register (Write-only)

7	6	5	4	3	2	1	0
AGC_SLVL	VOLSH	Reserved	AMUTE_L	SE_FM	Reserved	Reserved	Reserved

bit 7: **AGC_SLVL:** AGC set level bit.
This bit must be set to 1 for normal operation mode.

bit 6: **VOLSH:** Volume level shift bit.
0 = Normal volume level.
1 = Increase volume of 12dB.

bit 5: **Reserved:** should be written with 0.

bit 4: **AMUTE_L:** Audio mute bit.
0 = Audio muted.
1 = Audio not muted.

bit 3: **SE_FM:** FM radio select bit.
0 = Disable FM radio.
1 = Enable FM radio.

bit 2: **Reserved:** should be written with 0.

bit 1: **Reserved:** should be written with 0.

bit 0: **Reserved:** should be written with 0.

Block 2, Register 08h - STEREO_CTRL - Stereo Control Register (Write-only)

7	6	5	4	3	2	1	0
FRCST	FMCS[2:0]			AUTOSSR	DELTA_TN	SD_PM	ST_M

bit 7: **FRCST:** Force stereo bit.
0 = Normal mode.
1 = Force stereo mode for test.

bit 6-4: **FMCS[2:0]:** FM channel separation bits.
0…7 = FM channel separation level.

bit 3: **AUTOSSR:** Auto stereo slew rate enable bit.
0 = Disable stereo auto slew rate.
1 = Enable stereo auto slew rate.

bit 2: **DELTA_TN:** Delta tune bit.
0 = Decrease delta tune.
1 = Normal delta tune.

bit 1: **SD_PM:** Stereo decoder PLL mute bit.
0 = Stereo decoder PLL not muted (normal operation).
1 = Stereo decoder PLL is muted (presetting mode).

bit 0: **ST_M:** FM stereo/mono mode bit.
0 = Stereo mode.
1 = Mono mode.

Block 2, Register 09h - AUDIO_CTRL1 - Audio Control 1 Register (Write-only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	VOL_LVL			

bit 7-4: **Reserved:** should be written with 0

bit 3-0: **VOL_LVL:** volume level bits
1111b = Minimum volume level.
0000b = Maximum volume level.
Each level is about 3dB volume adjustment.

Block 2, Register 0Ah - AUDIO_CTRL2 - Audio Control 2 Register (Write-only)

7	6	5	4	3	2	1	0
Reserved	Reserved	DEEMP	Reserved	Reserved	Reserved	Reserved	Reserved

bit 7-6: **Reserved:** should be written with 11b.

bit 5: **DEEMP:** De-emphasis bit.
0 = De-emphasis 50μs.
1 = De-emphasis 75μs.

bit 4-0: **Reserved:** should be written with 00000b.

Block 2, Register 0Bh - PW_SCTRL - Power and Soft Control Register (Write-only)

7	6	5	4	3	2	1	0
SS_CTRL			SM_CTRL			Reserved	PW_RAD

bit 7-5: **SS_CTRL:** Soft stereo control bits (8 levels).
000b = Minimal soft stereo (off).
111b = Maximal soft stereo level.

bit 4-2: **SM_CTRL:** Soft audio mute bits (8 levels).
000b = Minimal audio mute (off).
111b = Maximal soft audio mute level.

bit 1: **Reserved:** should be written with 0.

bit 0: **PW_RAD:** Radio circuitry power bit.
0 = Radio circuitry is switched OFF.
1 = Switch radio circuitry ON.

Note: PW_RAD is 0 at power up.

Block 4, Register 03h - RDS_FLTDAC - RDS Filter DAC Register (Write-only)

7	6	5	4	3	2	1	0
RFLTDAC[7:0]							

bit 7-0: **RFLTDAC[7:0]:** DAC value for RDS filter.

Note: This register should be programmed with 95% of the value of RDS_OSC register.

Block 4, Register 04h - RDAT_L - RDS Data Low Register (Read-only)

7	6	5	4	3	2	1	0
RD_L[7:0]							

bit 7-0: **RD_L[7:0]:** Low byte of the RDS data.

Note: bit 0 contains the first received bit.

Block 4, Register 05h - RDAT_H - RDS Data High Register (Read-only)

7	6	5	4	3	2	1	0
RD_L[7:0]							

bit 7-0: **RD_H[7:0]:** High byte of the RDS data.

Note: bit 0 contains the first received bit.

Block 4, Register 06h - RDS_CTRL - RDS Control Register (Write-only)

7	6	5	4	3	2	1	0
RDS_EN_L	RDS_PM	RDSLRG	RDSITG_L	RDSBW1	RDSBW0	RDCNT_EN	RDCNT_RS

bit 7: **RDS_EN_L:** Enable RDS (active low).
0 = RDS is switched ON.
1 = RDS is switched OFF.

bit 6: **RDS_PM:** RDS PLL mute bit.
0 = RDS PLL is un-muted (normal operation mode).
1 = RDS PLL is muted (calibration mode).

bit 5: **RDSLRG:** RDS lock range.
0 = Normal lock range.
1 = Lock range × 2.

bit 4: **RDSITG_L:** RDS integrator.
0 = Enable RDS integrator.
1 = Disable RDS integrator.

bit 3-2: **RDSBW[1:0]:** RDS Band Width Bits.
00 = RDS Bandwidth is 2.5 kHz.
01 = RDS Bandwidth is 3.5 kHz.
10 = RDS Bandwidth is 4.5 kHz.
11 = RDS Bandwidth is 5.5 kHz.

bit 1: **RDCNT_EN:** Enable RDS received bit counter.
0 = Disable RDS counter.
1 = Enable RDS counter (normal mode).

Note: The RDS received bit counter should be enabled when RDS is enabled.

bit 0: **RDCNT_RS:** Reset RDS received bit counter.
0 = Reset is switched OFF (normal mode).
1 = Reset is switched ON.

Note: Generate RDS counter reset by making this bit high then low. This will flush the received RDS data FIFO.

Block 4, Register 07h - RDS_OSC - RDS PLL Oscillator Register (Write-only)

7	6	5	4	3	2	1	0
RDOSC[7:0]							

bit 7-0: **RDOSC[7:0]:** DAC value for RDS PLL oscillator.

Note: Positive DAC control (i.e. the frequency increases with the register's value).

Block 4, Register 09h - RDS_INPS - RDS Input Setting Register (Write-only)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RGAIN	RVREF	MPXDIV	EN_RNH

bit 7-4: **Reserved:** Must be programmed with 0000b.

bit 3: **RDS_PM:** RDS PLL mute bit.
0 = RDS PLL is un-muted (normal operation mode).
1 = RDS PLL is muted (calibration mode).

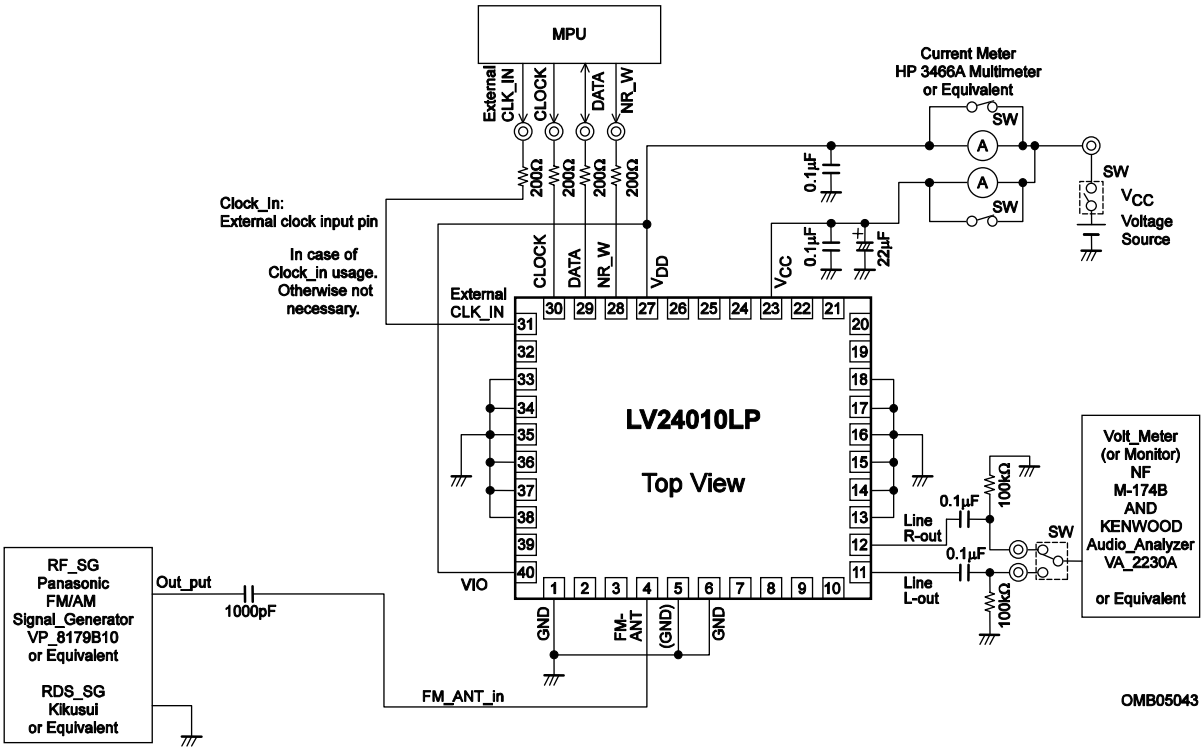
bit 5: **RGAIN:** Gain control.
0 = 11 ×.
1 = 8 ×.

bit 2: **RVREF:** Measure RDS Vref.
0 = Disable.
1 = Enable (test purpose only).

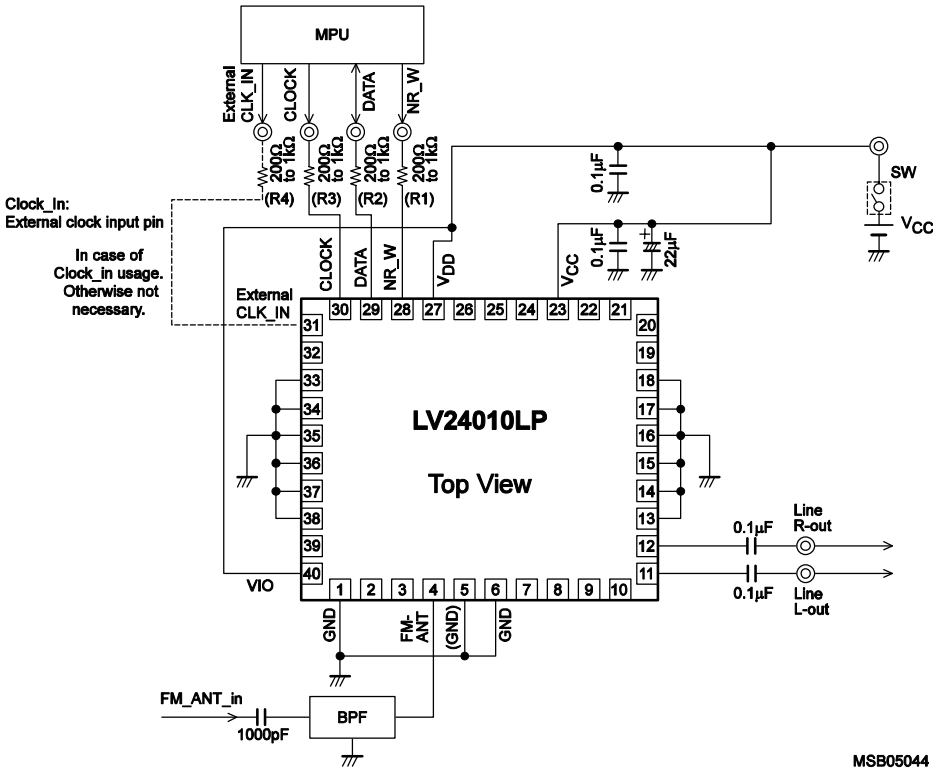
bit 1: **MPXDIV:** MPX input divider.
0 =1:3.
1 =1:1.

bit 0: **EN_RNH:** RDS notch.
0 = Disable.
1 = Enable.

Measurement Circuit

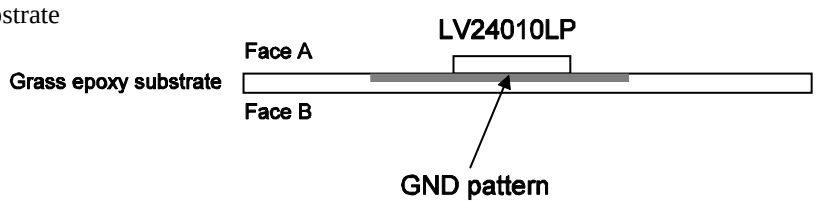


Application Circuit Example



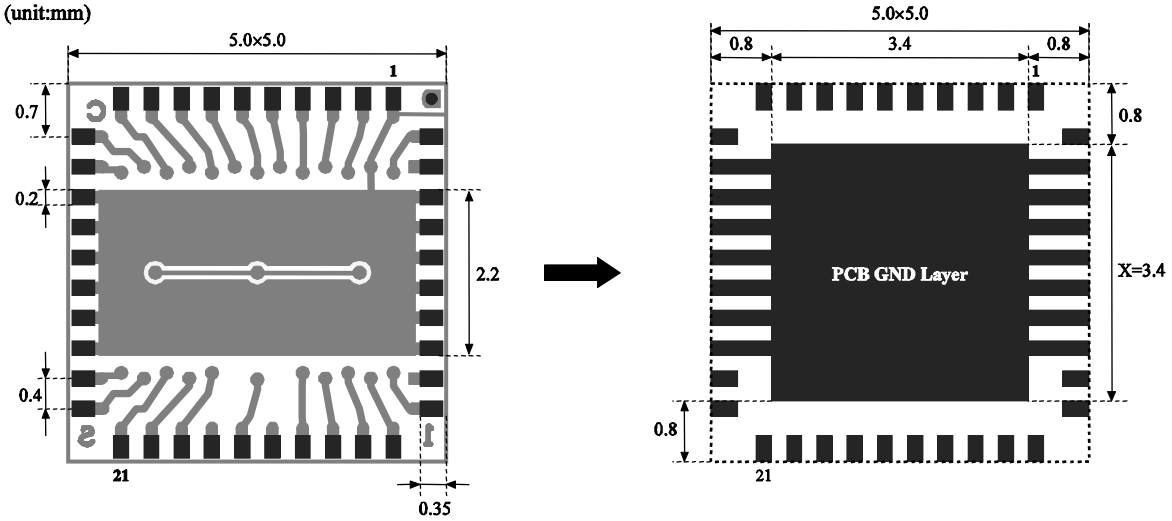
Note1: The vale of External Component is just reference. Please set most suitable value under actual operation.
Note2: In case of necessary about BPF for FM_in, Please take Consideration of most suitable value.
Note3: We recommend to put R1,R2,R3,R4 for interface between MPU and IC.
Note4: Please put Capacitor between V_{DD} and GND also, put Capacitor between V_{CC} and GND as shown on application.
Note5: In case of not using External Clock_in (pin31), Please tie to GND.

Recommended LV24010LP's PCB Layout Conditions



* This IC has an inductor for local oscillation on the bottom side of the package.
To enable coverage of the receive frequency range of 76MHz to 108MHz (according to the receive frequency 1 specification), it is requested to arrange the GND layer as the first layer on the PCB_A face directly below the package bottom surface, as shown in the figure.

Recommended PCB substrate layout



IC substrate_LV24010LP

Recommended GND layer for PCB directly below IC

- For this SPL, the receive frequency is measured under above following conditions:
- The X-value can be freely set between Min = 2.2mm and Max = 3.8mm (The X-value for Sanyo Demo Board is 3.4mm).
- It is recommended to avoid provision of other wiring within 0.4mm from the lower layer of PCB_GND as much as possible.