SKYWORKS™

RM009

Power Amplifier Module for Dual-band GSM900 DCS1800

The RM009 is a dual-band Power Amplifier Module (PAM) designed in a compact form factor for Class 4 GSM900 and Class 1 DCS1800 cellular handsets.

The module consists a GSM900 PA block and a DCS1800 PA block, matching circuitry for 50 Ω input and output impedances, and bias control circuitry. Two separate Heterojunction Bipolar Transistor (HBT) PA blocks are fabricated on a single Gallium Arsenide (GaAs) die. One PA block operates in the GSM900 band and the other supports the DCS1800 band. The PAM is optimized for three-cell operation with both PAs sharing common power supply pins to distribute current. A custom CMOS integrated circuit contains a current amplifier that minimizes the required power control current (I_{APC}) to 60 μA, typical.

RF input and output ports are internally matched to 50 Ω to reduce the number of external components for a dual-band design. Switching circuitry receives the band select signal on the band select pin (BS) to switch between GSM (logic 0) and DCS (logic 1). Analog Power Control (APC) controls the output power of each PA selected by the band select signal. The extremely low leakage current (2 μA, typical) of the RM009 dual-band module maximizes handset standby time.

The functional block diagram shows the relationship of the dual PAs and the CMOS device in the RM009.

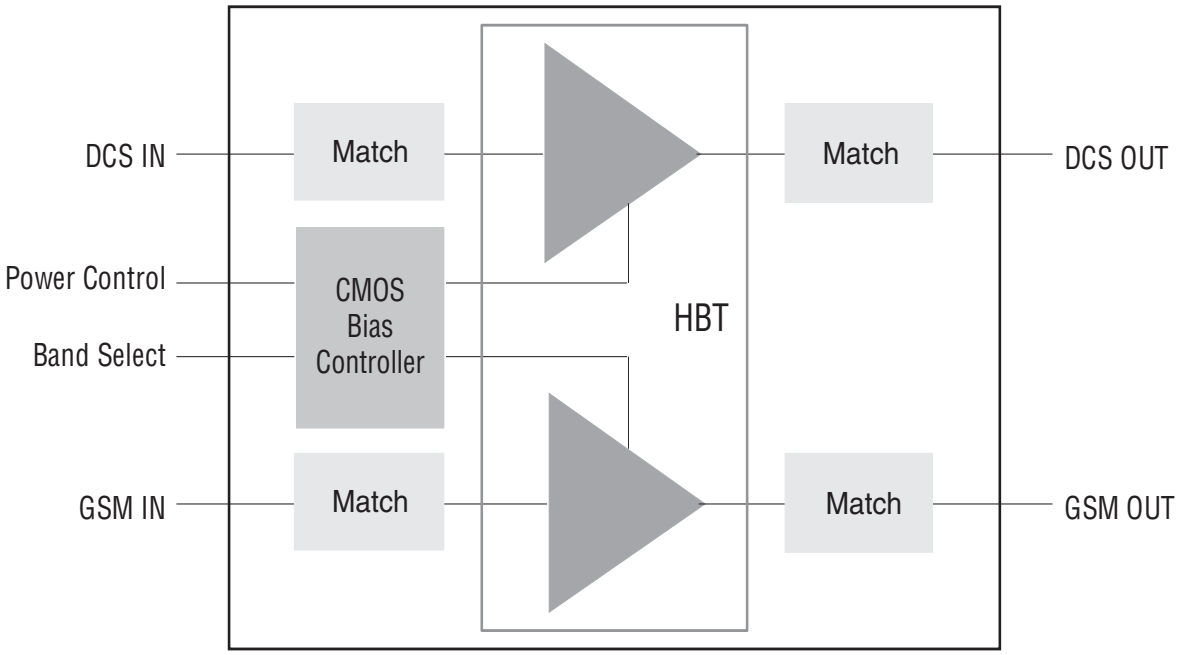
Distinguishing Features

- High efficiency
  GSM 54%
  DCS 45%
- Input/output matching
  50 Ω internal
- Small outline
  9.1 mm x 11.6 mm
- Low profile
  1.50 mm ±10%
- Low APC current
  60 μA

Applications

- Class 4 GSM900 and Class 1 DCS1800 dual-band cellular handsets

Functional Block Diagram



Electrical Specifications

Table 1 provides the absolute maximum ratings of the RM009, Table 2 shows the recommended operating conditions and Table 3 shows the electrical characteristics.

Table 1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply Voltage (V_{CC})	—	7	V
Storage Temperature	–55	+125	°C

Table 2. Recommended Operating Conditions

Parameter	Minimum	Typical	Maximum	Unit
Supply Voltage (V_{CC})	2.7	3.2	4.5	V
Temperature	–30	—	+85	°C

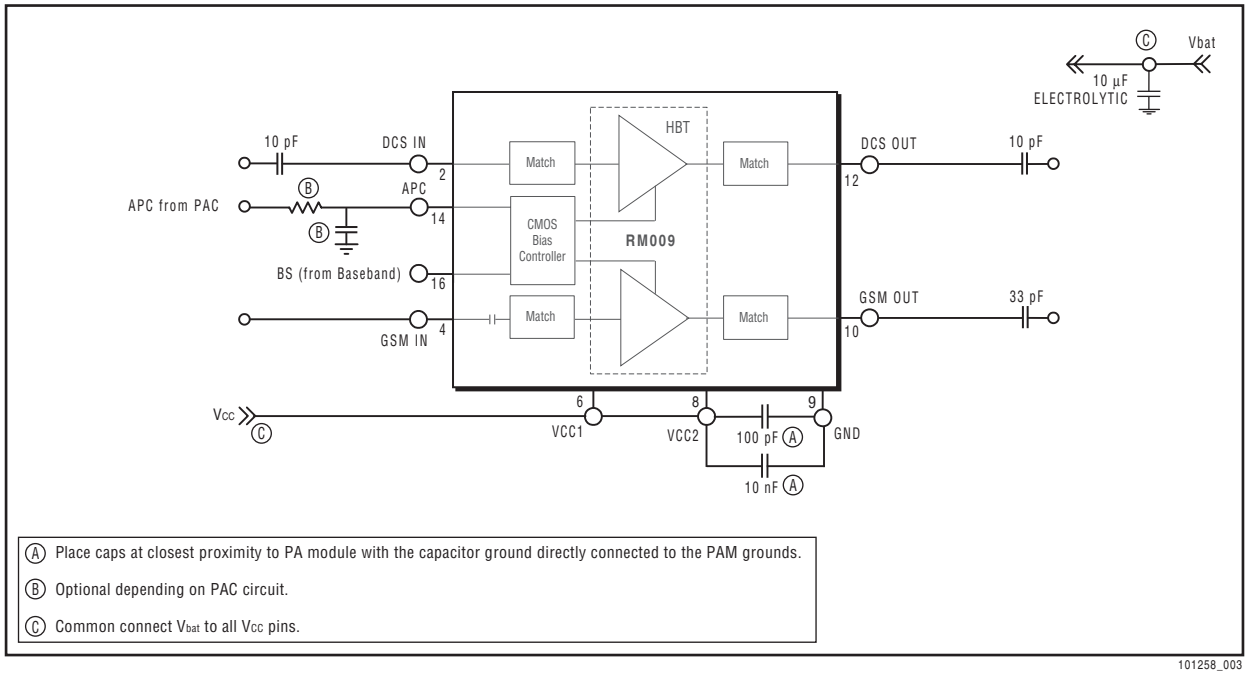
Table 3. RM009 Electrical Specifications *(1 of 2)*

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
GSM Mode (f = 880 MHz to 915 MHz and P_{IN} = 8 dBm to 12 dBm)						
Frequency Range GSM900	f_1	—	880	—	915	MHz
Input Power GSM900	P_{INGSM}	—	8	10	12	dBm
Leakage Current	$I_{LEAKAGE}$	V_{CC} = 4.5 V V_{APC} = 0 V V_{BS} = 0 V	—	5	—	µA
Efficiency GSM900	η_{GSM}	P_{INGSM} = 10 dBm	46	54	—	%
GSM 2nd and 3rd Harmonic Distortion	H_{2GSM}	P_{OUTGSM} = 34.5 dBm	–39.5	–45	—	dBc
Output Power GSM900	P_{OUTGSM}	P_{INGSM} = 10 dBm	34.5	35	—	dBm
	P_{OUTGSM}	P_{INGSM} = 10 dBm V_{CC} = 2.7 V T_{CASE} = –20 °C to +85 °C	32	—	—	dBm
Input VSWR	$VSWR_{(IN)}$	All	—	1.5:1	2:1	—
Isolation GSM900	—	P_{INGSM} = 10 dBm APC= 0.2 V	—	–40	–30	dBm
Cross Isolation	—	P_{OUTGSM} = 34.5 dBm	—	–30	–25	dBm
Noise Floor GSM900	—	P_{INGSM} = 10 dBm, BW = 100 kHz, fo ±20 MHz offset	—	—	–84	dBm
Bandselect Thresholds: GSM DCS	 V_{BSLMAX} V_{BSHMIN}	—	 2.0	—	0.5	 V V

***Table 3. RM009 Electrical Specifications** (2 of 2)*

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Full Power Control Voltage	—	P_{OUTGSM} = 34.5 dBm	—	2.0	—	—
Rise Time and Fall Time	—	P_{OUTGSM} = 34.5 dBm	—	1.8	—	µsec
DCS Mode (f = 1710 MHz to 1785 MHz and P_{IN} = 6 dBm to 10 dBm)						
Frequency Range DCS1800	f_2	—	1710	—	1785	MHz
Input Power DCS1800	P_{INDCS}	—	6	8	10	dBm
Control Voltage Range	V_{APC}	—	0.2	—	2.7	V
Control Current Into Vapc	I_{APC}	—	—	60	—	µA
Leakage Current	$I_{LEAKAGE}$	V_{CC} = 3.2 V V_{APC} = 0 V V_{BS} = 0 V	—	5	—	µA
Efficiency DCS1800	η_{DCS}	P_{INDCS} = 8 dBm	38.2	45.0	—	%
DCS 2nd and 3rd Harmonic Distortion	H_{2DCS}	P_{OUTDCS} = 31.5 dBm	–40.5	–50	—	dBc
Output Power DCS1800	P_{OUTDCS}	P_{INDCS} = 8 dBm	31.5	32	—	dBm
	P_{OUTDCS}	P_{INDCS} = 8 dBm V_{CC} = 2.7 V T_{CASE} = –20 °C to +85 °C	29.5	—	—	dBm
Input VSWR	$VSWR_{(IN)}$	All	—	1.5:1	2:1	—
Isolation DCS1800	—	P_{INDCS} = 8 dBm APC = 0.2 V	—	–45	–33	dBm
Stability Condition $VSWR_{(LOAD)}$ (no spurious oscillation > –35 dBm)	—	—	—	—	8:1 all angles	—
Load Mismatch $VSWR_{(LOAD)}$ (no damage/degradation)	—	—	—	—	10:1 all angles	—
Noise Floor DCS1800	—	P_{INDCS} = 8 dBm BW = 100 kHz fo ±20 MHz offset	—	—	–76	dBm
Full Power Control Voltage	—	P_{OUTDCS} = 31.5 dBm	—	2.0	—	—
Bandselect Thresholds: GSM DCS	 V_{BSLMAX} V_{BSHMIN}	—	 2.0	—	0.5	 V V
Rise Time and Fall Time	—	P_{OUTDCS} = 31.5 dBm	—	1.8	—	µsec
NOTE(S): T_{CASE} = 25 °C, RL = 50 Ω, pulsed operation with pulse width = 577 µsec and duty cycle of 1:8, V_{CC} = 3.2 V, unless specified otherwise						

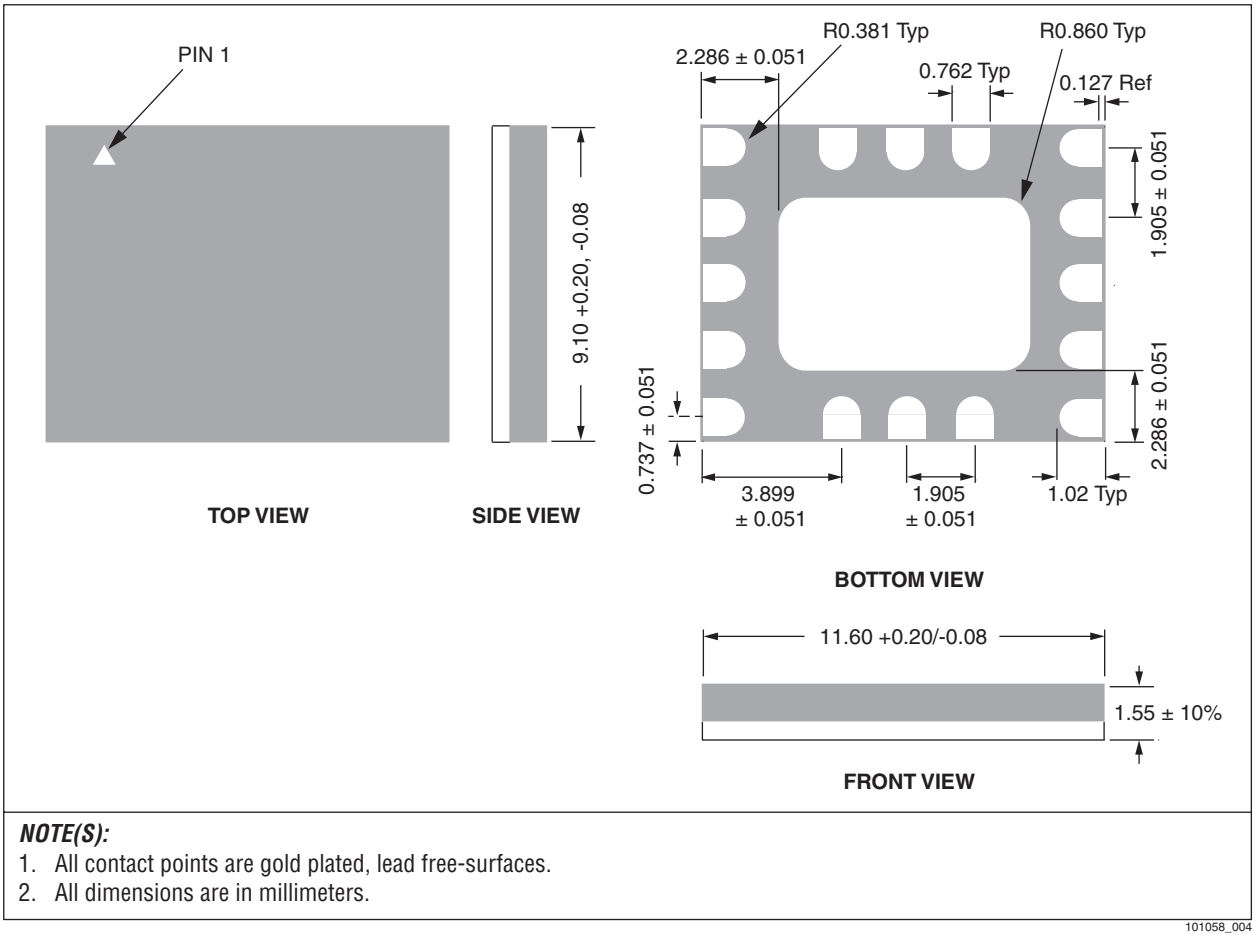
Figure 1. Typical RM009 Application



Package Dimensions and Pin Descriptions

Figure 2 is a mechanical diagram of the pad layout for the 16-pin leadless, RM009 Power Amplifier module. Figure 3 shows the device pin configuration and the pin numbering convention, which starts with pin 1 in the upper left and increments counter-clockwise around the package. Pin assignments and their functional descriptions are listed in Table 4. Figure 4 shows typical case markings.

Figure 2. RM009 PAM Package Dimensions—16-Pin Leadless Module (All Views)



NOTE(S):

1. All contact points are gold plated, lead free-surfaces.
2. All dimensions are in millimeters.

101058_004

Figure 3. RM009 Pin Configuration—16-Pin Leadless Module (Top View)

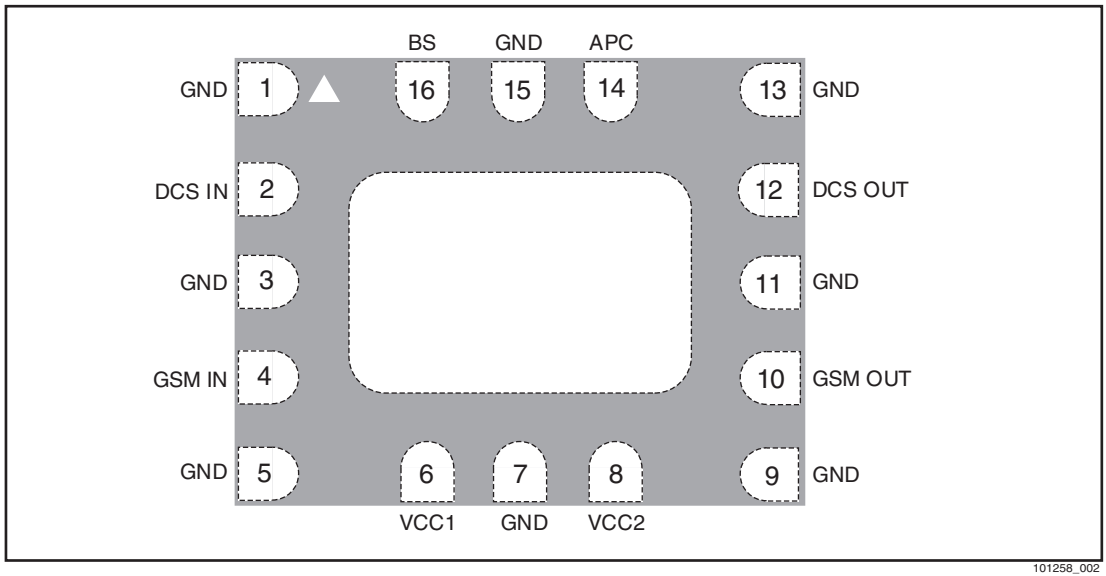


Table 4. RM009 Signal Description

Pin #	Name	Description	Pin #	Name	Description
1	GND	Ground	9	GND	Ground
2	DCS IN	RF input to DCS PA (DC coupled)	10	GSM OUT	GSM RF output (DC coupled)
3	GND	Ground	11	GND	Ground
4	GSM IN	RF input to GSM PA	12	DCS OUT	DCS RF output (DC coupled)
5	GND	Ground	13	GND	Ground
6	VCC1	Power supply for PA driver stages/ CMOS Bias Controller	14	APC	Analog Power Control
7	GND	Ground	15	GND	Ground
8	VCC2	Power supply for PA output stages	16	BS	Bandselect

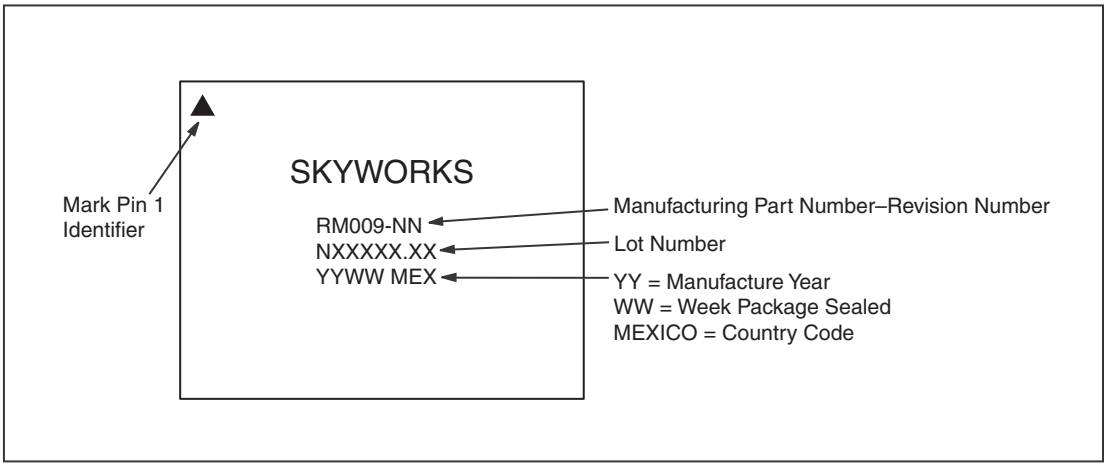
Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The RM009 is capable of withstanding an MSL 3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 5 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds.

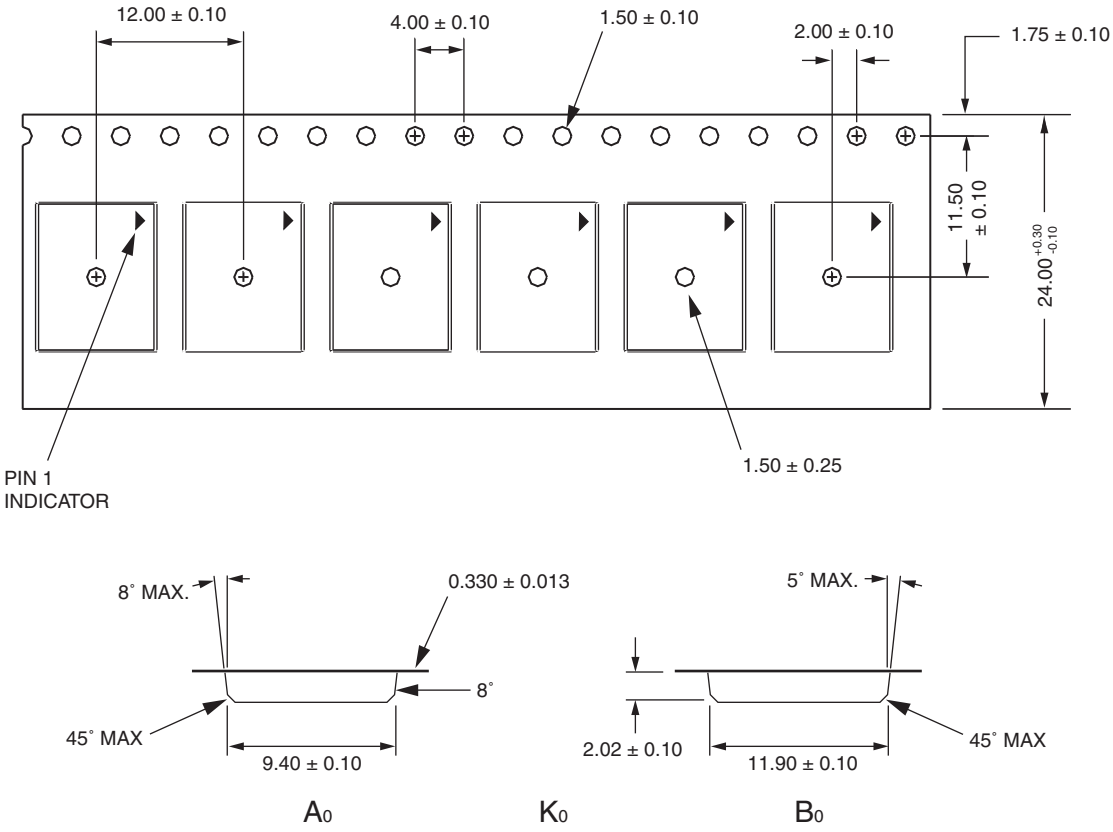
For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to *Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752*. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J–STD–020A*.

Figure 4. Typical Case Markings



Production quantities of this product are shipped in the standard tape and reel format illustrated in Figure 5.

Figure 5. RM009 Tape and Reel – 9.1 mm x 11.6 mm



NOTE(S):

1. Carrier tape material: Black conductive polycarbonate
2. Carrier tape part number: US 042 281
3. Cover tape material: Conductive Pressure Sensitive Adhesive (PSA)
4. Cover tape width: 21.3 mm
5. Number of parts per 330 mm (diameter) x 24 mm reel: 2000
6. All diagram dimensions in millimeters

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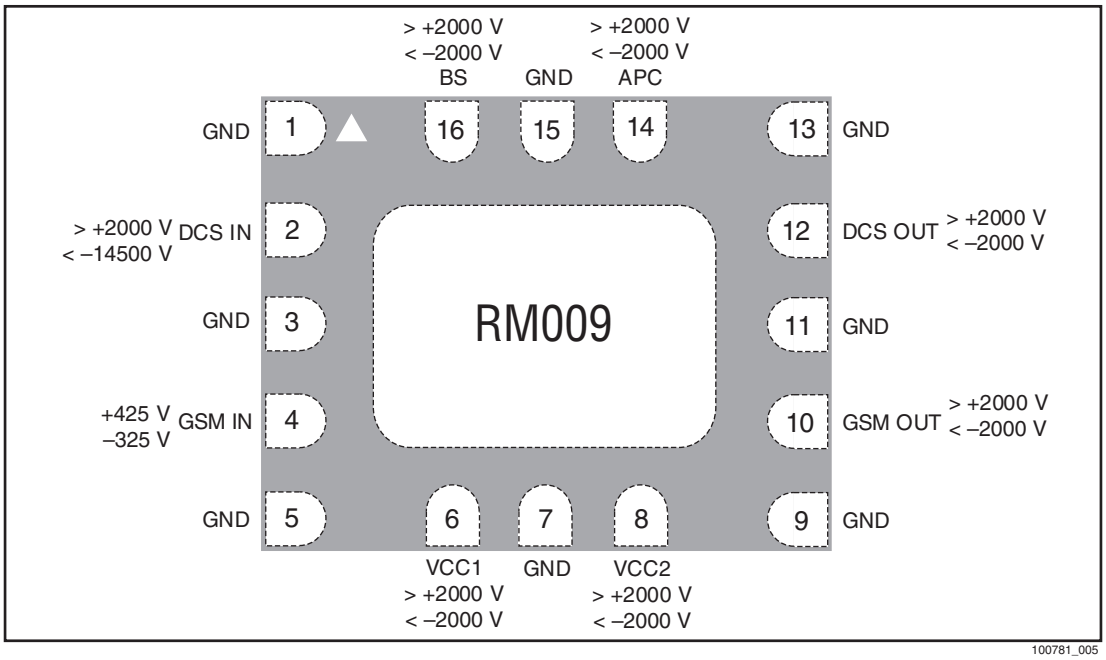
Electrostatic Discharge Sensitivity

RM009 is a Class I device. Figure 6 lists the Electrostatic Discharge (ESD) immunity level for each pin of the RM009 product. The numbers in Figure 6 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation. The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. Since 2000 volts represents the maximum measurement limit of the test equipment used, pins marked > 2000 V pass 2000 V ESD stress.

Figure 6. ESD Sensitivity Areas (Top view)



Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria, fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in Table 5.

Table 5. Precautions for GaAs ICs with ESD Thresholds Greater Than 200 V But Less Than 2000 V

Personnel Grounding	**Facility**
Wrist Straps Conductive Smocks, Gloves and Finger Cots Antistatic ID Badges	Relative Humidity Control and Air Ionizers Dissipative Floors (less than 10^9 Ω to GND)
Protective Workstation	**Protective Packaging & Transportation**
Dissipative Table Tops Protective Test Equipment (Properly Grounded) Grounded Tip Soldering Irons Conductive Solder Suckers Static Sensors	Bags and Pouches (Faraday Shield) Protective Tote Boxes (Conductive Static Shielding) Protective Trays Grounded Carts Protective Work Order Holders

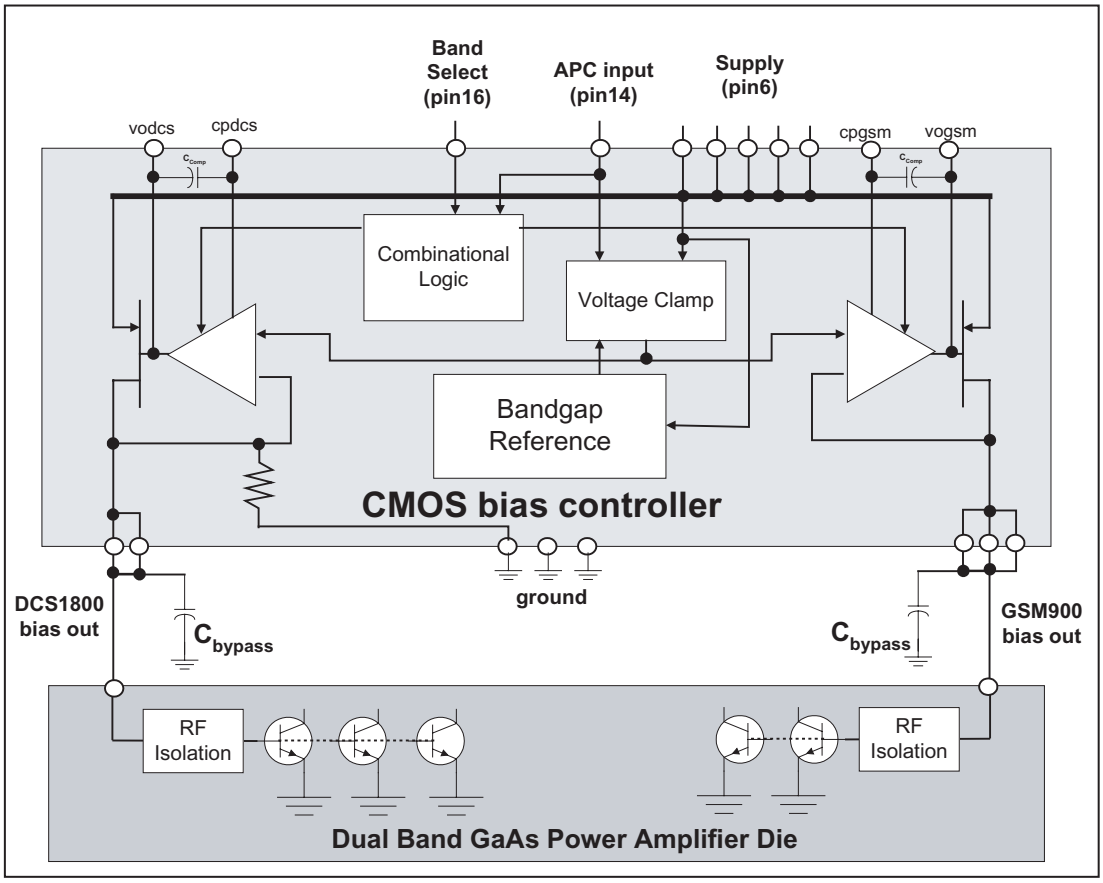
Technical Information

CMOS Bias Controller Characteristics

The CMOS die within the PAM performs several functions that are important to the overall module performance. Some of these functions must be considered for development of the power ramping features in a 3GPP compliant transmitter power control loop[1]. Power ramping considerations will be discussed later in this section.

The four main functions that will be described in this section are Standby Mode Control, Band Select, Voltage Clamp, and Current Buffer. The functional block diagram is shown in Figure 7.

Figure 7. Functional Block Diagram



1. Please refer to 3GPP TS 05.05, Digital Cellular Communications System (Phase 2+); Radio Transmission and Reception. All GSM specifications are now the responsibility of 3GPP. The standards are available at http://www.3GPP.org/specs/specs.htm

Standby Mode Control

The Combinational Logic cell includes enable circuitry that monitors the APC ramping voltage from the power amplifier controller (PAC) circuit in the GSM transmitter. Typical handset designs directly connect the PA V_{CC} to the battery at all times, and for some PA manufacturers this requires a control signal to set the device in or out of standby mode. The Skyworks PAM does not require a Transmit Enable input because it contains a standby detection circuit that senses the V_{APC} to enable or disable the PA. This feature helps minimize battery discharge when the PA is in standby mode. When V_{APC} is below the enable threshold voltage, the PA goes into a standby mode, which reduces battery current (I_{CC}) to 6 µA, typical, under nominal conditions.

For voltages less than 700 mV at the APC input (pin 14), the PA bias is held at ground. As the APC input exceeds the enable threshold, the bias will activate. After an 8 µsec delay, the amplifier internal bias will ramp quickly to match the ramp voltage applied to the APC input. In order for the internal bias to precisely follow the APC ramping voltage, it is critical that a ramp pedestal is set to the APC input at or above the enable threshold level with a timing at least 8 µsec prior to ramp-up. This will be discussed in more detail in the following section, “Power Ramping Considerations for 3GPP Compliance”.

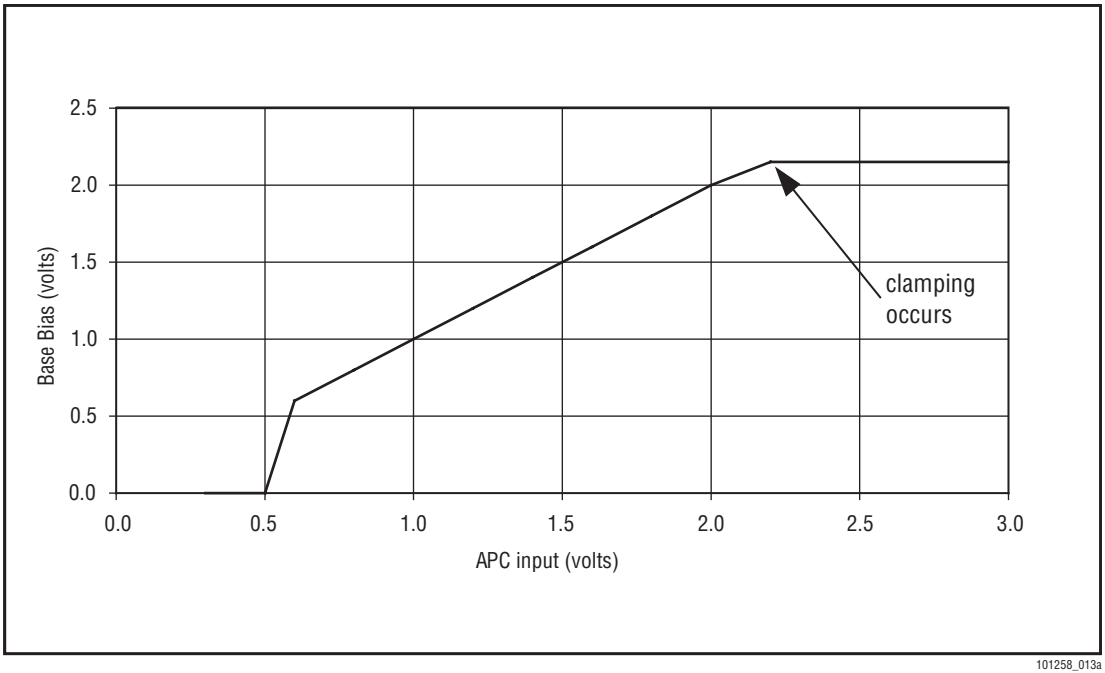
Band Select

The Combinational Logic cell also includes a simple gate arrangement that selects the desired operational band by activating the appropriate current buffer. The voltage threshold level at the Band Select input (pin 16) will determine the active path of the bias output to the GaAs die.

Voltage Clamp

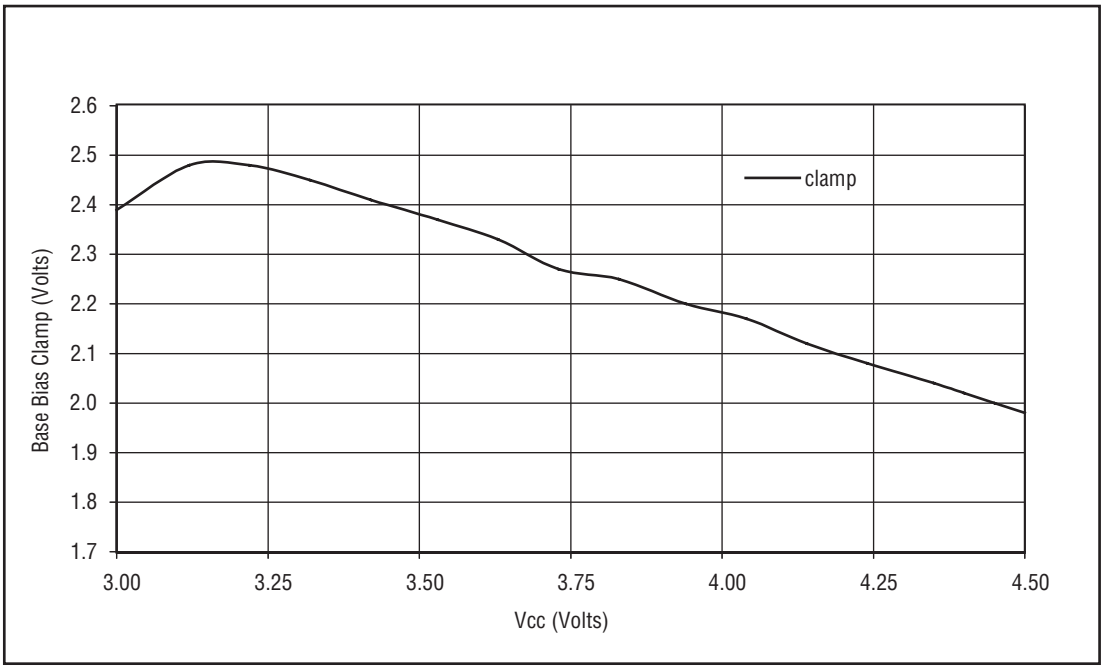
The Voltage Clamp circuit will limit the maximum bias voltage output applied to the bases of the HBT devices on the GaAs die. This provides protection against electrical overstress (EOS) of the active devices during high voltage and/or load mismatch conditions. Figure 8 shows the typical transfer function of the APC input to buffer output under resistively loaded conditions. Notice the enable function near 600 mV, and the clamp acting at 2.15 V, corresponding to a supply voltage of 4.0 V.

Figure 8. Base Bias Voltage vs. APC Input, V_{CC} = 4.0 V



Due to output impedance effects, the bias of the GaAs devices increases as the supply voltage increases. The Voltage Clamp is designed to gradually decrease in level as the battery voltage increases. The performance of the clamp circuit is enhanced by the band gap reference that provides a supply-, process-, and temperature-independent reference voltage. The transfer function relative to V_{BAT} is shown in Figure 9. For battery voltages below 3.4 V, the base bias voltage is limited by the common mode range of the buffer amplifier. For battery voltages above 3.4 V, the clamp limits the base bias.

Figure 9. Base Bias Clamp Voltage vs. Supply Voltage



Current Buffer

The output buffer amplifier performs a vital function in the CMOS device by transferring the APC input voltage ramp to the base of the GaAs power devices. This allows the APC input to be a high impedance port, sinking only 10 µA, typical, assuring no loading effects on the PAC circuit. The buffers are designed to source the high GaAs base currents required, while allowing a settling time of less than 8 µsec for a 1.5 V ramp.

Power Ramping Considerations for 3GPP Compliance

These are the primary variables in the power control loop that the system designer must control:

- software control of the DSP / DAC
- software control of the transmitter timing signals
- ramp profile attributes - pedestal, number of steps, duration of steps
- layout of circuit / parasitics
- RC time constants within the PAC circuit design

All of these variables will directly influence the ability of a GSM transmitter power control loop to comply with 3GPP specifications.

Although there is a specific time mask template in which the transmitter power is allowed to ramp up, the method is very critical. The 3GPP system specification for switching transients results in a

requirement to limit the edge rate of output power transitions of the mobile. Switching transients are caused by the transition from minimum output power to the desired output power, and vice versa. The spectrum generated by this transition is due to the ramping waveform amplitude modulation imposed on the carrier. Sharper transitions tend to produce more spectral "splatter" than smooth transitions. If the transmit output power is ramped up too slowly, the radio will violate the time mask specification. In this condition, the radio may not successfully initiate or maintain a phone call. If the transmit output power is ramped up too quickly, this will cause RF "splatter" at certain frequency offsets from the carrier as dictated by the 3GPP specification. This splatter, known as Output RF Spectrum (ORFS) due to Switching Transients, will increase the system noise level, which may knock out other users on the system. The main difficulty with TDMA power control is allowing the transmitter to ramp the output power up and down gradually so switching transients are not compromised while meeting the time mask template at all output power levels in all operational bands. The transmitter has 28 µsec to ramp up power from an off state to the desired power level.

The GSM transmitter power control loop generally involves feedback around the GaAs PA, which limits the bandwidth of signals that can be applied to the PA bias input. Since the PA is within the feedback loop, its own small-signal frequency response must exhibit a bandwidth 5 to 10 times that of the power control loop. As discussed in the previous section, the PA bias is held at ground for inputs less than 700mV. As the APC input exceeds the enable threshold, the bias will activate. After an 8 µs delay, the amplifier internal bias will quickly ramp to match the ramp voltage applied to the V_{APC} input. Since the bias must be wide band relative to the power control loop, the ramp will exhibit a fast edge rate. If the APC input increases beyond 1V before the 8 µs switching delay is allowed to occur after the bias is enabled, the PA will have significant RF output as the internal bias approaches the applied bias. During this ramp, the internal power control is running "open loop" and the edge rates are defined by the frequency response of the PA bias rather than that of the power control loop. This open loop condition will result in switching transients that are directly correlated to the PA bias bandwidth.

Application of an initial APC voltage, which enables the bias at least 8 µs before the V_{APC} voltage is ramped, will ensure that the internal bias of the PAM will directly follow the applied V_{APC}. As a result, the power control loop will define all edge transitions rather than the PA internal bandwidth defining the transition. Figures 10 and 11 show the relationship of the internal bias relative to the applied APC in two cases. One case has ramping starting from ground; the other case has ramping starting with an initial enable pedestal of 700 mV. It is evident that the pedestal level is critical to ensure a predictable and well behaved power control loop.

To enable the CMOS driver in the PAM prior to ramp-up, a PAC output pedestal level to the APC input of the PAM (pin 14) should be set to about 700 mV. This pedestal level should have a duration of at least 8 µsec directly prior to the start of ramp up.

Figure 12 shows typical signals and timings measured in a GSM transmitter power control loop. This particular example is at GSM Power Level 5, Channel 62. The oscilloscope traces are TxVCO_enable, PAC_enable, DAC Ramp, and V_{APC} (pin 14).

NOTE: When the TxVCO is enabled, the pedestal becomes set at the APC input of the PAM, then the PAC is enabled, and finally the DAC ramp begins.

The device specifications for enable threshold level and switching delay are shown in Table 3.

Figure 10. PAM Internal Bias Performance – No Pedestal Applied

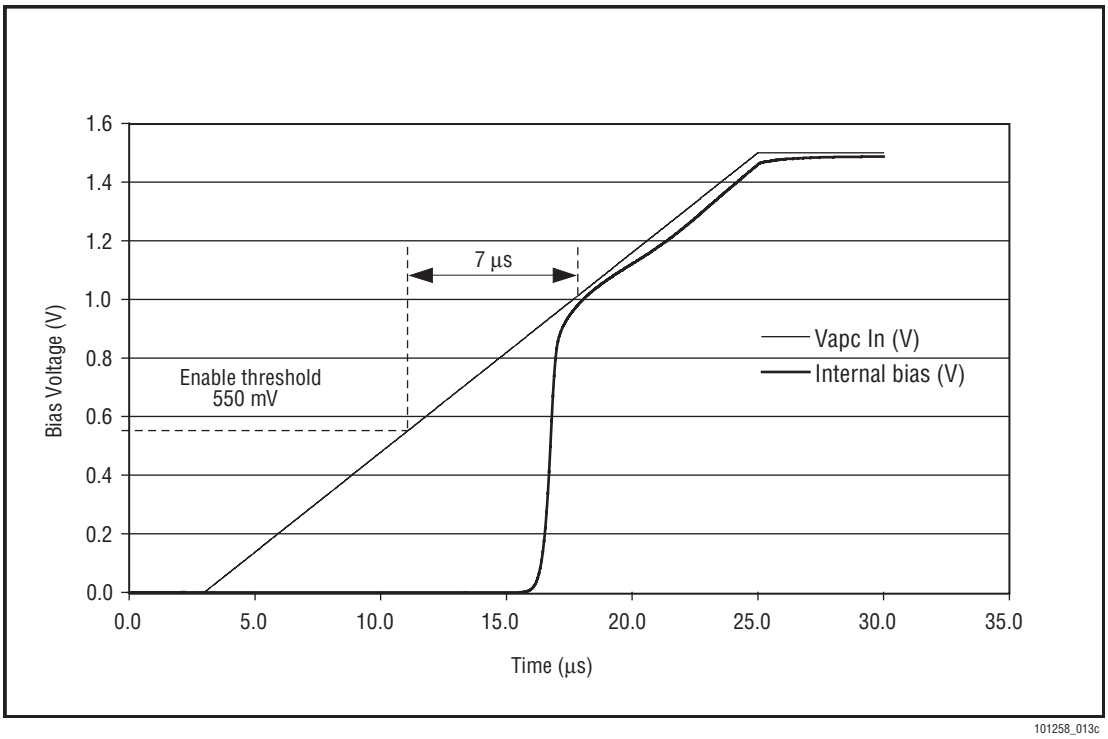


Figure 11. PAM Internal Bias Performance – Pedestal Applied

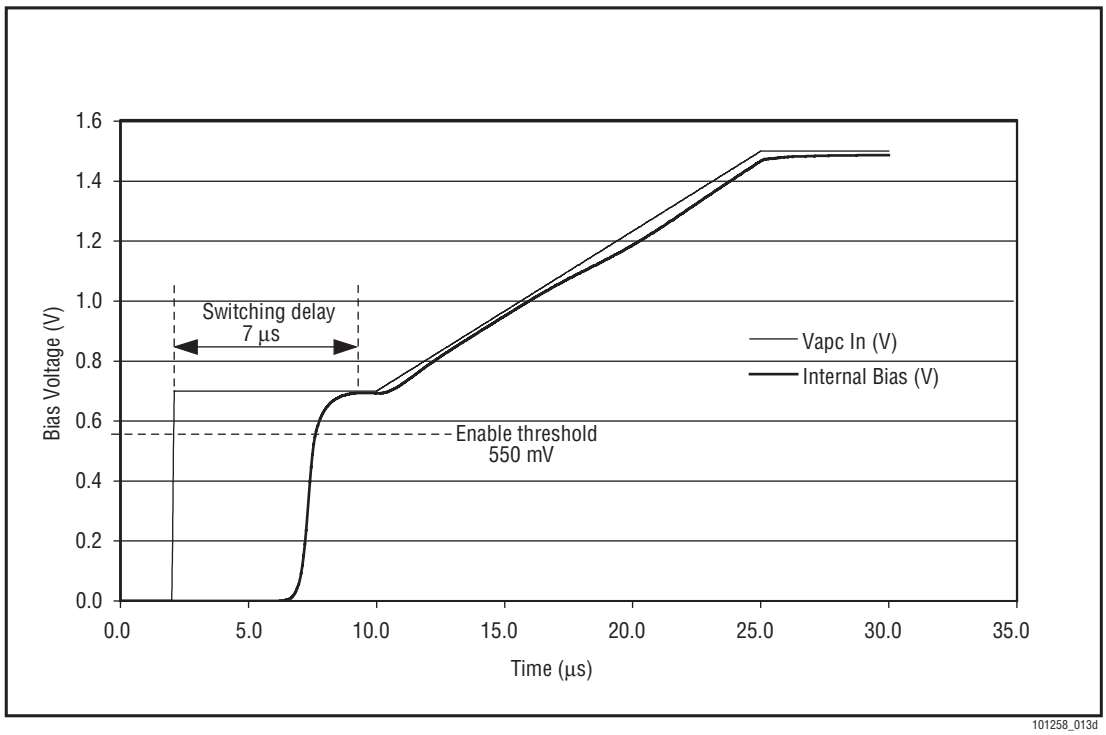
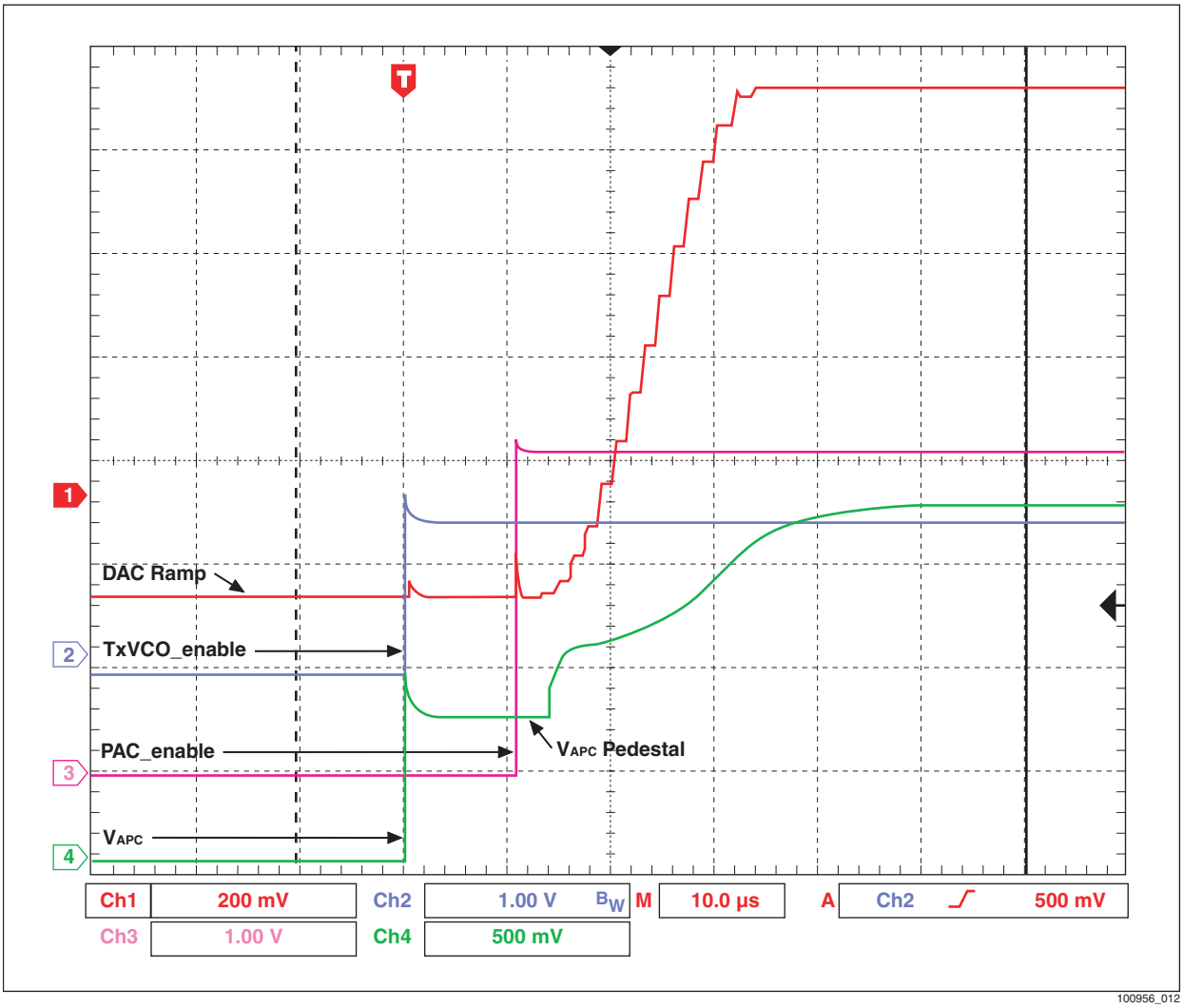


Figure 12. GSM Transmitter - Typical Ramp-up Signals



Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
RM009	RM009-19	19		–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		June 2001	Initial Release
B		February 26, 2003	Add: Packaging and Handling Information section, Technical Information Section Revise: Table 3

References:

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101762
JEDEC Standard J–STD–020A

General Information:
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Newport Beach, CA. 92660-3007
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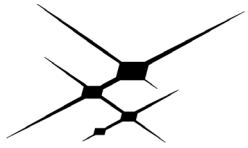

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