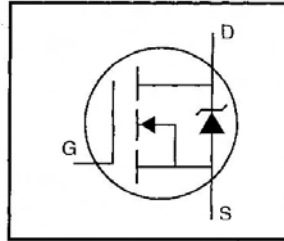


# IRFR310PbF

# IRFU310PbF

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR310)
- Straight Lead (IRFU310)
- Available in Tape & Reel
- Fast Switching
- Ease of Paralleling
- Lead-Free

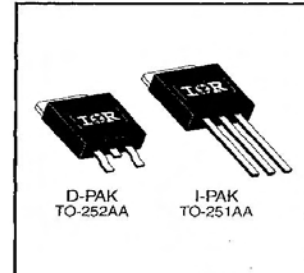


$V_{DSS} = 400V$   
 $R_{DS(on)} = 3.6\Omega$   
 $I_D = 1.7A$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.7	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10 V$	1.1	
$I_{DM}$	Pulsed Drain Current ①	6.0	
$P_D @ T_C = 25^\circ C$	Power Dissipation	25	W
$P_D @ T_A = 25^\circ C$	Power Dissipation (PCB Mount)**	2.5	
	Linear Derating Factor	0.20	W/°C
	Linear Derating Factor (PCB Mount)**	0.020	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	86	mJ
$I_{AR}$	Avalanche Current ①	1.7	A
$E_{AR}$	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to +150	°C
	Soldering Temperature, for 10 seconds	260 (1.6mm from case)	

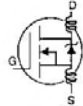
### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	5.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)**	—	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	—	110	

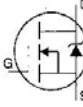
\*\* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

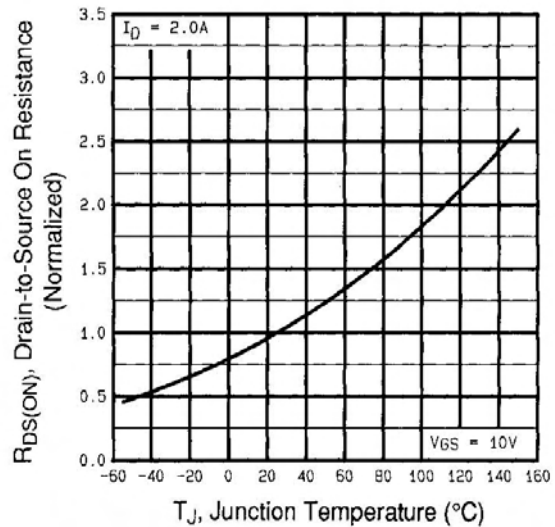
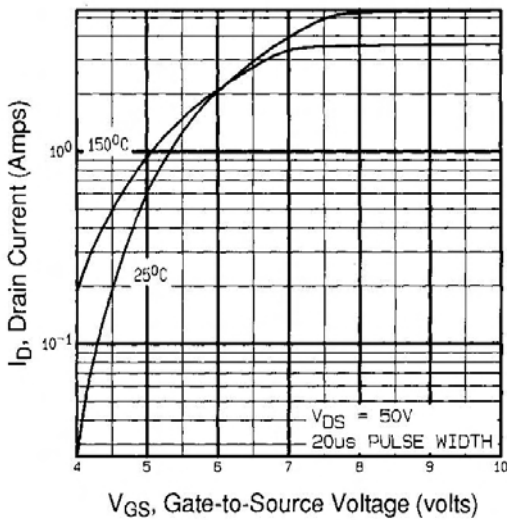
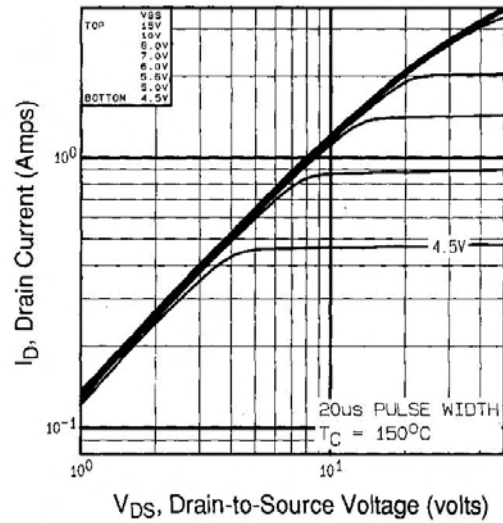
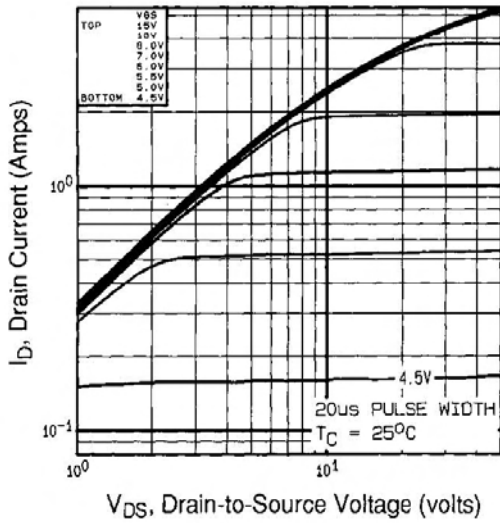
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	400	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.47	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	3.6	$\Omega$	$V_{GS}=10V, I_D=1.0A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	0.97	—	—	S	$V_{DS}=50V, I_D=1.0A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=400V, V_{GS}=0V$
		—	—	250		$V_{DS}=320V, V_{GS}=0V, T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-20V$
$Q_g$	Total Gate Charge	—	—	12	nC	$I_D=2.0A$
$Q_{gs}$	Gate-to-Source Charge	—	—	1.9		$V_{DS}=320V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	6.5		$V_{GS}=10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	7.9	—	ns	$V_{DD}=200V$
$t_r$	Rise Time	—	9.9	—		$I_D=2.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G=24\Omega$
$t_f$	Fall Time	—	11	—		$R_D=95\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	170	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	34	—		$V_{DS}=25V$
$C_{riss}$	Reverse Transfer Capacitance	—	6.3	—		$f=1.0\text{MHz}$ See Figure 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	1.7	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	6.0		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J=25^\circ\text{C}, I_S=1.7A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	240	540	ns	$T_J=25^\circ\text{C}, I_F=2.0A$
$Q_{rr}$	Reverse Recovery Charge	—	0.85	1.6	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

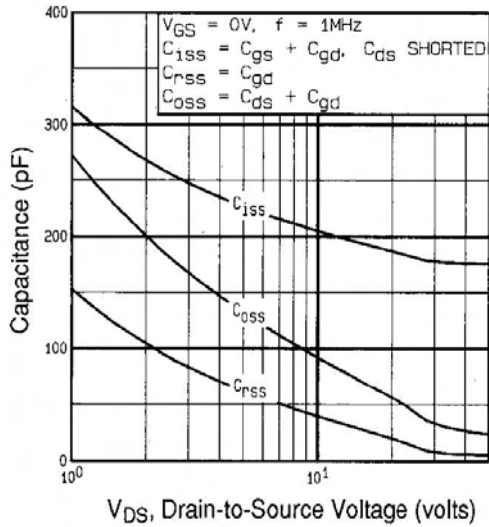
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=50V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=52\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=1.7A$  (See Figure 12)
- ③  $I_{SD}\leq 1.7A$ ,  $di/dt\leq 40A/\mu s$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

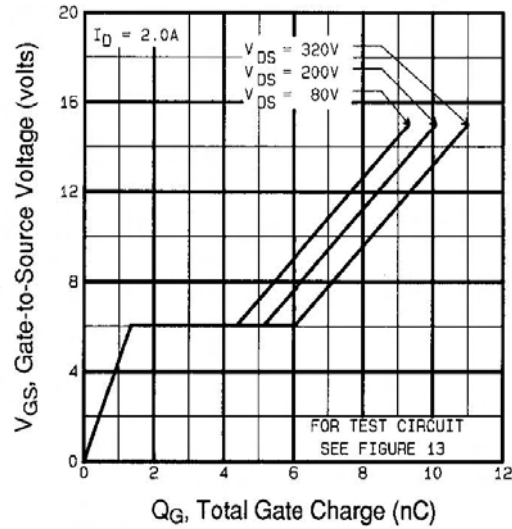


# IRFR/U310PbF

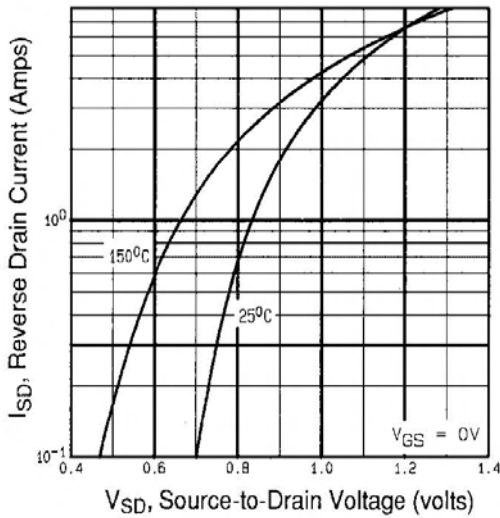
International  
**IR** Rectifier



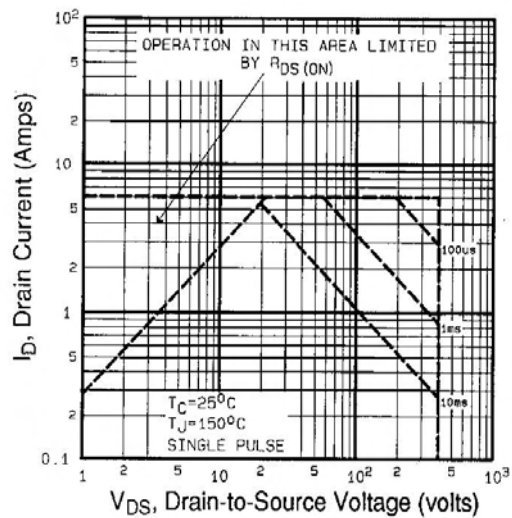
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

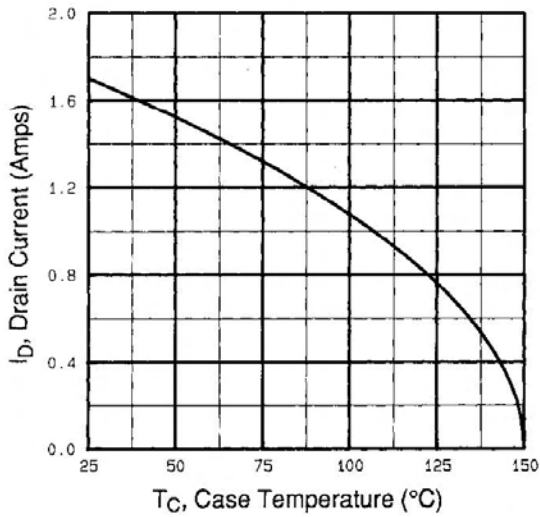


Fig 9. Maximum Drain Current Vs. Case Temperature

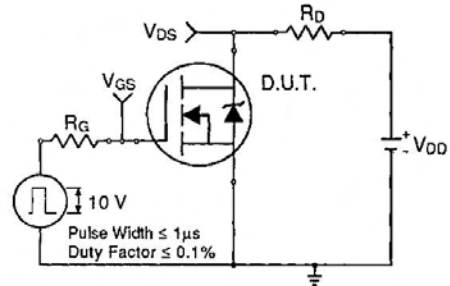


Fig 10a. Switching Time Test Circuit

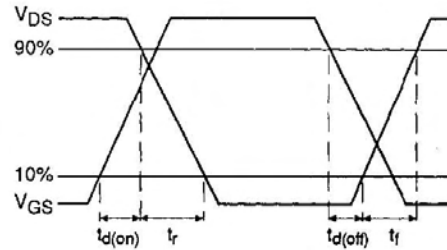


Fig 10b. Switching Time Waveforms

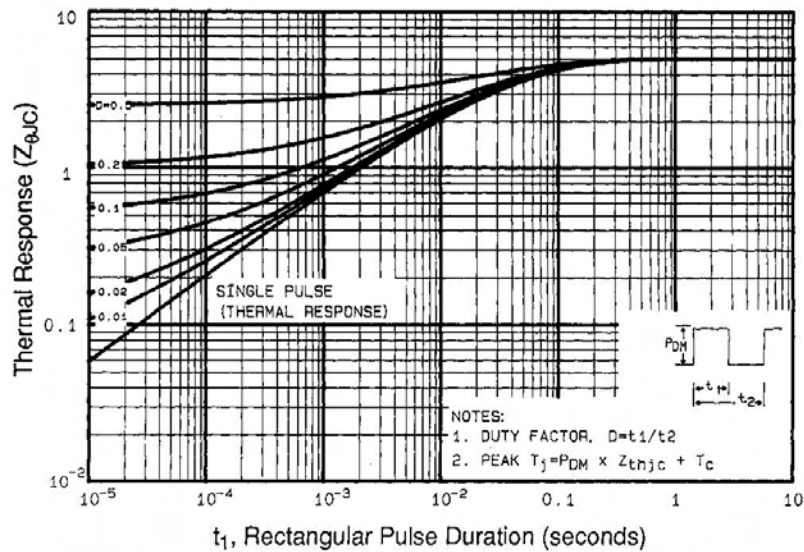
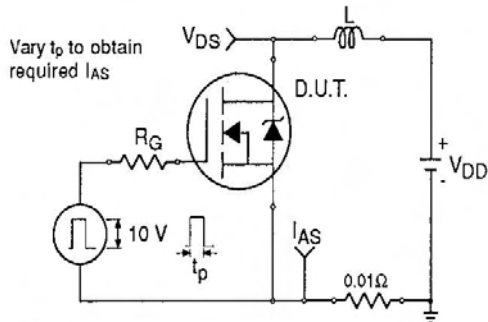
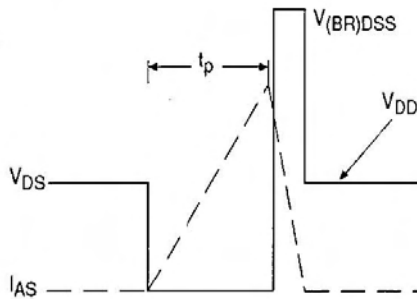


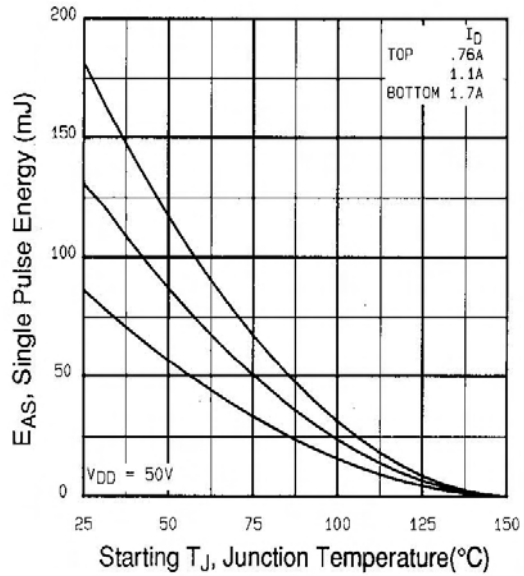
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



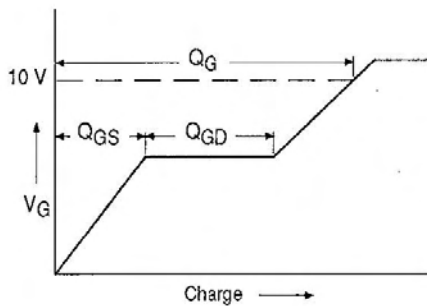
**Fig 12a.** Unclamped Inductive Test Circuit



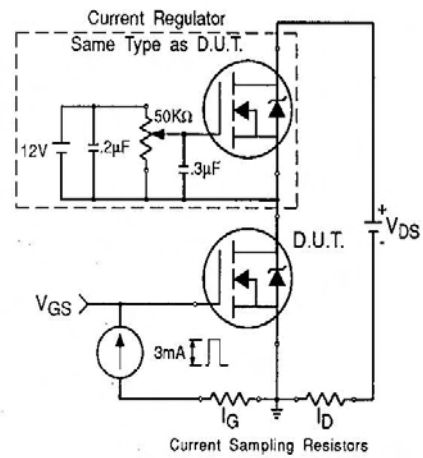
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

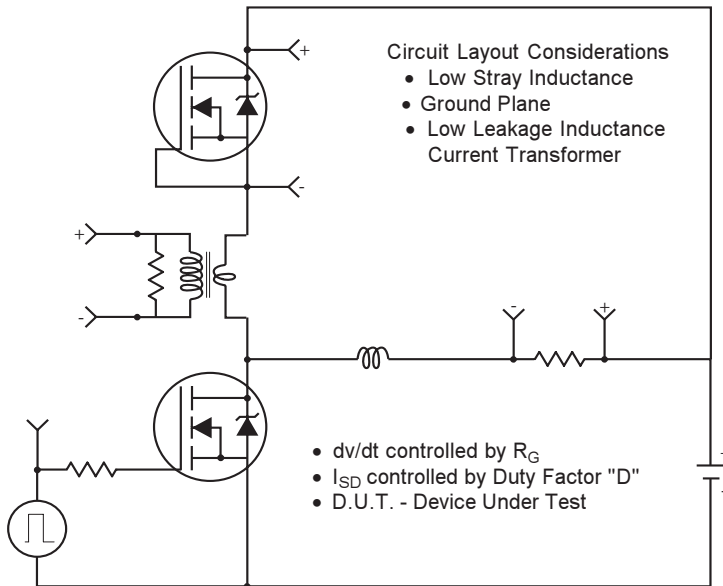


**Fig 13a.** Basic Gate Charge Waveform



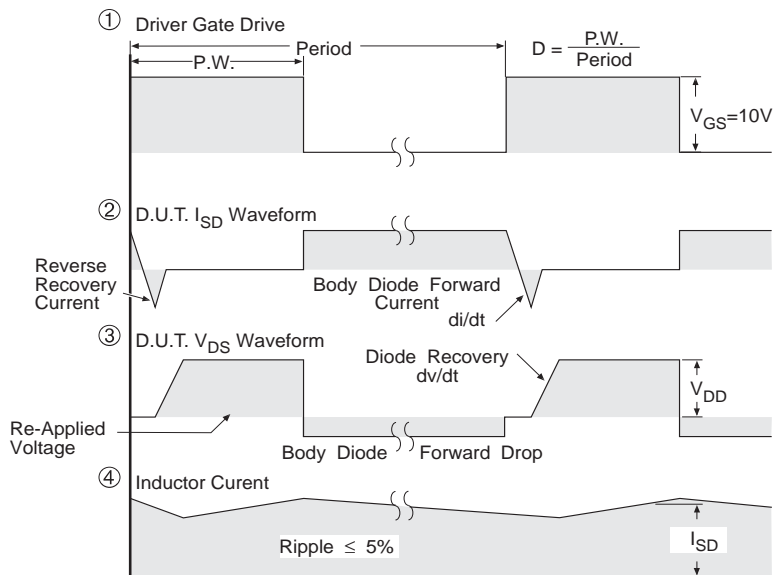
**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



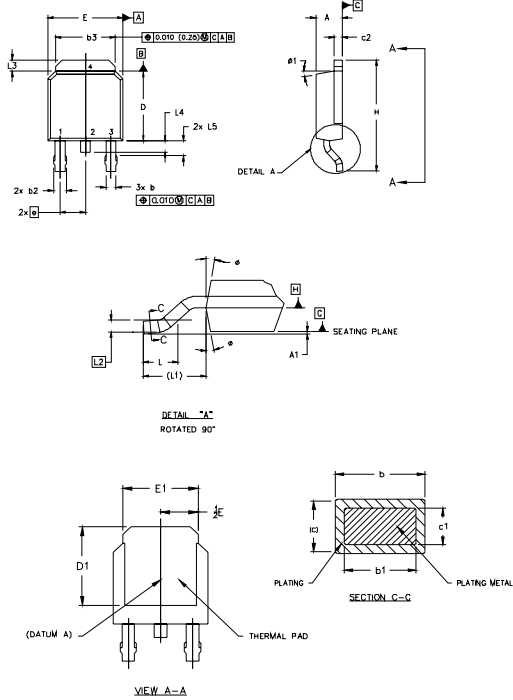
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and  $3V$  Drive Devices

**Fig 14** For N Channel HEXFETS

# IRFR/U310PbF

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M-1994.
  - 2.0 DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
  - 3.0 LEAD DIMENSION UNCONTROLLED IN L5
  - 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
  - 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

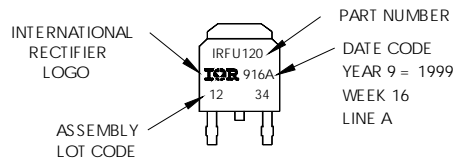
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.15		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.206	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29		.090 BSC		
H	8.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.021 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
e	0"	10"	0"	10"	
e1	0"	15"	0"	15"	

- LEAD ASSIGNMENTS
- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN
- IGBTs, CoPACK
- 1.- GATE
  - 2.- COLLECTOR
  - 3.- EMITTER
  - 4.- COLLECTOR

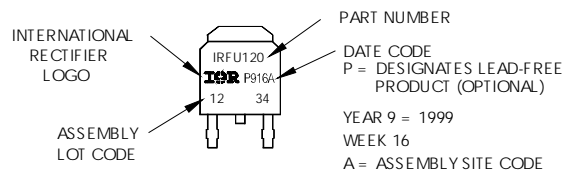
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON VV 16, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position  
indicates "Lead-Free"



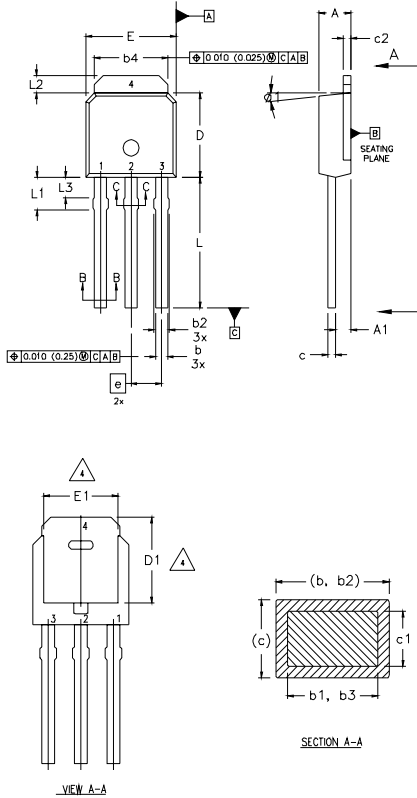
OR





## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

**LEAD ASSIGNMENTS**

**HEXFET**

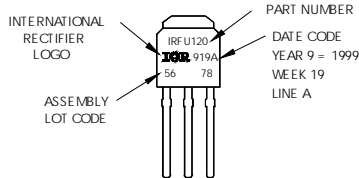
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	ø	15°	ø	15°	

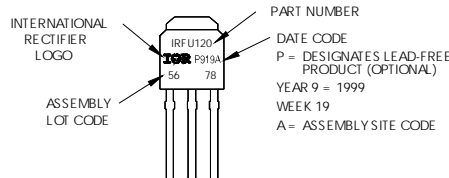
## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
WITH ASSEMBLY  
LOT CODE 5678  
ASSEMBLED ON WW 19, 1999  
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line  
position indicates "Lead-Free"



**OR**

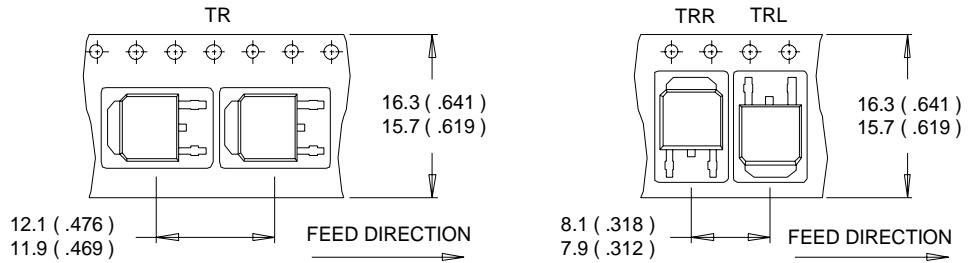


# IRFR/U310PbF

International  
**IR** Rectifier

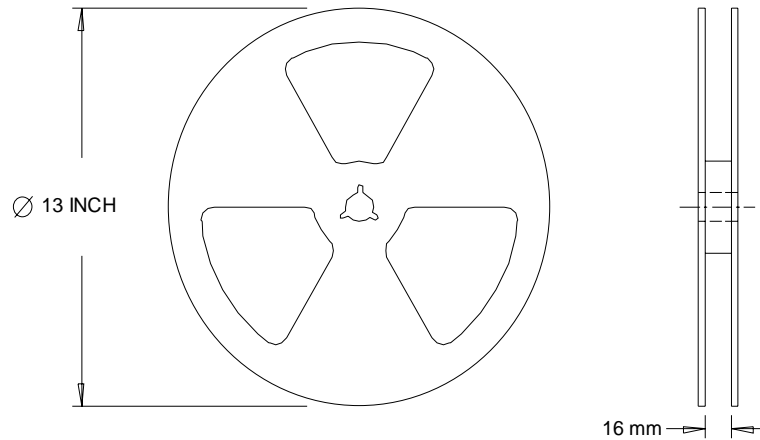
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

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