

2.0A SBR[®]
Surface Mount Super Barrier Rectifier
PowerDI[™]123

NEW PRODUCT

Features

- Low Forward Voltage Drop
- Low Leakage Current
- Superior Reverse Avalanche Capability
- Excellent High Temperature Stability
- Patented Interlocking Clip Design for High Surge Current Capacity
- Patented Super Barrier Rectifier Technology
- Soft, Fast Switching Capability
- 150°C Operating Junction Temperature
- ±16KV ESD Protection (HBM, 3B)
- ±25KV ESD Protection (IEC61000-4-2 Level 4, Air Discharge)
- **Lead Free Finish, RoHS Compliant (Note 1)**
- **“Green” Molding Compound (No Br, Sb)**
- **Qualified to AEC-Q 101 Standards for High Reliability**

Mechanical Data

- Case: PowerDI[™]123
- Case Material: Molded Plastic, “Green” Molding compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Polarity Indicator: Cathode Band
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 (E3)
- Marking Information: See Page 4
- Ordering Information: See Page 4

Maximum Ratings @ T_A = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load.
 For capacitive load, derate current by 20%.

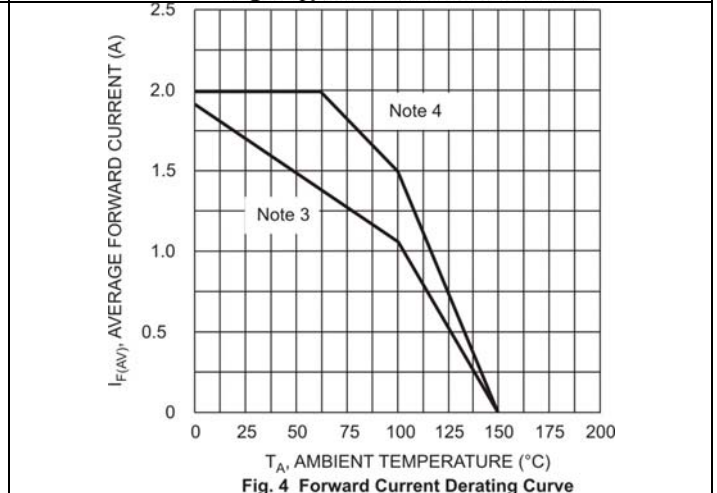
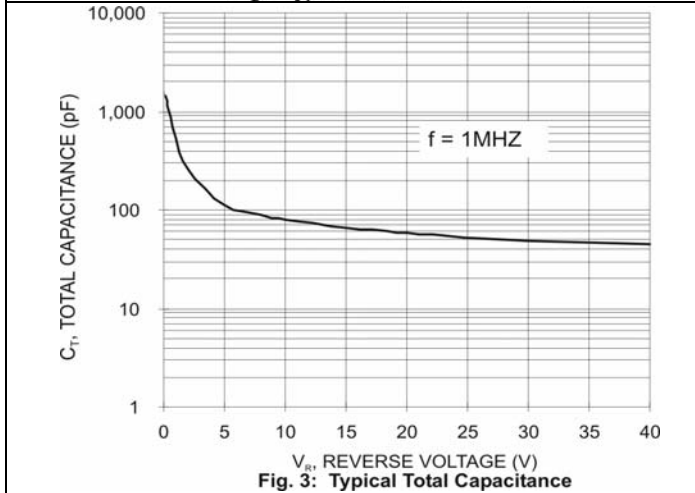
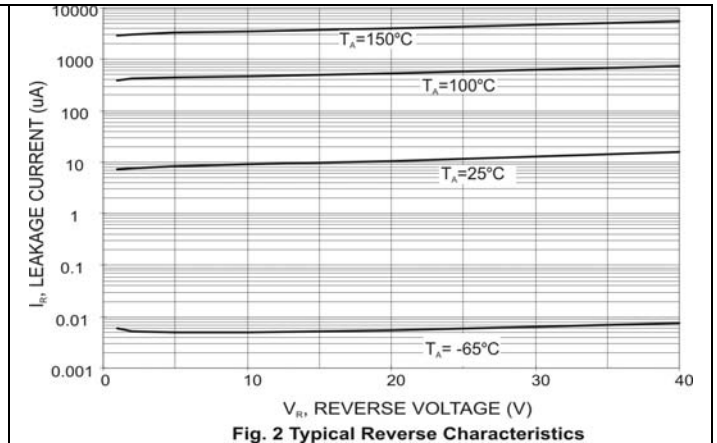
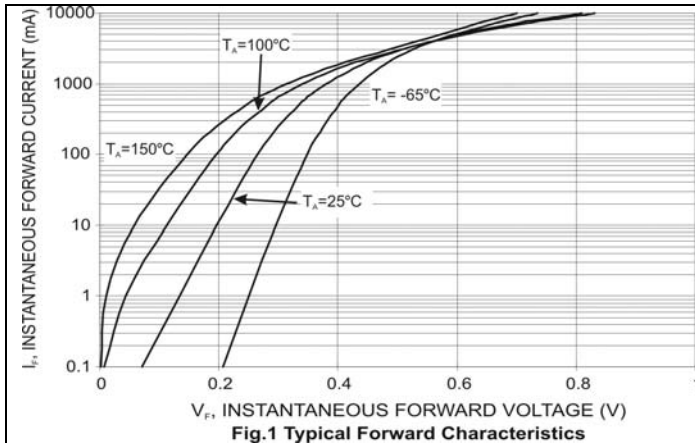
Characteristic	Symbol	Value	Unit
Peak Repetitive Reverse Voltage	V _{RRM}	40	V
Working Peak Reverse Voltage	V _{RWM}		
DC Blocking Voltage	V _{RM}		
RMS Reverse Voltage	V _{R(RMS)}	28	V
Average Rectified Output Current (See Figure 1)	I _O	2.0	A
Non-Repetitive Peak Forward Surge Current 8.3ms Single Half Sine-Wave Superimposed on Rated Load	I _{FSM}	50	A
Maximum Thermal Resistance	R _{θJS}	5	°C/W
Thermal Resistance Junction to Soldering (Note 2)	R _{θJA}	180	
Thermal Resistance Junction to Ambient (Note 3)	R _{θJA}	115	
Thermal Resistance Junction to Ambient (Note 4)	R _{θJA}	115	
Operating and Storage Temperature Range	T _J , T _{STG}	-65 to +150	°C

- Notes:
1. RoHS revision 13.2.2003. High temperature solder exemption applied, see *EU Directive Annex Note 7*.
 2. Theoretical R_{θJS} calculated from the top center of the die straight down to the PCB cathode tab solder junction.
 3. FR-4 PCB, 2 oz. Copper, minimum recommended pad layout per <http://www.diodes.com/datasheets/ap02001.pdf>.
 4. Polyimide PCB, 2 oz. Copper, minimum recommended pad layout per <http://www.diodes.com/datasheets/ap02001.pdf>.

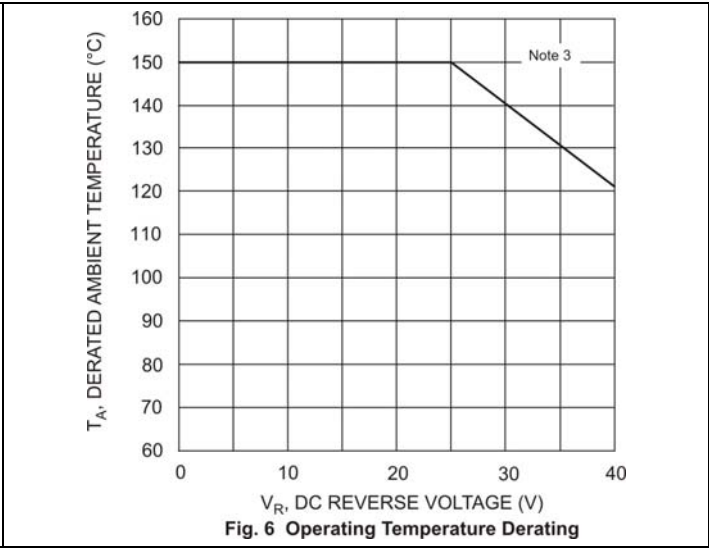
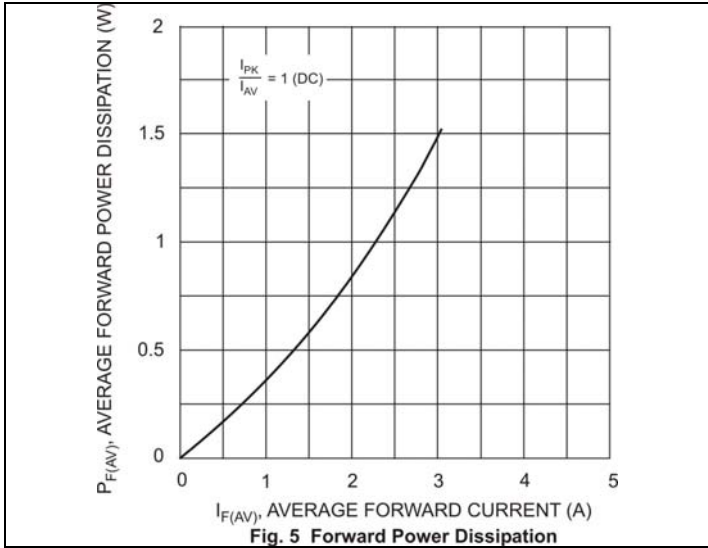
Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Breakdown Voltage (Note 5)	$V_{(BR)R}$	40	-	-	V	$I_R = 100 \mu\text{A}$
Forward Voltage Drop	V_F	-	0.265	0.315	V	$I_F = 0.1\text{A}, T_J = 25^\circ\text{C}$
		-	0.38	0.43		$I_F = 1.0\text{A}, T_J = 25^\circ\text{C}$
		-	0.45	0.50		$I_F = 2.0\text{A}, T_J = 25^\circ\text{C}$
		-	0.17	0.22		$I_F = 0.1\text{A}, T_J = 125^\circ\text{C}$
		-	0.325	0.375		$I_F = 1.0\text{A}, T_J = 125^\circ\text{C}$
Leakage Current (Note 5)	I_R	-	8	40	μA	$V_R = 5\text{V}, T_J = 25^\circ\text{C}$
		-	16	100	μA	$V_R = 40\text{V}, T_J = 25^\circ\text{C}$
		-	1.3	8	mA	$V_R = 5\text{V}, T_J = 125^\circ\text{C}$
			2.1	10	mA	$V_R = 40\text{V}, T_J = 125^\circ\text{C}$

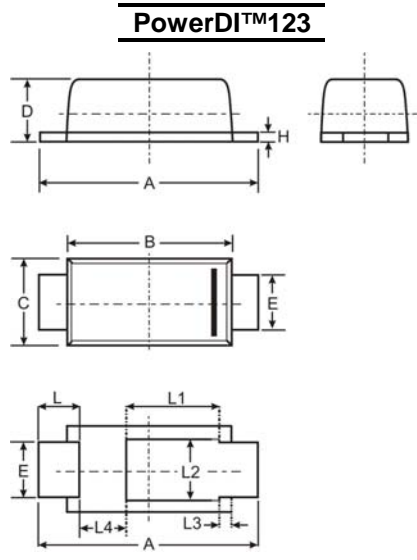
Notes: 5. Short duration pulse test used to minimize self-heating effect.



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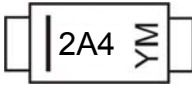


Package Outline Drawings



PowerDI™123			
Dim	Min	Max	Typ
A	3.65	3.75	3.70
B	2.775	2.825	2.80
C	1.750	1.800	1.775
D	0.955	1.000	0.98
E	0.95	1.05	1.00
H	0.15	0.25	0.20
L	0.60	0.70	0.65
L1	—	—	1.36
L2	—	—	1.10
L3	—	—	0.20
L4	0.95	1.25	1.05
All Dimensions in mm			

Marking, Polarity, Weight & Ordering Information

SBR2A40P1	Case Style		Marking	Weight
	 Top View	 Back View		0.096g (approx.)

Ordering Information	Date Code
SBR2A40P1-7 3000/Tape & Reel	2A4 = Product Type Marking Code YM = Date Code Marking Y = Year (ex: T = 2006) M = Month (ex: 9 = September)

Date Code Key

Year	2006	2007	2008	2009	2010	2011	2012
Code	T	U	V	W	X	Y	Z

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

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