NTLTD7900ZR2

Power MOSFET

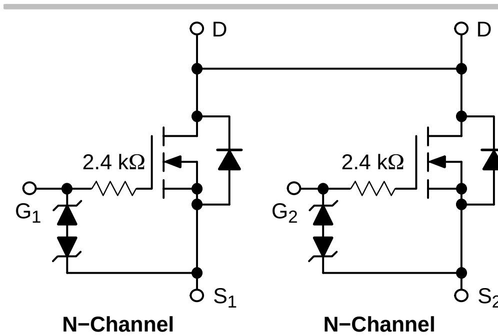
9 A, 20 V, Logic Level, N−Channel Micro−8 Leadless

EZFETs™ are an advanced series of Power MOSFETs which contain monolithic back−to−back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc−dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones.

ON Semiconductor®

http://onsemi.com

9 AMPERES
20 VOLTS
$R_{DS(on)}$ = 26 mΩ
(V_{GS} = 4.5 V, I_D = 6.5 A)
$R_{DS(on)}$ = 31 mΩ
(V_{GS} = 2.5 V, I_D = 5.8 A)



Applications

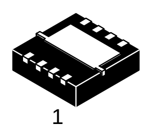
- Zener Protected Gates Provide Electrostatic Discharge Protection
- Designed to Withstand 4000 V Human Body Model
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive − Can be Driven by Logic ICs
- Micro−8 Leadless Surface Mount Package − Saves Board Space
- I_{DSS} Specified at Elevated Temperature

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	10 Secs	Steady State	Unit
Drain−to−Source Voltage	V_{DSS}	20		V
Gate−to−Source Voltage	V_{GS}	±12		V
Continuous Drain Current (Note 1) T_A = 25°C T_A = 85°C	I_D	 9.0 6.4	 6.0 4.3	A
Pulsed Drain Current (tp ≤ 10 μs)	I_{DM}	30		A
Continuous Source−Diode Conduction (Note 1)	I_s	2.9	1.4	A
Total Power Dissipation (Note 1) T_A = 25°C T_A = 85°C	P_D	 3.2 1.7	 1.5 0.79	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to 150		°C
Thermal Resistance (Note 1) Junction−to−Ambient	$R_{\theta JA}$	38	82	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to 1″ x 1″ FR−4 board.



Micro−8 Leadless
CASE 846C

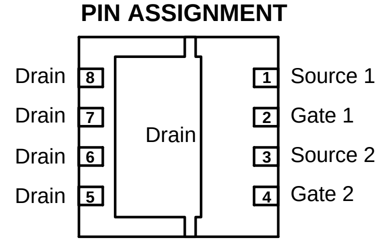
MARKING DIAGRAM

1

7900
AYWW

A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NTLTD7900ZR2	Micro−8 LL	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 2) (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	20	24	–	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 85°C)		I_{DSS}	– –	– –	1.0 20	μAdc
Gate−Body Leakage Current (V_{GS} = ±4.5 Vdc, V_{DS} = 0 Vdc) (V_{GS} = ±12 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	– –	– –	1.0 500	μAdc μAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (Note 2) (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	0.4	0.67	1.0	Vdc
Static Drain−to−Source On−Resistance (Note 2) (V_{GS} = 4.5 Vdc, I_D = 6.5 Adc) (V_{GS} = 2.5 Vdc, I_D = 5.8 Adc)		$R_{DS(on)}$	– –	21 27	26 31	mΩ
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	–	7.4	15	pF
Output Capacitance		C_{oss}	–	237	400	
Transfer Capacitance		C_{rss}	–	4.1	10	pF
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{GS} = 4.5 Vdc, V_{DD} = 10 Vdc, I_D = 1.0 Adc, R_G = 9.1 Ω) (Note 2)	$t_{d(on)}$	–	0.55	1.0	μs
Rise Time		t_r	–	1.17	2.0	
Turn−Off Delay Time		$t_{d(off)}$	–	1.87	3.0	
Fall Time		t_f	–	4.8	7.0	μs
Gate Charge	(V_{GS} = 4.5 Vdc, I_D = 6.5 Adc, V_{DS} = 10 Vdc) (Note 2)	Q_T	–	12	18	nC
		Q_1	–	0.7	–	
Gate Charge		Q_2	–	3.7	–	nC
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 85°C) (Note 2)	V_{SD}	– –	0.69 0.62	0.8 –	Vdc

2. Pulse Test: Pulse Width • 300 μs, Duty Cycle • 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

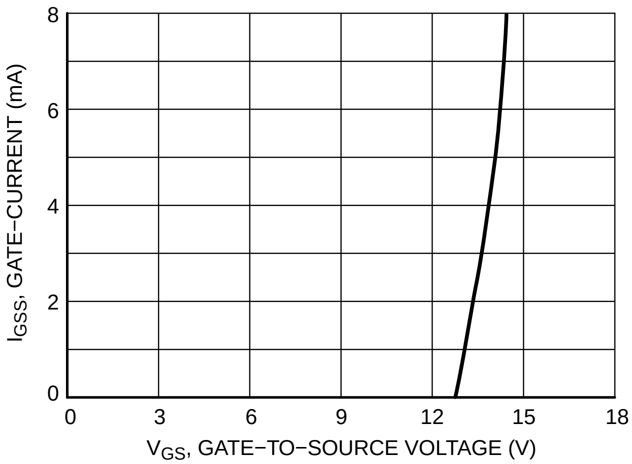


Figure 1. Gate−Current versus Gate−Source Voltage

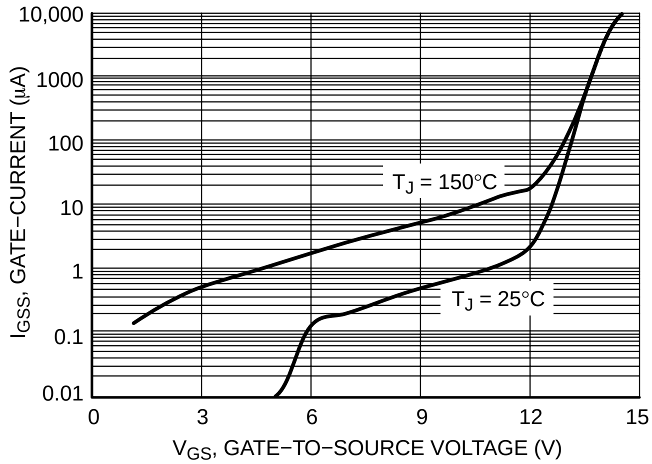


Figure 2. Gate−Current versus Gate−Source Voltage

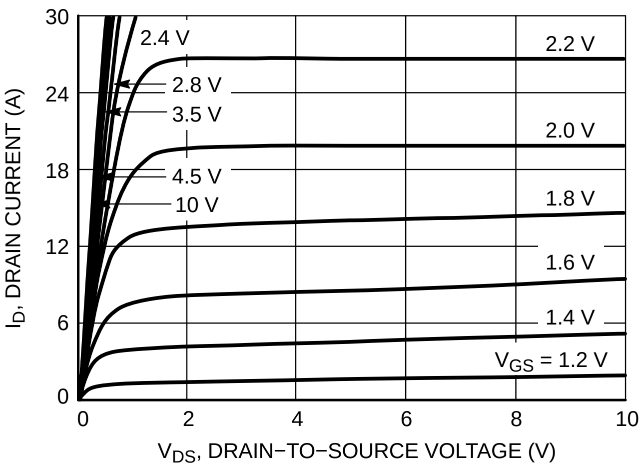


Figure 3. On−Region Characteristics

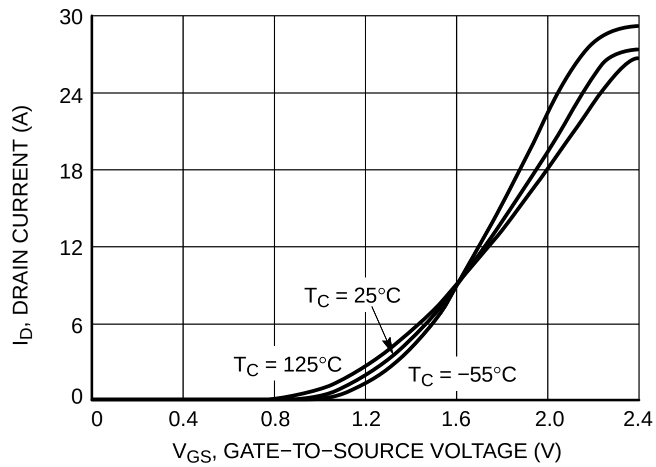


Figure 4. Transfer Characteristics

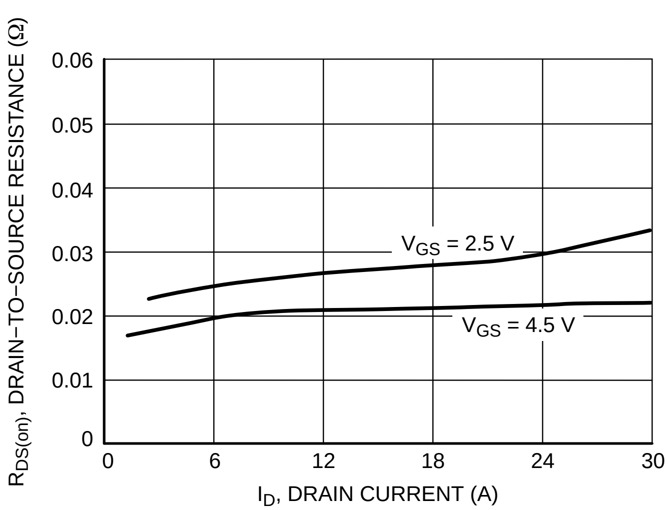


Figure 5. On−Resistance versus Drain Current

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{In} [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \text{In} (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

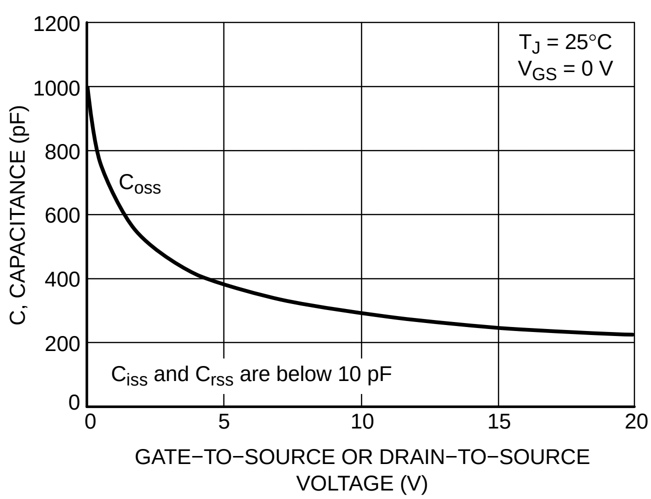


Figure 6. Capacitance Variation

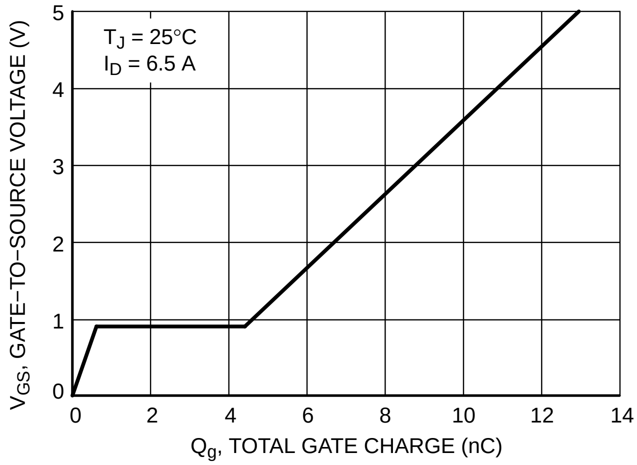


Figure 7. Gate−to−Source

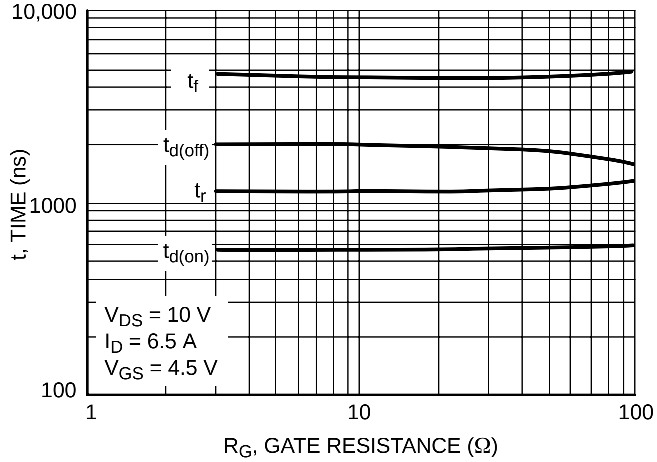


Figure 8. Resistive Switching Time Variation versus Gate Resistance

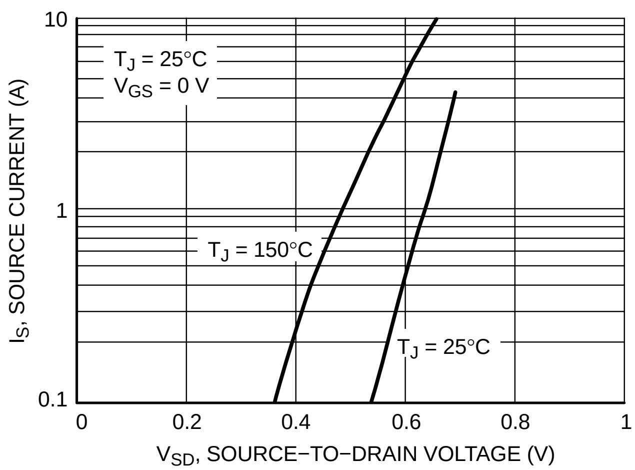


Figure 9. Diode Forward Voltage versus Current

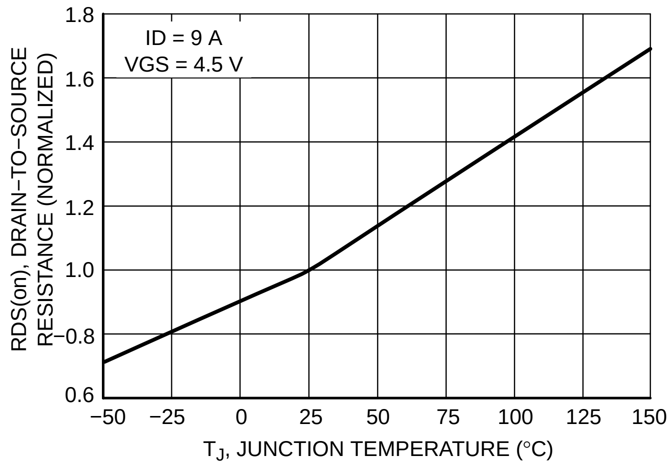


Figure 10. On−Resistance Variation with Temperature

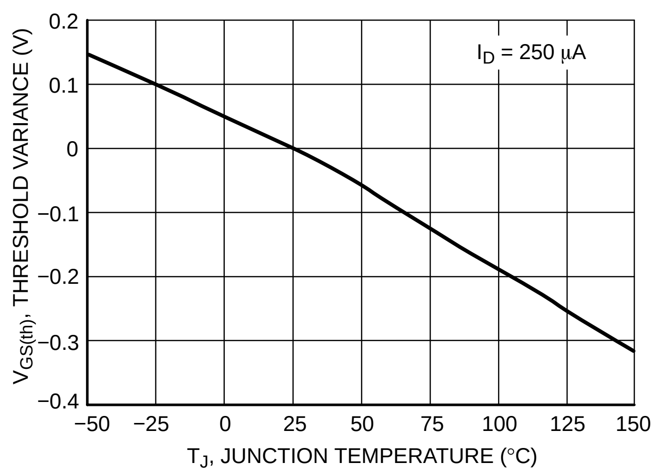


Figure 11. Threshold Voltage

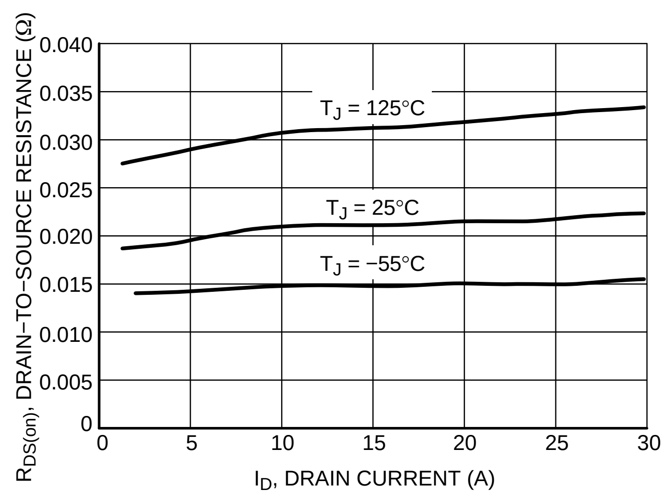


Figure 12. On−Resistance versus Drain Current and Temperature

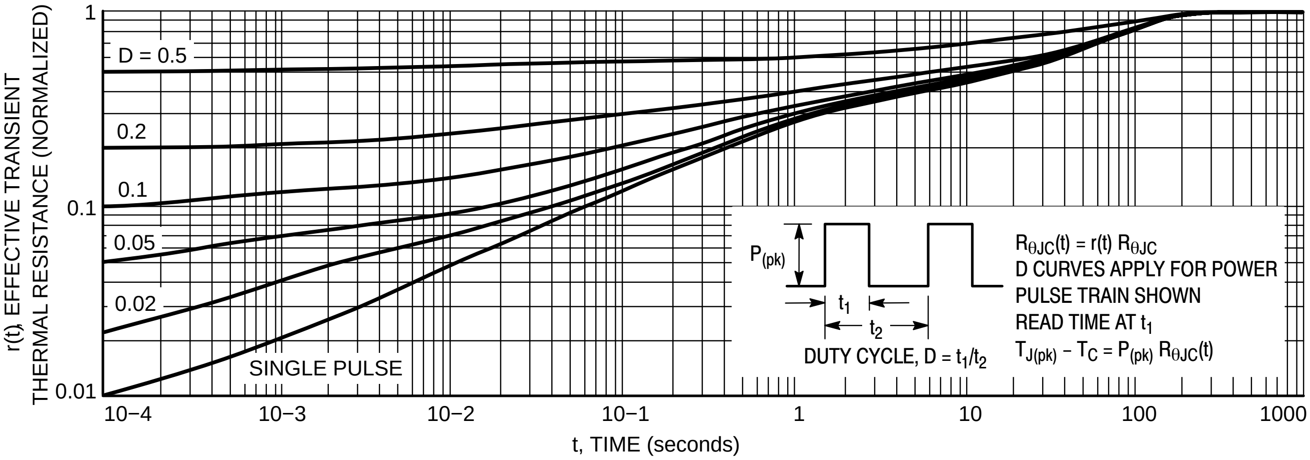
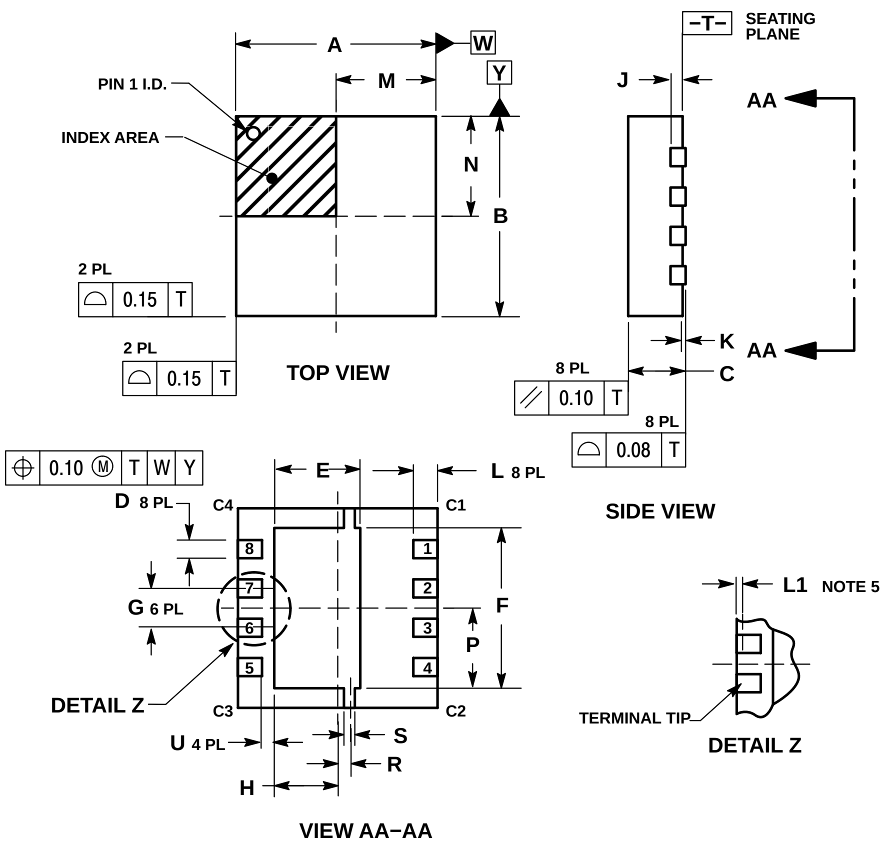


Figure 13. Thermal Response

PACKAGE DIMENSIONS

Micro−8 Leadless
CASE 846C−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95−1 SPP−012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
4. DIMENSION D APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 0.30 MM FROM TERMINAL TIP. DIMENSION L1 IS THE TERMINAL PULL BACK FROM PACKAGE EDGE, UP TO 0.1 MM IS ACCEPTABLE. L1 IS OPTIONAL.
5. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

	MILLIMETERS	
DIM	MIN	MAX
A	3.20	3.40
B	3.20	3.40
C	0.85	0.95
D	0.28	0.33
E	1.30	1.50
F	2.55	2.75
G	0.65 BSC	
H	0.95	1.15
J	0.25 BSC	
K	0.00	0.05
L	0.35	0.45
M	1.60	1.70
N	1.60	1.70
P	1.28	1.38
R	0.200	0.250
S	0.18	0.23
U	0.20	---

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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