

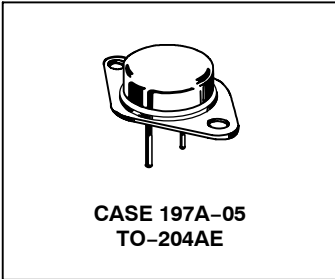
# High-Current Complementary Silicon Power Transistors

... designed for use in high-power amplifier and switching circuit applications.

- High Current Capability –  
 $I_C$  Continuous = 50 Amperes.
- DC Current Gain –  
 $h_{FE} = 15-60 @ I_C = 25 \text{ Adc}$
- Low Collector-Emmitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ Vdc (Max) @ } I_C = 25 \text{ Adc}$
- **These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices. Please see our website at [www.onsemi.com](http://www.onsemi.com) for specific Pb-free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**

**PNP  
2N5684  
NPN  
2N5686**

**50 AMPERE  
COMPLEMENTARY  
SILICON  
POWER TRANSISTORS  
60-80 VOLTS  
300 WATTS**



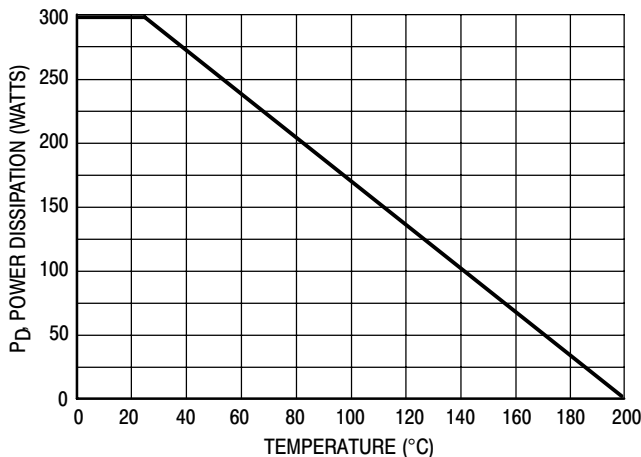
## MAXIMUM RATINGS (1)

Rating	Symbol	2N5684 2N5686	Unit
Collector-Emmitter Voltage	$V_{CEO}$	80	Vdc
Collector-Base Voltage	$V_{CB}$	80	Vdc
Emmitter-Base Voltage	$V_{EB}$	5.0	Vdc
Collector Current – Continuous	$I_C$	50	Adc
Base Current	$I_B$	15	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 1.715	Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

## THERMAL CHARACTERISTICS (1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.584	$^\circ\text{C/W}$

(1) Indicates JEDEC Registered Data.



**Figure 1. Power Derating**

Safe Area Curves are indicated by Figure 5. All limits are applicable and must be observed.

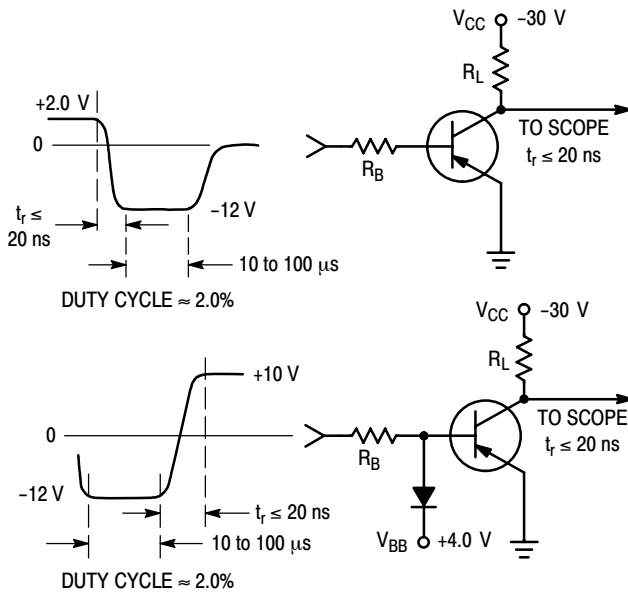
# 2N5684 2N5686

## \*ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 2) ( $I_C = 0.2 \text{ Adc}$ , $I_B = 0$ )	$V_{CEO(sus)}$	80	–	Vdc
Collector Cutoff Current ( $V_{CE} = 40 \text{ Vdc}$ , $I_B = 0$ )	$I_{CEO}$	–	1.0	mAdc
Collector Cutoff Current ( $V_{CE} = 80 \text{ Vdc}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ ) ( $V_{CE} = 80 \text{ Vdc}$ , $V_{EB(off)} = 1.5 \text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	$I_{CEX}$	–	2.0 10	mAdc
Collector Cutoff Current ( $V_{CB} = 80 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	2.0	mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	5.0	mAdc
<b>ON CHARACTERISTICS</b>				
DC Current Gain (Note 2) ( $I_C = 25 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ ) ( $I_C = 50 \text{ Adc}$ , $V_{CE} = 5.0 \text{ Vdc}$ )	$h_{FE}$	15 5.0	60 –	–
Collector–Emitter Saturation Voltage (Note 2) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ ) ( $I_C = 50 \text{ Adc}$ , $I_B = 10 \text{ Adc}$ )	$V_{CE(sat)}$	–	1.0 5.0	Vdc
Base–Emitter Saturation Voltage (Note 1) ( $I_C = 25 \text{ Adc}$ , $I_B = 2.5 \text{ Adc}$ )	$V_{BE(sat)}$	–	2.0	Vdc
Base–Emitter On Voltage (Note 1) ( $I_C = 25 \text{ Adc}$ , $V_{CE} = 2.0 \text{ Vdc}$ )	$V_{BE(on)}$	–	2.0	Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain – Bandwidth Product ( $I_C = 5.0 \text{ Adc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f = 1.0 \text{ MHz}$ )	$f_T$	2.0	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ )	$C_{ob}$	–	2000 1200	pF
Small–Signal Current Gain ( $I_C = 10 \text{ Adc}$ , $V_{CE} = 5.0 \text{ Vdc}$ , $f = 1.0 \text{ kHz}$ )	$h_{fe}$	15	–	

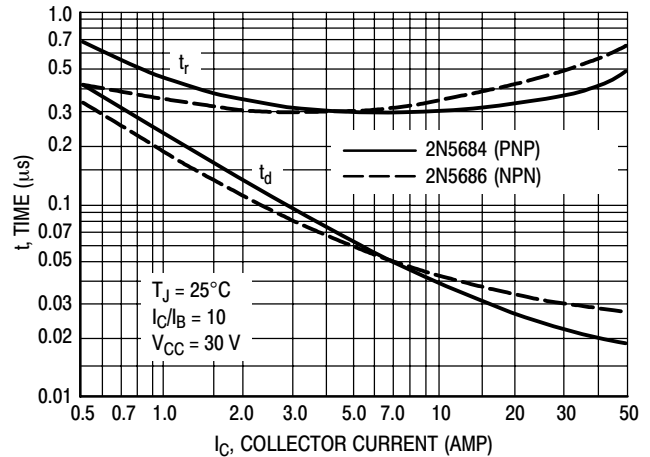
\*Indicates JEDEC Registered Data.

Note 2: Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .



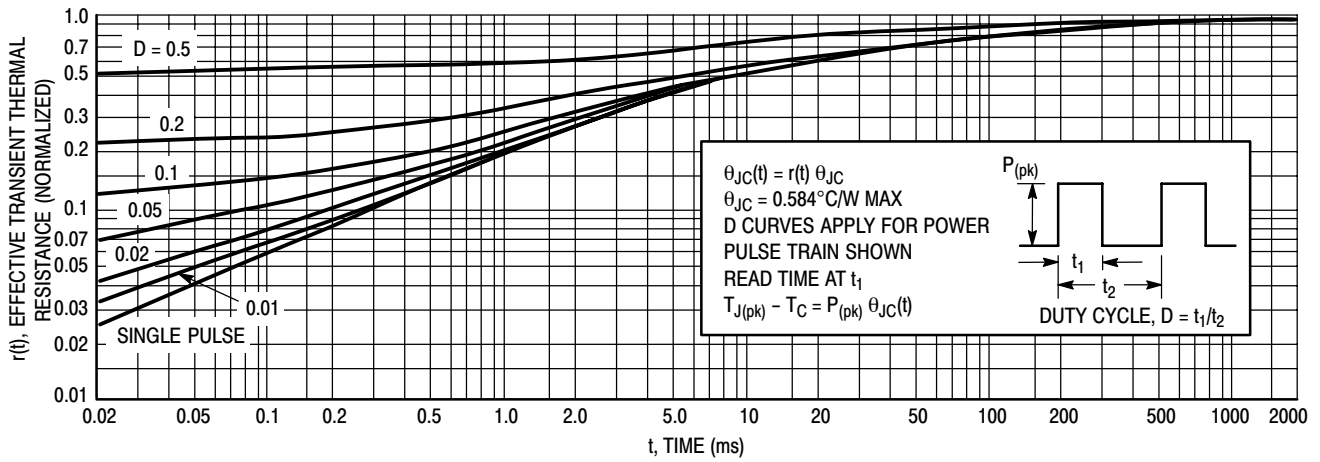
FOR CURVES OF FIGURES 3 & 6,  $R_B$  &  $R_L$  ARE VARIED.  
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.  
FOR NPN CIRCUITS, REVERSE ALL POLARITIES.

**Figure 2. Switching Time Test Circuit**

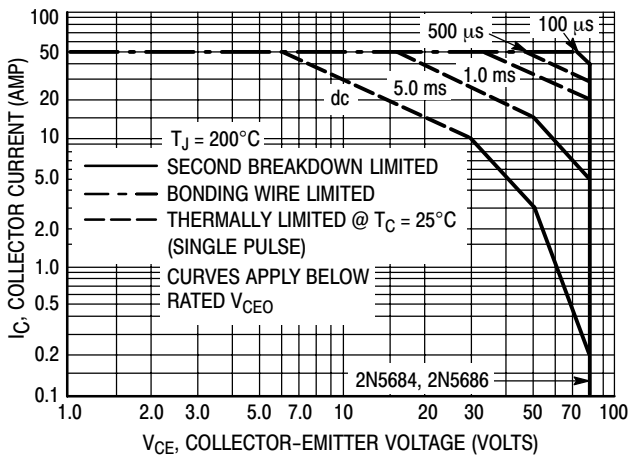


**Figure 3. Turn–On Time**

## 2N5684 2N5686



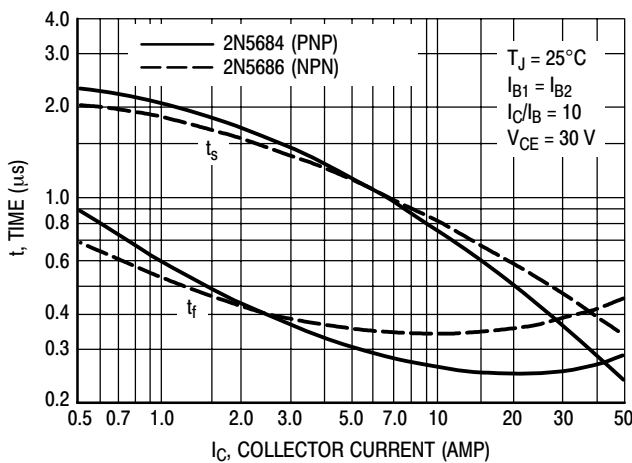
**Figure 4. Thermal Response**



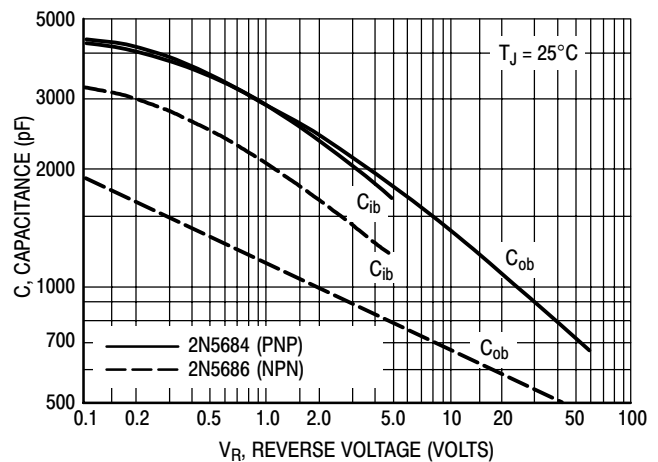
**Figure 5. Active-Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



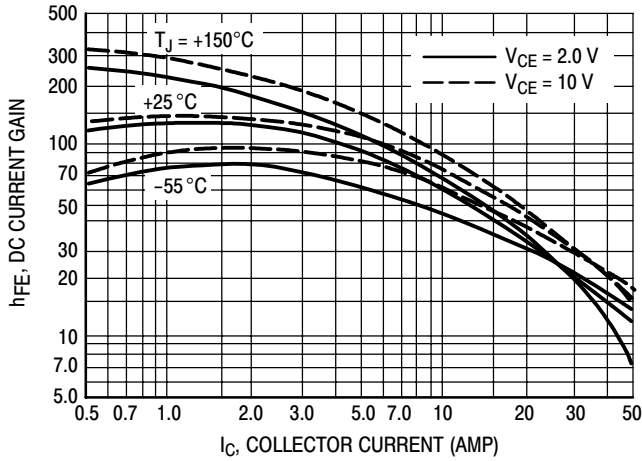
**Figure 6. Turn-Off Time**



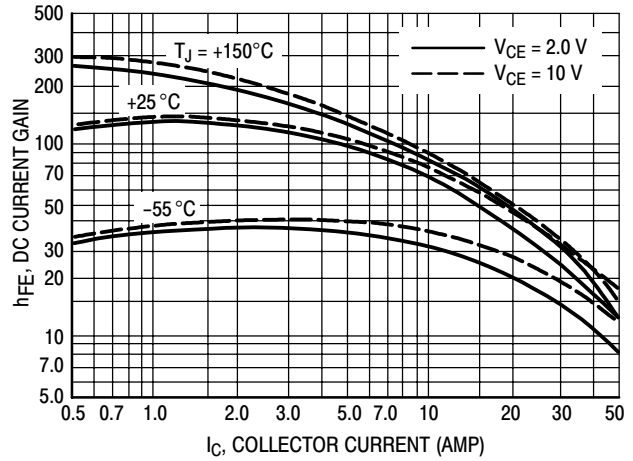
**Figure 7. Capacitance**

# 2N5684 2N5686

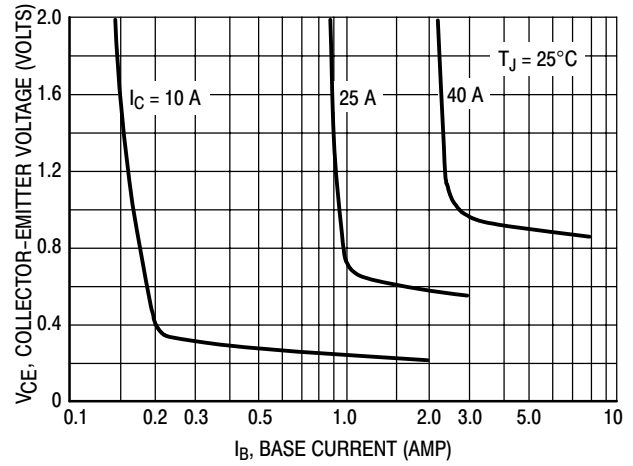
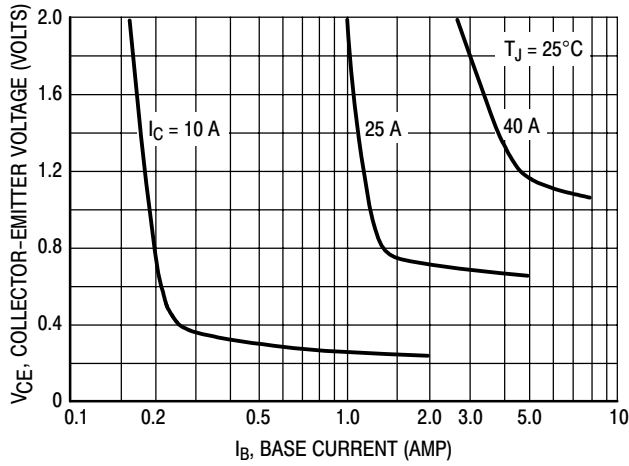
**PNP  
2N5684**



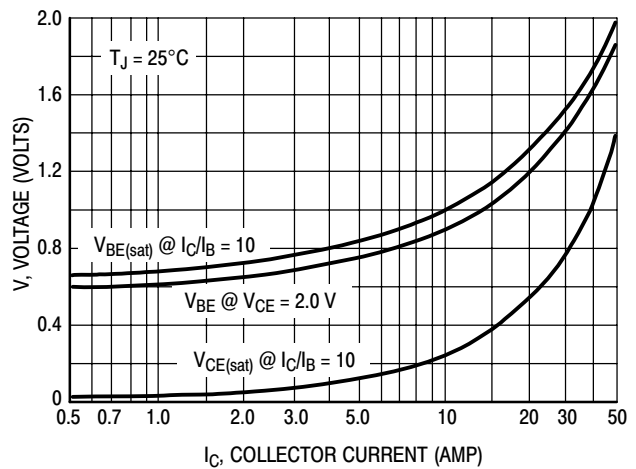
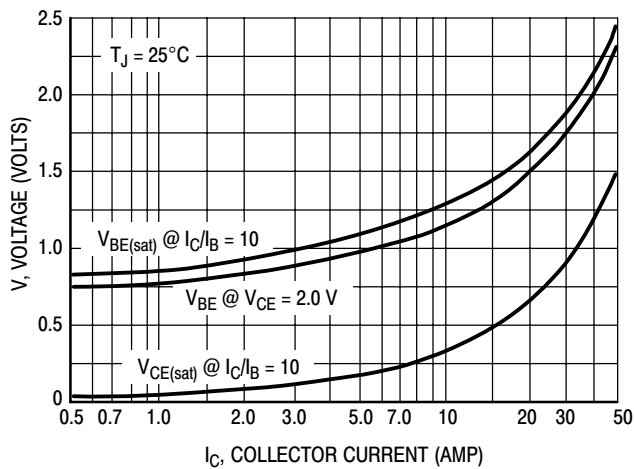
**NPN  
2N5686**



**Figure 8. DC Current Gain**



**Figure 9. Collector Saturation Region**



**Figure 10. "On" Voltages**



## Notes

# Notes

**ON Semiconductor** and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.