## CMOS 4–Bit Microcontroller

**TMP47C430N**

**TMP47C430M**

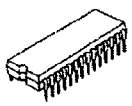
The 47C430 is based on the TLCS-470 CMOS series. The 47C430 have on-screen display circuit (OSD) to display characters and marks which indicate channel or time on TV screen, A/D converter (comparator) input, and D/A converter output such as TV.

| Part No. | ROM | RAM | Package |
|---|---|---|---|
| TMP47C430N | 4096 x 8-bit | 256 x 4-bit | SDIP28-P-400 |
| TMP47C430M | | | SOP28-P-450 |

### Features

- 4-bit single chip microcomputer
- Instruction execution time: 1.9$\mu$s (at 4.2MHz),
- 92 basic instructions
- Table look-up instructions
- Subroutine nesting: 15 levels max.
- 5 interrupt sources (External: 2, Internal: 3)
  All sources have independent latches each, and multiple interrupt control is available.
- I/O port (19 pins)
  - Input 2 ports 5 pins
  - I/O 5 ports 14 pins
- Interval Timer
- Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- Watchdog Timer
- On-screen display circuit
  - Character patterns: 48 characters
  - Characters displayed: 16 columns x 2 lines
  - Composition: 8 x8 dots (smoothing function)
  - Size of character: 2 kinds (line by line)
  - Color of character: 3 kinds (character by character)
  - Variable display position: Horizontal/vertical 64 steps
- D/A converter (Pulse width modulation) outputs
  - 14-bit resolution 1 channel
  - 6-bit resolution 1 channels
- 4-bit A/D converter (Comparator) input (4 channels)
- Horizontal synchronous signal is detected by timer/counter
- Remote control signal preprocessing capability
- High current outputs
  LED direct drive capability (typ. 20mA x 4 bits).
- Hold function: Battery/Capacitor back-up

SDIP28-P-400

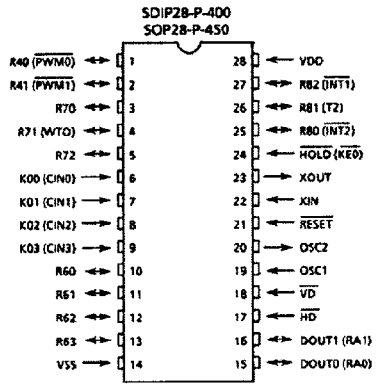


TMP47C430N

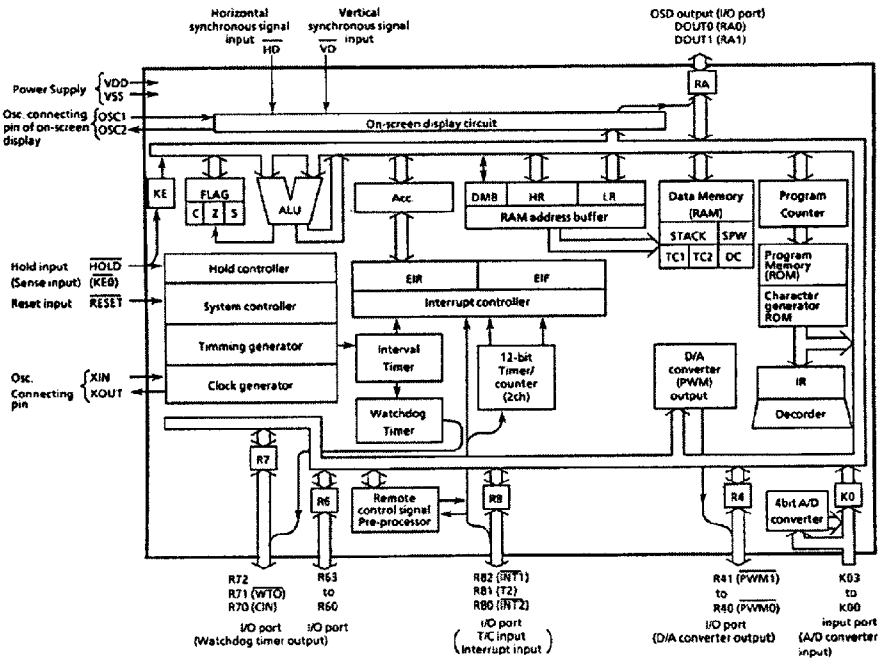
SOP28-P-450

TMP47C430M

## Pin Assignments (Top View)




## Block Diagram



## Pin Function

| Pin Name | Input/Output | Function | |
|---|---|---|---|
| K03 to K00 | Input | 4-bit input port | 4-bit A/D Converter input |
| R41 ($\overline{PWM1}$) | I/O (output) | 2-bit I/O port with latch.<br>When used as input port or D/A converter outputs pins, the latch must be set to "1". | 6-bit D/A converter (PWM) output |
| R40 ($\overline{PWM0}$) | | | 14-bit D/A converter (PWM) output |
| R63 to R60 | I/O | 4-bit I/O port with latch.<br>When used as input port, the latch must be set to "1". | |
| R72 | I/O | 4-bit I/O port with latch. | |
| R71 ($\overline{WTO}$) | I/O (output) | When used as input port, watchdog timer output pin, or A/D converter input pin, the latch must be set to "1". | Watchdog timer output |
| R70 (CIn) | I/O (input) | | |
| R82 ($\overline{INT1}$) | I/O (output) | 4-bit I/O port with latch.<br>When used as input port, external interrupt input pin, or timer/counter external input pin, the latch must be set to "1". | External interrupt 1 input |
| R81 (T2) | I/O (Input) | | Timer/Counter 2 external input |
| R80 ($\overline{INT2}$) / $\overline{HOLD}$ | I/O (Input) | | External interrupt 2 input |
| DOUT1 (RA1) | Output (I/O) | RGB Output | 2-bit I/O port with latch.<br>When used as input port, the latch must be set to "1" |
| DOUT0 (RA0) | | | |
| $\overline{HD}$, $\overline{VD}$ | Input | Horizontal synchronous signal input, Vertical synchronous signal input | |
| OSC1, OSC2 | input, output | Resonator connecting pin of on-screen display circuit | |
| XIN, XOUT | input, output | Resonator connecting pin.<br>For inputting external clock, XIN is used and XOUT is opened. | |
| $\overline{RESET}$ | Input | Reset signal input | |
| $\overline{HOLD}$ ($\overline{KE0}$) | input (input) | HOLD request/release signal input | Sense input |
| VDD | Power Supply | +5V | |
| VSS | | 0V (GND) | |

## Operational Description

## 1. System Configuration

- Internal CPU Function

  They are the same as those of the 47C660/860 except program memory (ROM), data memory (RAM) and system clock controller.

- Peripheral Hardware Function

  ① Input/Output Ports

  ② Interval Timer

  ③ Timer/Counters (TC1,TC2)

  ④ Watchdog Timer

  ⑤ Remote control pulse detector

  ⑥ On-screen display (OSD) control circuit

  ⑦ A/D Converter (Comparator) input

  ⑧ D/A converter (Pulse Width Modulation) output

The description has been provide with priority on functions (①, ③, ⑥, ⑦, and⑧) added to and changed from 47C660/860.

## 2. Internal CPU Function

### 2.1 Program Memory (ROM)

Programs are stored in address 0000 to $0FFF_H$ of 47C430. By the ROM data reference instruction [LDH A,@DC+, LDL A,@DC], the fixed data in address 0000 to $0FFF_H$ can be loaded to the accumulator, respectively.

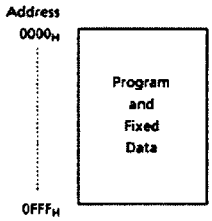



**Figure 2-1. Program Memory**

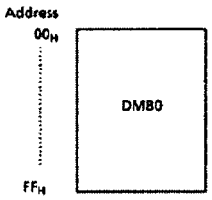



**Figure 2-2. Data Memory (RAM)**

### 2.2 Data Memory (RAM)

The 47C430 contains 256 x 4 bits data memory (DMB0).

### 2.3 Operation Clock Control

On the 47C430 only single clock mode is available. As single clock mode is automatically selected at the initialization, there is no necessary to set system clock control command register (OP16).

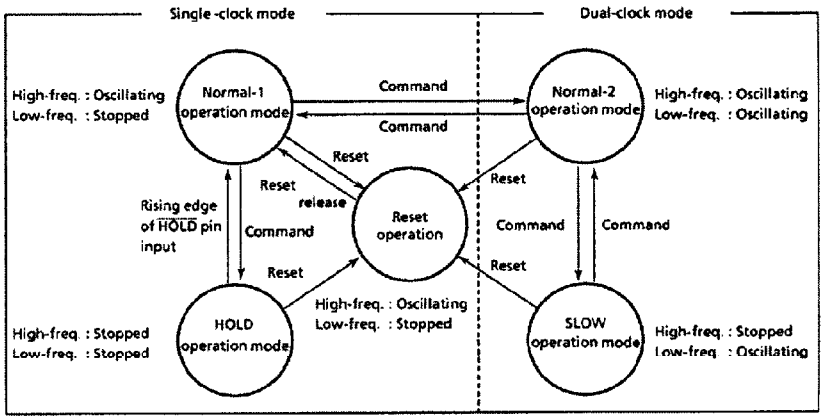



**Figure 2-3. Operation Mode Transition Diagram**

## 3. Peripheral Hardware Function

### 3.1 I/O Ports

The 47C434A/634A have 7 I/O ports (19 pins) each as follows

① K0 ; 4-bit input (shared with comparator inputs)

② R4 ; 2-bit input/output (shared with pulse width modulation output)

③ R6 ; 4-bit input/output

④ R7 ; 3-bit input/output (shared with comparator input and watchdog timer output)

⑤ R8 ; 3-bit input/output (shared with external interrupt input and timer/counter input)

⑥ RA ; 2-bit input/output (shared with on-screen display output)

⑦ KE ; 1-bit sense input (shared with hold request/release signal input)

The description has been provide with priority on functions (①, ②, ④ and ⑤) added to and changed from 47C660/860, and it describes port ⑥, which item of on-screen display circuit.

(1) Port K0 (K03-K00)

The 4-bit input port. Port K0 is shared digital input with the A/D converter (comparator) input. The K0 port input selector (OP13) determines whether this port is to be used for digital or comparator input. The most significant bit of the K0 port input selector is set to "1" for digital input and to "0" for comparator input.

The K0 port selector is initialized to "0" during reset.

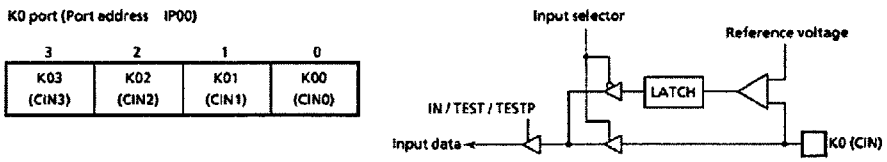



**Figure 3-1. Port K0**

(2) Port R4 (R41 to R40)

This is a 2-bit I/O port with latch. It is a port common to D/A converter (PWM) output port. R4 port output buffers are Tri-state, and each bit of them can be controlled independently by the program. Controlling the Tri-state is performed by the command register accessed as port address OP00. When some bit of the OP00 is 0, the corresponding bit of the output buffers becomes High-impedance state. The output latch should be set to "1" when the port is used as $\overline{\text{PWM}}$ output port, the $\overline{\text{PWM}}$ output should be to "H" level (PWM data is all "0") when the port is used as R4 port. The output buffers should be set to high impedance state, when the port is used as input port. And the R4 output latch be set to "1", $\overline{\text{PWM}}$ output be set to "High" level, and the output buffer be set to High-impedance state during reset.

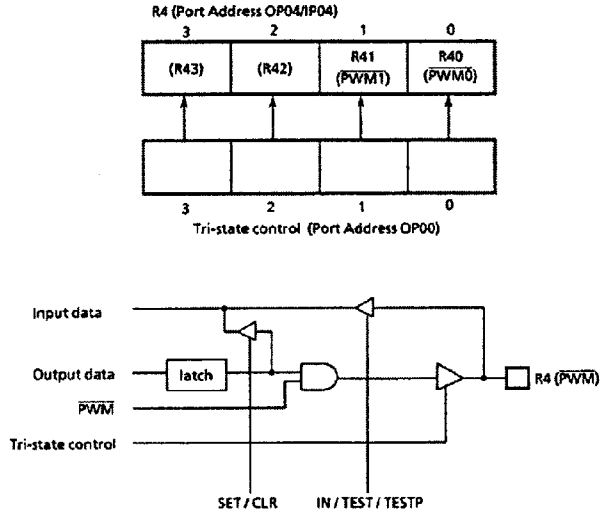



**Figure 3-2. Port R4 (PWM)**

(3) Port R7 (R72 to R70)

This is a 3-bit I/O port with latch.

R7 port output buffers are Tri-state, and each bit of them can be controlled independently by the program. Controlling the Tri-state is performed by the command register accessed as port address OP01. When some bit of the OP01 is 0, the corresponding bit of the output buffers becomes High-impedance state

Pin R71 (WTO) is shared with the watchdog timer output.

The output latch should be set to "1" when the port is used as WTO output port. The output buffers should be set to High impedance state, when the port is used as input port, and the output buffer be set to High-impedance state during reset. R73 pin does not exist actually but R73 has the latch.

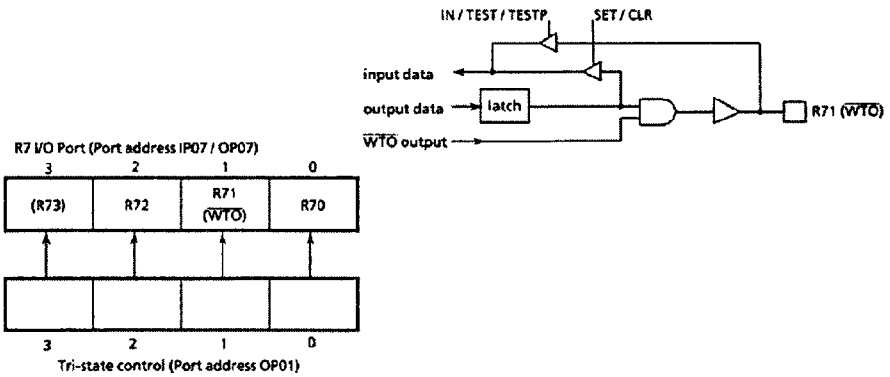



**Figure 3-3. Port R7**

(4) Port R8 (R82 to R80)

This is a 3-bit I/O port with latch.

R8 port output buffers are Tri-state, and each bit of them can be controlled independently by the program. Controlling the Tri-state is performed by the command register accessed as port address OP02. When some bit of the OP02 is 0, the corresponding bit of the output buffers becomes High-impedance state

The output buffers should be set to High impedance state, when the port is used as input port, and the output buffer be set to High-impedance state during reset. R83 pin does not exist actually but R83 has the latch. There is no timer/counter1 external input pin (T1).

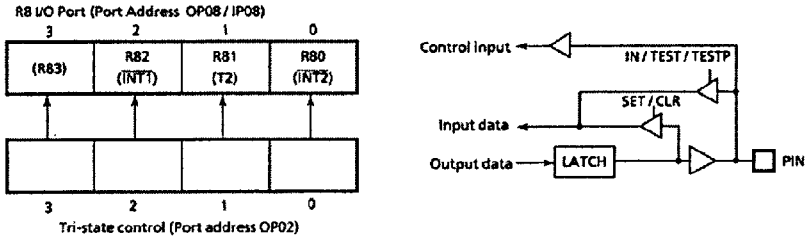



**Figure 3-4. Port R8**

## Table 3-1 Port Address Assignments and Available I/O Instructions

| Port address (**) | Port | | I/O instruction | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Input (IP**) | Output (OP**) | IN %p, A<br>IN %p, @HL | OUT A, %p<br>OUT @HL, %p | OUT #k, %p | OUTB@HL | SET %p, b<br>CLR %p, b | TEST %p, b<br>TESTP %p, b | SET @L<br>CLR @L<br>TEST @L |
| $00_H$ | K0 input port | Tri-state(R4 port)control | ○ | ○ | ○ | - | - | ○ | - |
| 01 | —— | Tri-state(R7 port)control | - | ○ | ○ | - | - | ○ | - |
| 02 | —— | Tri-state(R8 port)control | - | ○ | ○ | - | - | ○ | - |
| 03 | —— | —— | - | - | - | - | - | - | - |
| 04 | R4 input port | R4 output port | ○ | ○ | ○ | - | ○ | ○ | ○ |
| 05 | —— | —— | - | - | - | - | - | - | - |
| 06 | R6 input port | R6 output port | ○ | ○ | ○ | - | ○ | ○ | ○ |
| 07 | R7 input port | R7 output port | ○ | ○ | ○ | - | ○ | ○ | ○ |
| 08 | R8 input port | R8 output port | ○ | ○ | ○ | - | ○ | ○ | - |
| 09 | —— | —— | - | - | - | - | - | - | - |
| 0A | RA input port | RA output port | ○ | ○ | ○ | - | ○ | ○ | - |
| 0B | —— | —— | - | - | - | - | - | - | - |
| 0C | —— | OSD command selector | - | ○ | ○ | - | - | - | - |
| 0D | Remote control count value register | Remote control offset valve register | ○ | ○ | ○ | - | - | - | - |
| 0E | status input (Note 2) | Remote control single preprocess circuit control | ○ | ○ | ○ | - | - | ○ | - |
| 0F | —— | —— | - | - | - | - | - | - | - |
| $10_H$ | undefined | Hold operation mode | - | ○ | - | - | - | - | - |
| 11 | undefined | —— | - | - | - | - | - | - | - |
| 12 | undefined | A/D converter input control1 | - | ○ | - | - | - | - | - |
| 13 | undefined | A/D converter input control2 | - | ○ | - | - | - | - | - |
| 14 | undefined | —— | - | - | - | - | - | - | - |
| 15 | undefined | Watchdog timer control | - | ○ | - | - | - | - | - |
| 16 | undefined | —— | - | - | - | - | - | - | - |
| 17 | undefined | PWM buffer selector | - | ○ | - | - | - | - | - |
| 18 | undefined | PWM data transfer buffer | - | ○ | - | - | - | - | - |
| 19 | undefined | Interval timer interrupt control | - | ○ | - | - | - | - | - |
| 1A | undefined | OSD control | - | ○ | - | - | - | - | - |
| 1B | undefined | —— | - | - | - | - | - | - | - |
| 1C | undefined | Timer/counter 1 control | - | ○ | - | - | - | - | - |
| 1D | undefined | Timer/counter 2 control | - | ○ | - | - | - | - | - |
| 1E | undefined | —— | - | - | - | - | - | - | - |
| 1F | undefined | —— | - | - | - | - | - | - | - |

Note1: "----" means the reserved state. Unavailable for the user programs.

Note 2: the status input of $\overline{\text{HOLD}}$ ($\overline{\text{KE0}}$) pin.

### 3.2 Timer/Counter (TC1, TC2)

The 47C430 does not have timer/counter1 external input. Therefore, timer/counter1 can be used as internal timer mode only. The other functions are equivalent to the timer/counters of the 47C660/860.

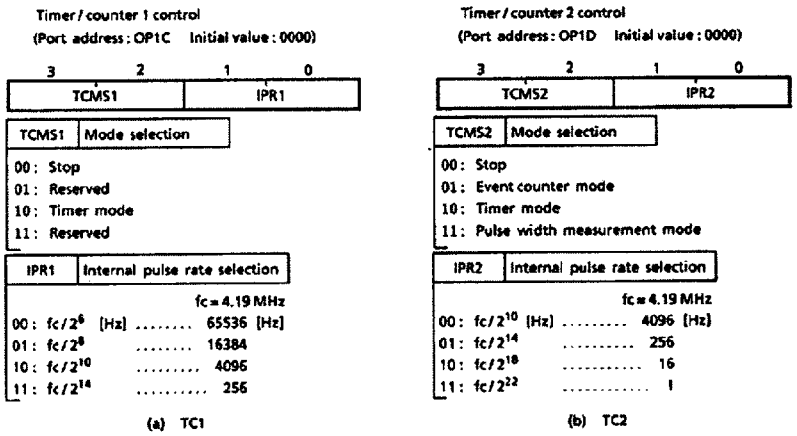



**Figure 3-5. Timer/Counter Control Command Registers**

### 3.3 On-Screen Display (OSD) Circuit

An on-screen display (OSD) circuit used to display characters and symbols in built into the TV screen.

A maximum of 32 characters, as 16 columns x 2 lines, out of 48 character patterns can be displayed at a time.

#### 3.3.1 OSD Circuit Function

| | |
|---|---|
| ① Number of characters | 48 kinds |
| ② Number of characters displayed | 32 characters (16 columns x 2 lines) |
| ③ Composition of a character | 8 x 8 dots (with smoothing function) |
| ④ Size of character | 2 kinds (selectable line by line) |
| ⑤ Color of character | 3 kinds (selectable character by character) |
| ⑥ Display position variable | horizontal 64 steps, vertical 64 steps |

### 3.3.2 OSD Circuit Configuration

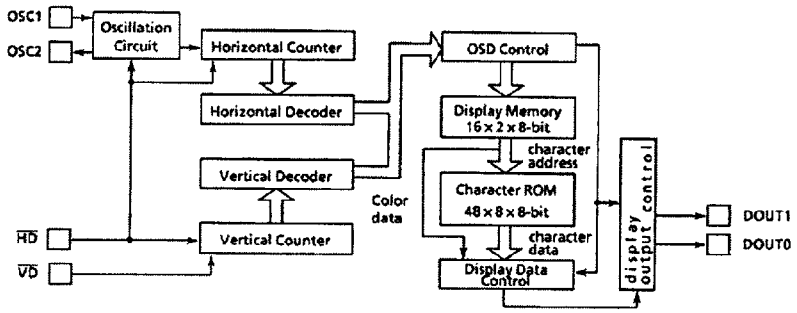



**Figure 3-6. OSD Circuit**

### 3.3.3 OSD Circuit Control

The OSD circuit is controlled by the command selector (OP0C) and control register (OP1A). Table 3-2 shows the relationship between OP0C and OP1A. OP1A is multiplexed with the six output control registers which control the display start position, color of character and character size of character, and the two transfer control registers which transfer data to the display memory.

The output control registers consist of 8 bits and all bits can be written by accessing Op1A two times. However, the second access is not required unless the second data are changed. The addressed "0 to 5" are assigned to the six output control registers. OP1A can be accessed by writing the address of the control register where data are to be changed to OP0C. The transfer control registers can be accessed by writing "6" or "7" to OP0C. The transfer control registers have a 12-bit configuration and can access OP1A three times succession. The first access sets which column is displayed within one line 16 columns.

The second and third accesses written 6 bit of character data.

The display memory has a 16-columns x 8-bit x 2 lines configuration with a one-to-one correspondence to the number of columns displayed on the screen. The display data consist of 6 character data bits and 2 color data bits for a total of 8 bits. When "6" is written to OP0C, line 1 is stored to the display memory, when "7" is written to OP0C, line 2 is stored. That is after accessing OP0C, the character data specified the second and third times are written to the display memory area specified in the first OP1A access together with the color data loaded to control register DCR50. Thus color can be specified for each character. After setting of all control registers is completed, the character data read from the character ROM(00 to $2F_H$) are output to the DOUT0 and DOUT1 pins together with the color data by setting OP0C to "F".

## Table 3-2 OSD Control Commands and Control Registers

| OSD command selector (OP0C) | OSD control register to be accessed through OP1A |
|---|---|
| 0 | Control for the horizontal start position of the first display line<br>3 2 1 0<br>DCR00 – – HS15 HS14 (1st access)<br>DCR01 HS13 HS12 HS11 HS10 (2st access) |
| 1 | Control for the vertical start position of the first display line<br>3 2 1 0<br>DCR10 – – VS15 VS14 (1st access)<br>DCR11 VS13 VS12 VS11 VS10 (2st access) |
| 2 | Control for the horizontal start position of the second display line.<br>3 2 1 0<br>DCR20 – – HS25 HS24 (1st access)<br>DCR21 HS23 HS22 HS21 HS20 (2st access) |
| 3 | Control for the vertical start position of the second display line.<br>3 2 1 0<br>DCR30 – – VS25 VS24 (1st access)<br>DCR31 VS23 VS22 VS21 VS20 (2st access) |
| 4 | Control for the character sizes,smoothing switch and OSD output polarities<br>3 2 1 0<br>DCR40 CS21 CS20 CS11 CS10 (1st access)<br>DCR41 ESMZ – – RGBIV (2st access) |
| 5 | Control for the color register and OSD output buffers'tri-state'<br>3 2 1 0<br>DCR50 – DOUT0DT DOUT1DT – (1st access)<br>DCR51 – – EBF1 EBF0 (2st access) |
| 6 | display memory write mode for the first display line(address 00 to 0F)<br>3 2 1 0<br>DMA3 DMA2 DMA1 DMA0 (1st access)<br>– – CRA5 CRA4 (2st access)<br>CRA3 CRA2 CRA1 CRA0 (3st access) |
| 7 | display memory write mode for the second display line(address 10 to 1F)<br>3 2 1 0<br>DMA3 DMA2 DMA1 DMA0 (1st access)<br>– – CRA5 CRA4 (2st access)<br>CRA3 CRA2 CRA1 CRA0 (3st access) |
| E | display OFF |
| F | display ON |

(1) Composition of character and smoothing function

Each character is composited by 8 x 8 dots. Each dot corresponds to a bit in the character ROM. Figure 3-7. (a) shows an example Composition of a character.

Smoothing function is the function to make characters look smooth. In the time the smoothing function is enabled, additional dots are displayed in the middle of the place where two dots contact each other only at a corner. Controlling of the smoothing function is performed by ESMZ in the OSD control register DCR41. Figure 3-7.(b) shows an example of the smoothing function.

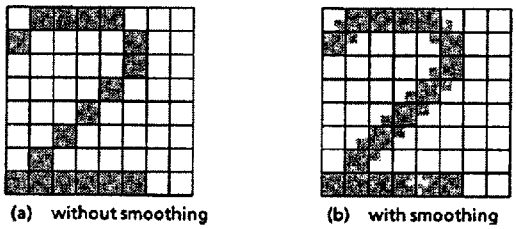



**Figure 3-7. Composition of Character and Smoothing Function**

(2) Character size and color to display

Size of the characters displayed on screen is selectable line by line from 2 sizes. The size of the first and second display line is designated by CS11 to CS10 and CS21 to CS20 in the OSD control register DCR40, respectively.

Table 3-3 shows the setting values and character sizes of DCR40.

Table 3-4 shows the display character sizes.

One out of seven colors can be selected for each character to be displayed and are determined by DOUT0DT and DOUT1DT of DCR50. The color data are written to the display memory automatically at the same time as character data are written.

**Table 3-3 Designation of Character Size**

| Character size (DCR40) | second display line | | first display line | |
|---|---|---|---|---|
| | CS21 | CS20 | CS11 | CS10 |
| small character | 1 | 0 | 1 | 0 |
| large character | 0 | 1 | 0 | 1 |
| display OFF | 0 | 0 | 0 | 0 |

**Table 3-4 Character Size**

| | small character | large character |
|---|---|---|
| dot size | $2T_{HD} \times 2T_{OSC}$ | $4T_{HD} \times 4T_{OSC}$ |
| character size | $16T_{HD} \times 16T_{OSC}$ | $32T_{HD} \times 32T_{OSC}$ |

Note. $T_{HD}$ : the period of horizontal synchrorous signal
$T_{OSC}$ : the period of OSD clock oscillation

(3) Display start position

Display start position of each display line on screen can be shifted by software.

The vertical and horizontal display starting position for the first line is determined by HS10 to 15 and VS10 to 15 of DCR00 to 11.

The vertical and horizontal display starting position for the second line is determined by HS20 to 25 and VS20 to 25 of DCR20 to 31. Each has a resolution of 64 steps.

The control register and display line on screen are shown in Table 3-6.

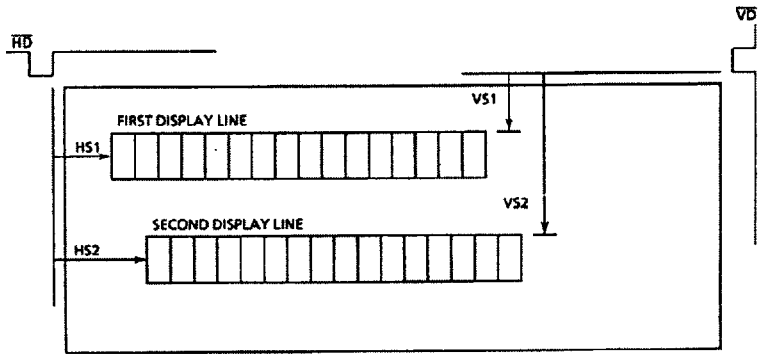



**Figure 3-8. TV Screen Image**

**Table 3-5 Display Start Position**

| Symbol | Contents |
|---|---|
| HS10 to HS15 | horizontal start position of the first display line<br>$HS1 = ((32 \times HS15 + 16 \times HS14 + 8 \times HS13 + 4 \times HS12 + 2 \times HS11 + HS10) \times 4 + X) T_{OSC}$ |
| VS10 to VS15 | vertical start position of the first display line<br>$VS1 = ((32 \times VS15 + 16 \times VS14 + 8 \times VS13 + 4 \times VS12 + 2 \times VS11 + VS10) \times 4T_{HD}$ |
| HS20 to HS25 | horizontal start position of the second display line<br>$HS2 = ((32 \times HS25 + 16 \times HS24 + 8 \times HS23 + 4 \times HS22 + 2 \times HS21 + HS20) \times 4 + X) T_{OSC}$ |
| VS20 to VS25 | vertical start position of the second display line<br>$VS2 = ((32 \times VS25 + 16 \times VS24 + 8 \times VS23 + 4 \times VS22 + 2 \times VS21 + VS20) \times 4T_{HD}$ |

Note. X: X is 17 when small character
X is 34 when large character

- The vertical display positions of lines 1 and 2 can be specified independently but, to prevent overlapping of the two lines on the display, the value for the vertical display position of line 2 must satisfy $[VS2 > VS1 + CS11 \times 16T_{HD} + CS10 \times 32T_{HD}]$.

### 3.3.4 Control of OSD outputs buffer

The OSD outputs for Y, BL and RGB use tri-state output buffers for which the respective polarities can be inverted. Polarity is controlled by DRC41 and tri-state is controlled by DRC51.

Bit 3 of DRC41 is used for controlling the smoothing function.

**Table 3-6 Control of OSD Output**

| register | bit | symbol | output name | data "0" | data "1" |
|---|---|---|---|---|---|
| DRC41 | 3 | ESMZ | — | smoozing OFF | smoozing ON |
| | 2 | — | — | — | — |
| | 1 | — | — | — | — |
| | 0 | DIV | DOUT1, DOUT0 | active High | active Low |
| DRC51 | 3 | — | — | — | — |
| | 2 | — | — | — | — |
| | 1 | EBF1 | DOUT1 | output buffer OFF | output buffer ON |
| | 0 | EBF0 | DOUT0 | output buffer OFF | output buffer ON |

### 3.3.5 RA Port Function

R signal output and G signal output ports are also used as I/O ports. When not used for color signals, use is possible as normal I/O ports. RA port and Y/BL selection is performed by OP0A.

Also, the upper 2 bits of IP0A are used to input the OSD display status.

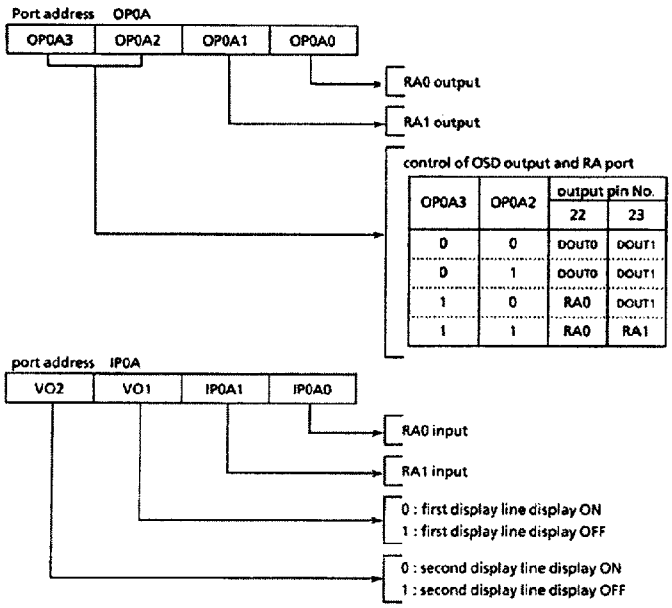



**Figure 3-9. Port RA**

### 3.3.6 Character ROM (Standard Characters)

Figure 3-10 shows the standard pattern characters and symbols available as character data. Character patterns can also be set by the user. For details, refer to the section on piggyback chip 47C034.

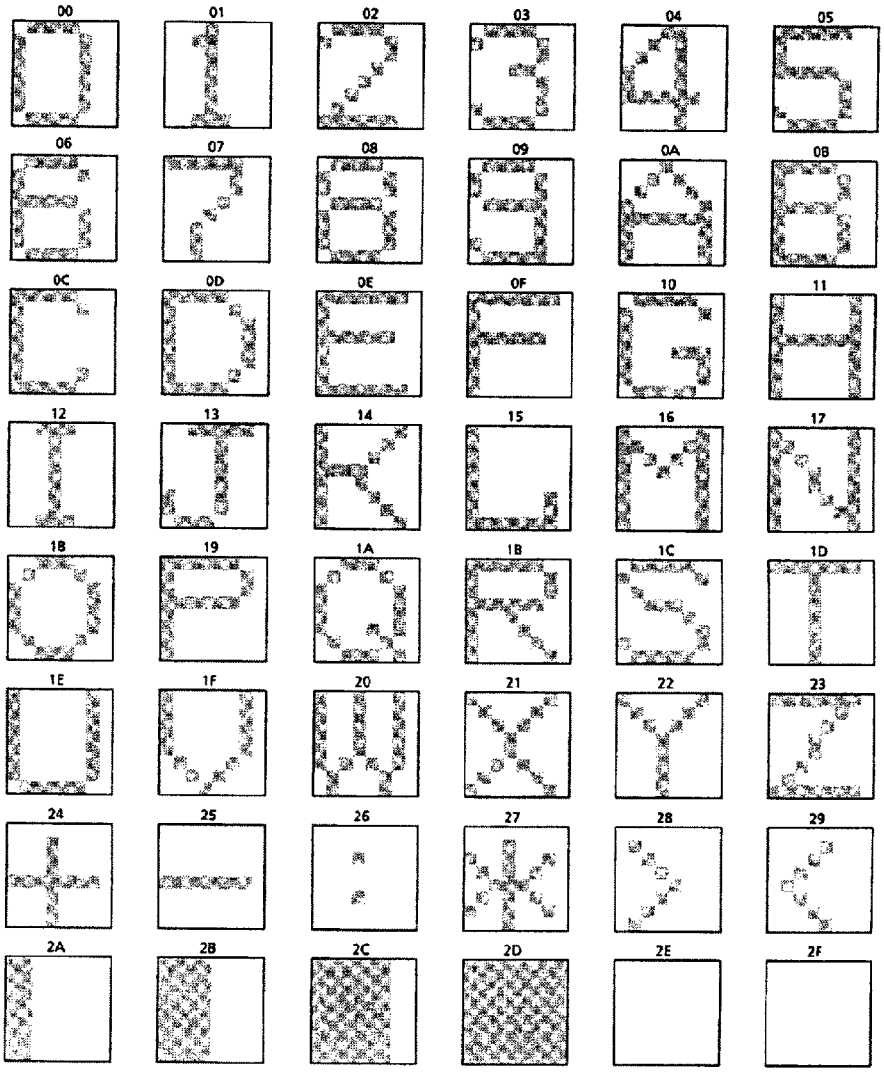



**Figure 3-10. Character ROM Address and Character Pattern**

### 3.4 4-Bit A/D Conversion (Comparator) Input

The comparator input is analog input to discriminate key input or AFC (Auto Frequency Control) signal. It's composed of 4-bit D/A converter, comparator and control circuit. Analog input level (CIN0 to CIN3) can be detected as 16-stage by setting reference voltage.

The comparator input can also be used as K0 port (digital input). To use as K0 port, set the most significant bit of the port address OP13 to "1". Which port is selected digital (K0) or comparator (CIN) input can be monitored by accessing the port address IP13. DTB selector/status is also assigned to port address OP13/IP13.

Note. When the comparator input is selected, the comparator consumes typically 700μA current at VDD = 5V. To reduce the power consumption, K0 port should be set to digital input mode. In the HOLD mode, the comparator is automatically cut off by hardware. Further, during the slow operating mode, A/D conversion input is automatically disabled by hardware to reduce the power consumption.

#### 3.4.1 Circuit Configuration of Comparator Input

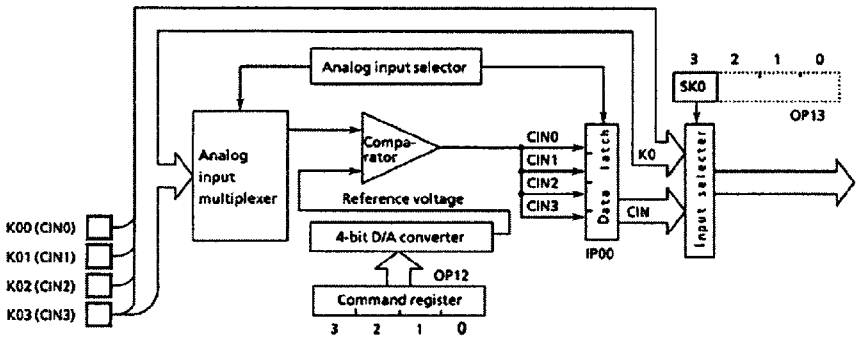



**Figure 3-11. Circuit of Comparator Input**

### 3.4.2 Control of Comparator Input

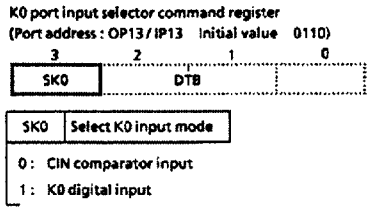



**Figure 3-12. Command Register, Status Register**

Reference voltage (Vref) is set by command register (port address OP12), and it is determined by the following form.

$$V_{REF} = V_{DD} \times (n + 1) / 16[V] \quad (n = 0 \text{ to } 15)$$

After initialization sequence, 4-channel comparator inputs continue comparison operation successively.

Since 2-instruction cycles are required to complete comparison of 1-channel, it is necessary to wait for 8-instruction cycles after setting a reference voltage to read data from the comparator. When analog input voltage is higher than reference voltage, comparator data latch is set to "1". At the initialization sequence, OP12 is set to "0". There is not latch when used to port K0.

**Table 3-7 Reference Voltage**

| OP12 | | | | Vref. [V] |
|---|---|---|---|---|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 0.31 |
| 0 | 0 | 0 | 1 | 0.62 |
| 0 | 0 | 1 | 0 | 0.94 |
| 0 | 0 | 1 | 1 | 1.25 |
| 0 | 1 | 0 | 0 | 1.56 |
| 0 | 1 | 0 | 1 | 1.87 |
| 0 | 1 | 1 | 0 | 2.19 |
| 0 | 1 | 1 | 1 | 2.50 |
| 1 | 0 | 0 | 0 | 2.81 |
| 1 | 0 | 0 | 1 | 3.12 |
| 1 | 0 | 1 | 0 | 3.44 |
| 1 | 0 | 1 | 1 | 3.75 |
| 1 | 1 | 0 | 0 | 4.06 |
| 1 | 1 | 0 | 1 | 4.37 |
| 1 | 1 | 1 | 0 | 4.69 |
| 1 | 1 | 1 | 1 | 5.00 |

### 3.5 D/A Converter (PWM) Output

The 47C430 have 2 channels built-in D/A converter (Pulse width Modulation) outputs. $\overline{PWM}$ output can easily be obtained by connecting an external low pass filter.

$\overline{PWM}$ outputs data are multiplex to the R4 port. When the R4 ($\overline{PWM}$) port is used for $\overline{PWM}$ output, the corresponding bits of R4 output latch should be set to "1". The R4 output latch is initialized to "1" during reset.

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). PWM data written to the data transfer buffer can be sent to the PWM data latch by writing "$C_H$" to the buffer selector, and $\overline{PWM}$ output $\overline{PWM}$ output. PWM data transferred to the PWM data latch remain intact until overwritten. Resetting and holding clear the buffer selector, data transfer buffer and PWM data latch to "0" ($\overline{PWM}$ output is "H" level).

#### 3.5.1 Configuration of Pulse Width Modulation Circuit

Configuration of pulse width modulation circuit shown in Figure 3-13.

#### 3.5.2 Output Waveform of PWM Circuit

(1) $\overline{PWM0}$ output

$\overline{PWM0}$ is a PWM output controlled by 14 bits data. The basic period of the $\overline{PWM0}$ is $T_M = 2^{15}/fs$.

The higher 8 bits of 14 bits data are used to control the pulse width of the pulse output with the period of $T_S = T_M/64$, which is the sub - period of the $\overline{PWM0}$. When the 8 bits data are decimal n ($0 \geq n \geq 255$), this pulse width becomes n x $t_0$, where $t_0 = 2/fc$.

The lower 6 bits of 14 bits data are used to control the generation of an additional $t_0$ wide pulse in each $T_S$ period. When the 6 bits data are decimal m ($0 \geq m \geq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a $T_M$ period. The relationship between the 6 bits data and the position of $T_S$ period where the additional pulse is generated is shown in Table 3-8.

(2) $\overline{PWM1}$ output

$\overline{PWM1}$ is a PWM output controlled by 6 bits data. The period of them is $T_M = 2^7/fs$. When the 6 bits data are decimal k ($0 < k < 63$), the pulse width becomes kx $t_0$. The waveform is also illustrated in Figure 3-13.

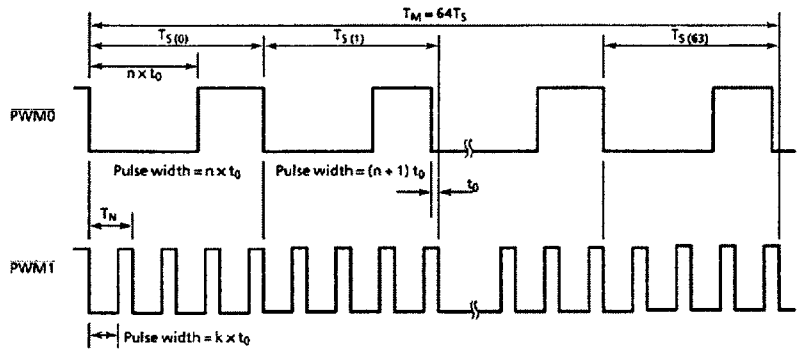



**Figure 3-13. $\overline{PWM}$ Output Waveform (It is Shown to the Additional Pulse $T_{S(1)}$ and $T_{S(63)}$ of the $\overline{PWM0}$)**

**Table 3-8 Correspondence Between 6 Bits Data and the Additional Pulse Generated $T_S$ Periods**

| Bit position of 6 bits data | Relative position of $T_S$ where the output pulse is generated (No. i of $T_{S(i)}$ is listed) |
|---|---|
| bit 0 | 32 |
| bit 1 | 16, 48 |
| bit 2 | 8, 24, 40, 56 |
| bit3 | 4, 12, 20, 28, 36, 44, 52, 60 |
| bit4 | 2, 6, 10, 14, 18, 22, 26, 30, —, 58, 62 |
| bit5 | 1, 3, 5, 7, 9, 11, 13, 15, 17, —, 59, 61, 63 |

Note. When the corresponding bit is "1", it is output.

### 3.5.3 Control of PWM Circuit (Data Transfer)

$\overline{\text{PWM}}$ output is controlled by writing output data to a data transfer buffer (OP18). For writing, the output data are divided using the buffer selector (OP17). Buffer numbers are assigned to the data transfer buffers for these divided data, after which the data are written as shown in Table 3-9.

① The number of the transfer buffer to which the data are to be written is written to the buffer selector (OP17)

② The corresponding PWM data are written to the selected buffer (OP18).

③ Operations ① and ② are repeated, continuously writing data to the transfer buffer.

④ When all of the output data have been written. "$C_H$" is written to the buffer selector.

While the output data are being written to the transfer buffer, the previously written data are being output. For $\overline{\text{PWM0}}$ output, switching to $\overline{\text{PWM}}$ output occurs at a maximum of $2^{15}$/fc [s] (at 4 MHz, 8192fs) after "$C_H$" is written to the buffer selector. For $\overline{\text{PWM1}}$ output data switching, this requires $2^9$/fc [s] (at 4MHz, 128μs).

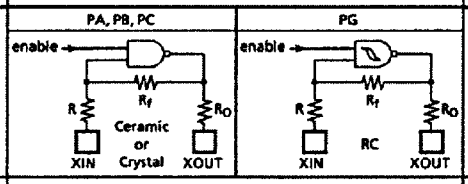
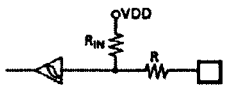
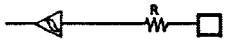
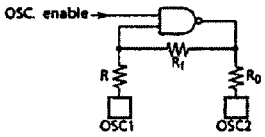
**Table 3-9 Bit and Buffer Number of Data Transfer Buffer**

| Buffer Number (OP17) | Correspondence to bit (OP18) | | Mode | PWM Output |
|---|---|---|---|---|
| 2 | Bit of PWM0 transfer buffer | 9 to 6 | Write | Preceding data |
| 3 | Bit of PWM0 transfer buffer | 13 to 10 | Write | Preceding data |
| 4 | Bit of PWM0 transfer buffer | 3 to 0 | Write | Preceding data |
| 5 | Bit of PWM0 transfer buffer | 5 to 4 | Write | Preceding data |
| 6 | Bit of PWM1 transfer buffer | 3 to 0 | Write | Preceding data |
| 7 | Bit of PWM1 transfer buffer | 5 to 4 | Write | Preceding data |
| C | None | | Transfer | Present data |

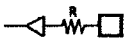
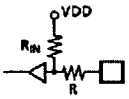
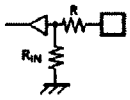
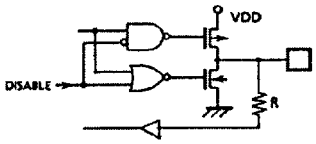
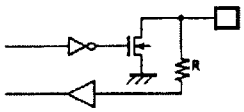
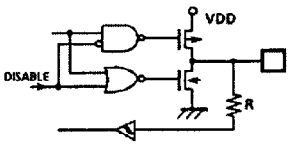
## Input/Output Circuitry

The input/output circuitries of the 47C434A/634A control pins are shown below.

(1) Control pins

| CONTROL PIN | I/O | CIRCUITRY | REMARKS |
|---|---|---|---|
| XIN<br>XOUT | Input<br>Output | PA, PB, PC / PG<br>  | Resonator connecting pins<br>R = 1 kΩ (typ.)<br>$R_f$ = 1.5 MΩ (typ.)<br>$R_O$ = 2 kΩ (typ.) |
| $\overline{RESET}$ | Input |  | Hysteresis input<br>Contained pull-up resistor<br>$R_{IN}$ = 220 kΩ (typ.)<br>R = 1 kΩ (typ.) |
| $\overline{HOLD}$ ($\overline{KE0}$) | Input<br>(Input) |  | Hysteresis input<br>(Sense input)<br>R = 1 kΩ (typ.) |
| OSC1<br>OSC2 | Input<br>Output |  | Oscilation terminals for OSD<br>R = 1 kΩ (typ.)<br>$R_f$ = 1.5 MΩ (typ.)<br>$R_O$ = 2 kΩ (typ.) |
| $\overline{HD}$<br>$\overline{VD}$ | Input |  | Synchronous signal input<br>Hysteresis input<br>R = 1 kΩ (typ.) |

(2) I/O ports

| PORT | I/O | INPUT/OUTPUT CIRCUITRY and CODE | | | REMARKS |
|---|---|---|---|---|---|
| | | PA, PG | PB | PC | |
| K0 | Input |  |  |  | Pull-up or pull-down resistor<br>$R_{IN}$ = 70 kΩ (typ.)<br>R = 1 kΩ (typ.) |
| R4<br>R7<br>RA | I/O |  | | | Tri-state<br>Initial "Hi-Z"<br>R = 1 kΩ (typ.) |
| R6 | I/O |  | | | Sink open drain<br>Initial "Hi-Z"<br>R = 1 kΩ (typ.) |
| R8 | I/O |  | | | Tri-state<br>Initial "Hi-Z"<br>Hysteresis input<br>R = 1 kΩ (typ.) |

## Electrical Characteristics

### Absolute Maximum Ratings ($V_{SS}$ = 0V)

| Parameter | Symbol | Pins | | Ratings | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | | -0.3 to 6.5 | V |
| Input Voltage | $V_{IN}$ | | | -0.3 to $V_{DD}$ + 0.3 | V |
| Output Voltage | $V_{OUT}$ | | | -0.3 to $V_{DD}$ + 0.3 | V |
| Output Current (Per 1 pin) | $I_{OUT1}$ | R6 port | | 30 | mA |
| | $I_{OUT2}$ | R7, R8, R9 port | | 3.2 | |
| Output Current (Total) | $\Sigma I_{OUT1}$ | R6 port | | 60 | mA |
| Power Dissipation | PD | | DIP | 300 | mW |
| | | | SOP | 180 | |
| Soldering temperature (time) | $T_{sld}$ | | | 260 (10 s) | °C |
| Storage Temperature | $T_{stg}$ | | | -55 to 125 | °C |
| Operating Temperature | $T_{opr}$ | | | -30 to 70 | °C |

### Recommended Operating Conditions ($V_{SS}$ = 0V, $T_{opr}$ = -30 to 70°C)

| Parameter | Symbol | Pins | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | In the Normal mode | 2.7 | 5.5 | V |
| | | | In the HOLD mode | 2.0 | | |
| High Input Voltage | $V_{IH1}$ | Except Hysteresis Input | $V_{DD} \geq 4.5V$ | $V_{DD}$ x 0.7 | $V_{DD}$ | V |
| | $V_{IH2}$ | Hysteresis Input | | $V_{DD}$ x 0.75 | | |
| | $V_{IH3}$ | | $V_{DD} < 4.5V$ | $V_{DD}$ x 0.9 | | |
| Low Input Voltage | $V_{IL1}$ | Except Hysteresis Input | $V_{DD} \geq 4.5V$ | 0 | $V_{DD}$ x 0.3 | V |
| | $V_{IL2}$ | Hysteresis Input | | | $V_{DD}$ x 0.25 | |
| | $V_{IL3}$ | | $V_{DD} < 4.5V$ | | $V_{DD}$ x 0.1 | |
| Clock Frequency | fc | | $V_{DD}$ = 2.7 to 5.5 V | 1 | 4.2 | MHz |
| | | | $V_{DD}$ = 4.5 to 5.5 V | 1 | 6.0 | |
| | $f_{OSD}$ | | | - | 6.0 | |

Note. Input voltage $V_{IH3}$, $V_{IL3}$: in the HOLD operating mode.

## DC Characteristics ($V_{SS}$ = 0V, $T_{opr}$ = -30 to 70°C)

| Parameter | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Hysteresis Voltage | $V_{HS}$ | Hysteresis Input | | - | 0.7 | - | V |
| Input Current | $I_{IN1}$ | K0 port, TEST, $\overline{RESET}$, $\overline{HOLD}$ | $V_{DD}$ = 5.5V, $V_{IN}$ = 5.5V/0V | - | - | ±2 | μA |
| | $I_{IN2}$ | R port (open drain) | | | | | |
| Input Resistance | $R_{IN1}$ | K0 port with pull-up/pull-down | | 30 | 70 | 150 | kΩ |
| | $R_{IN2}$ | $\overline{RESET}$ | | 100 | 220 | 450 | |
| Output Leakage Current | $I_{LO1}$ | Tri-state R6, R8, R9 port (open drain) | $V_{DD}$ = 5.5V, $V_{OUT}$ = 5.5V | - | - | ±2 | μA |
| Output High Voltage | $V_{OH}$ | R port (tri-state) | $V_{DD}$ = 4.5V, $I_{OH}$ = -0.7 mA | 4.1 | - | - | V |
| Output Low Voltage | $V_{OL}$ | R port (tri-state) | $V_{DD}$ = 4.5V, $I_{OL}$ = 0.7 mA | - | - | 0.4 | V |
| Output Level Low Current | $I_{OL}$ | R6 port | $V_{DD}$ = 4.5V, $V_{OL}$ = 1.0V | - | 20 | - | mA |
| Supply Current (in the Normal mode) | $I_{DD}$ | | $V_{DD}$ = 5.5V, fc = 4MHz | - | 2 | 4 | mA |
| Supply Current (in the HOLD mode) | $I_{DDH}$ | | $V_{DD}$ = 5.5V | - | 0.5 | 10 | μA |

Note 1. Typ. values show those when $T_{opr}$ = 25°C, $V_{DD}$ = 5V.

Note 2. Input Current $I_{IN1}$: The current through resistor is not included, when the pull-up/pull-down resistor is contained.

Note 3. Supply Current : $V_{IN}$ = 5.3V/0.2V
The port K0 is opened when the pull-up/pull-down resistor is contained.
The voltage applied to the R port is within the valid range $V_{IL}$ or $V_{IH}$.

## A/D Conversion Characteristics

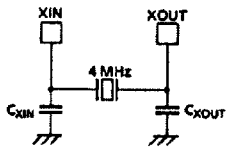
| Parameter | Symbol | Pins | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Analog Input Voltage | $V_{AIN}$ | CIN | | $V_{SS}$ | - | $V_{DD}$ | V |
| A/D conversion error | | | | - | - | ±1/4 | LSB |

## AC Characteristics ($V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V, $T_{opr}$ = -30 to 70°C)

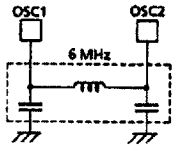
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Instruction Cycle Time | $t_{cy}$ | | 1.9 | - | 20 | μs |
| High level clock pulse width | $t_{WCJ}$ | For external clock operation | 80 | - | - | ns |
| Low level clock pulse width | $t_{WCL}$ | | | | | |

## Recommended Oscillating Conditions ($V_{SS}$ = 0V, $V_{DD}$ = 4.5 to 6.0V, $T_{opr}$ = -30 to 70°C)

(1) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF




(2) 6MHz
LC Resonator
TBEKSES-30361FBY (TOKO)




Note: An electrical shield by metal plate on the surface of the IC package should be recommendable in order to prevent the device from the high electric field stress applied from CRT (Cathode Ray Tube) for continuous reliable operation.

## Typical Characteristics