

# MSM548128BL

**131,072-Word × 8-Bit High-Speed PSRAM**

## DESCRIPTION

The MSM548128BL is a 1-Mbit, high-speed and low power CMOS Pseudo Static RAM organized as 131,072-word × 8-bit.

The MSM548128BL is fabricated using silicon gate N well CMOS process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density, minimum chip size, and high speed.

MSM548128BL has Self-refresh mode in addition to Address-refresh mode and Auto-refresh mode. In Self-refresh mode the internal refresh timer and address counter refresh the dynamic memory cells automatically. This series allows low power consumption when using standby mode with Self-refresh.

The MSM548128BL also features a static RAM-like write function that writes the data into the memory cell at the rising edge of  $\overline{WE}$ .

The MSM548128BL is pin compatible with CMOS static RAM and 256K pseudo static RAM.

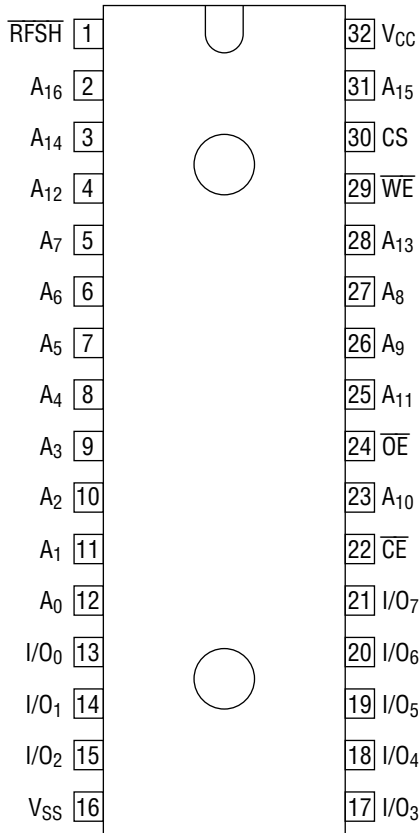
## FEATURES

- Large capacity : 1-Mbit (131,072-word × 8 bits)
  - Fast access time : 70 ns max.
  - Low power : 200  $\mu$ A max. (standby with Self-refresh)
  - Refresh free : Self refresh
  - Pin compatible : SRAM, 256K PSRAM
  - Logic compatible : SRAM  $\overline{WE}$  pin, no address multiplex
  - Single power supply : 5 V  $\pm$ 10%
  - Refresh : 512 cycle/8 ms auto-address refresh
  - Package compatible : SRAM standard package
  - Package options:
    - 32-pin 600 mil plastic DIP (DIP32-P-600-2.54) (Product : MSM548128BL-xxRS)
    - 32-pin 525 mil plastic SOP (SOP32-P-525-1.27-K) (Product : MSM548128BL-xxGS-K)
- xx indicates speed rank.

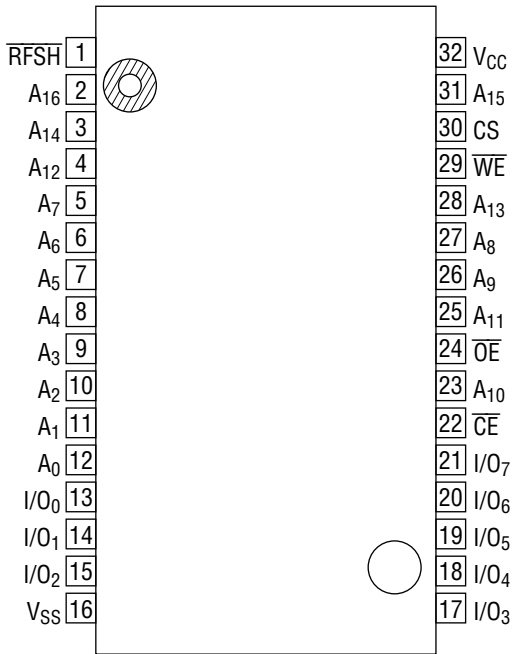
## PRODUCT FAMILY

Family	Access Time (Max.)	Package
MSM548128BL-70RS	70 ns	600 mil 32-pin Plastic DIP
MSM548128BL-80RS	80 ns	
MSM548128BL-70GS-K	70 ns	525 mil 32-pin Plastic SOP
MSM548128BL-80GS-K	80 ns	

**PIN CONFIGURATION (TOP VIEW)**



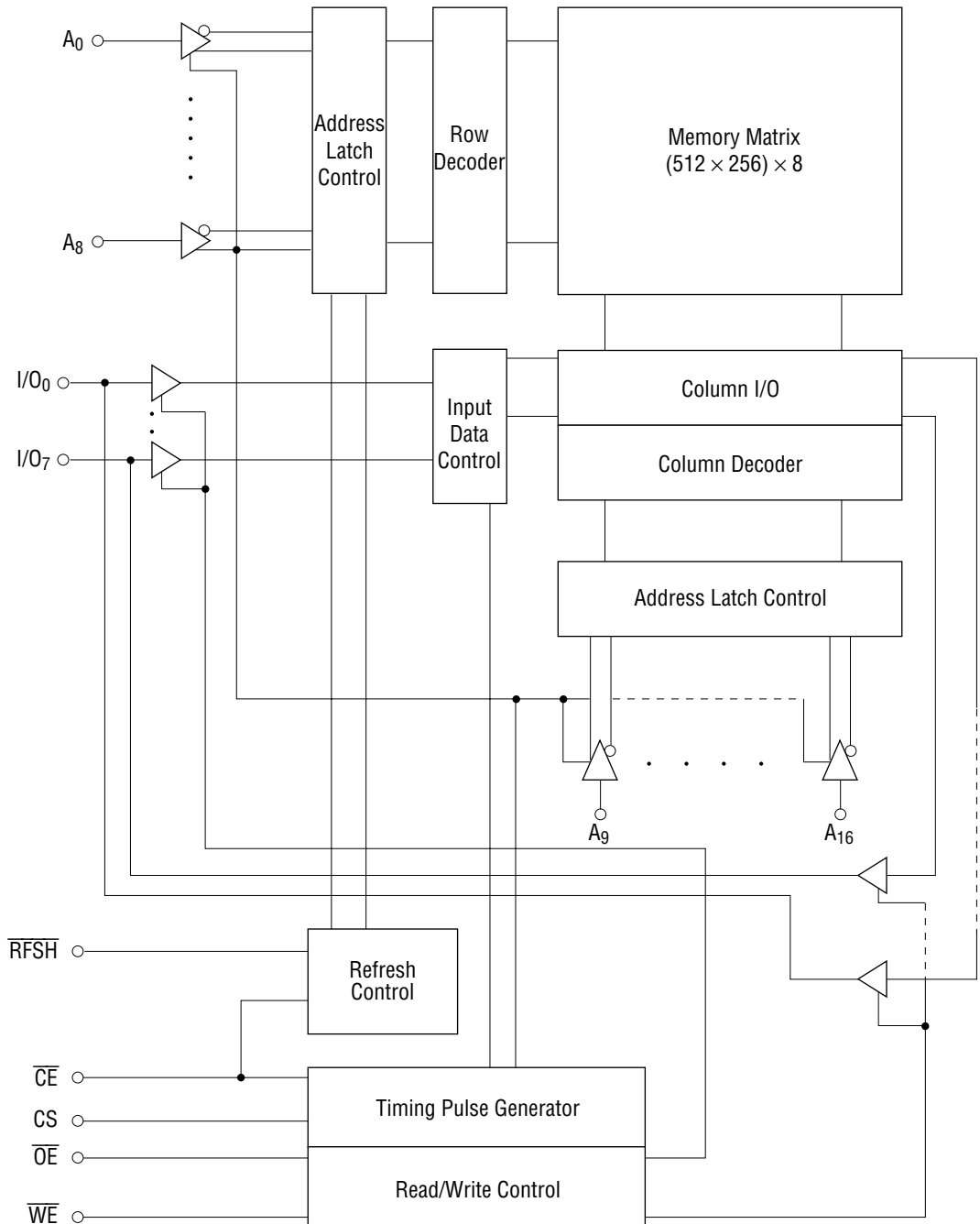
32-Pin Plastic DIP



32-Pin Plastic SOP

Pin Name	Function
A <sub>0</sub> - A <sub>16</sub>	Address Input
I/O <sub>0</sub> - I/O <sub>7</sub>	Data Input/Output
$\overline{\text{RFSH}}$	Refresh Input
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{WE}}$	Write Enable Input
CS	Chip Select Input
V <sub>CC</sub>	Power Voltage (5 V)
V <sub>SS</sub>	Ground (0 V)

**BLOCK DIAGRAM**



**FUNCTION TABLE**

$\overline{CE}$	$\overline{CS}$ ( $\overline{CE}$ Low)	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low-Z	Read
L	H	X	X	L	High-Z	Write
L	H	X	H	H	High-Z	—
L	L	X	X	X	High-Z	CS Standby
H	X	L	X	X	High-Z	Refresh
H	X	H	X	X	High-Z	Standby

L : Low Level Input  
 H : High Level Input  
 X : Don't Care

**ELECTRICAL CHARACTERISTICS**

**Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin from $V_{SS}$ *1	$V_T$	-1.0 to 7.0	V
Power Dissipation	$P_D$	1.0	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 125	°C
Storage Temperature (biased)	$T_{bias}$	-10 to 85	°C
Short Circuit Output Current	$I_{OS}$	50	mA

\*1 To  $V_{SS}$

Note: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input Voltage	$V_{IH}$	2.4	—	6.0	V
	$V_{IL}$	-0.5	—	0.8	V

**DC Characteristics**

( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operating Current	$I_{CC1}$	—	60	85	mA	$I_{I/O} = \text{Open}$ , $t_{cyc} = \text{min.}$
Standby Current	$I_{SB1}$	—	1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{RFSH} = V_{IH}$ , $V_{IN} \geq 0\text{ V}$
	$I_{SB2}$	—	100	200	$\mu\text{A}$	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $\overline{RFSH} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq 0\text{ V}$
Self Refresh Current	$I_{CC2}$	—	1	2	mA	$\overline{CE} = V_{IH}$ , $\overline{RFSH} = V_{IL}$ , $V_{IN} \geq 0\text{ V}$
	$I_{CC3}$	—	100	200	$\mu\text{A}$	$\overline{CE} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq 0\text{ V}$ , $\overline{RFSH} \leq 0.2\text{ V}$
Input Leakage Current	$I_{LI}$	-10	—	10	$\mu\text{A}$	$V_{CC} = 5.5\text{ V}$ , $V_{IN} = V_{SS}$ to $V_{CC}$
Output Leakage Current	$I_{LO}$	-10	—	10	$\mu\text{A}$	$\overline{OE} = V_{IH}$ , $V_{I/O} = V_{SS}$ to $V_{CC}$
Output Low Level	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1\text{ mA}$
Output High Level	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1\text{ mA}$

**Capacitance**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Capacitance	$C_{IN}$	$V_{IN} = 0\text{ V}$	—	—	8	pF
I/O Pin Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$	—	—	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**AC Characteristics**

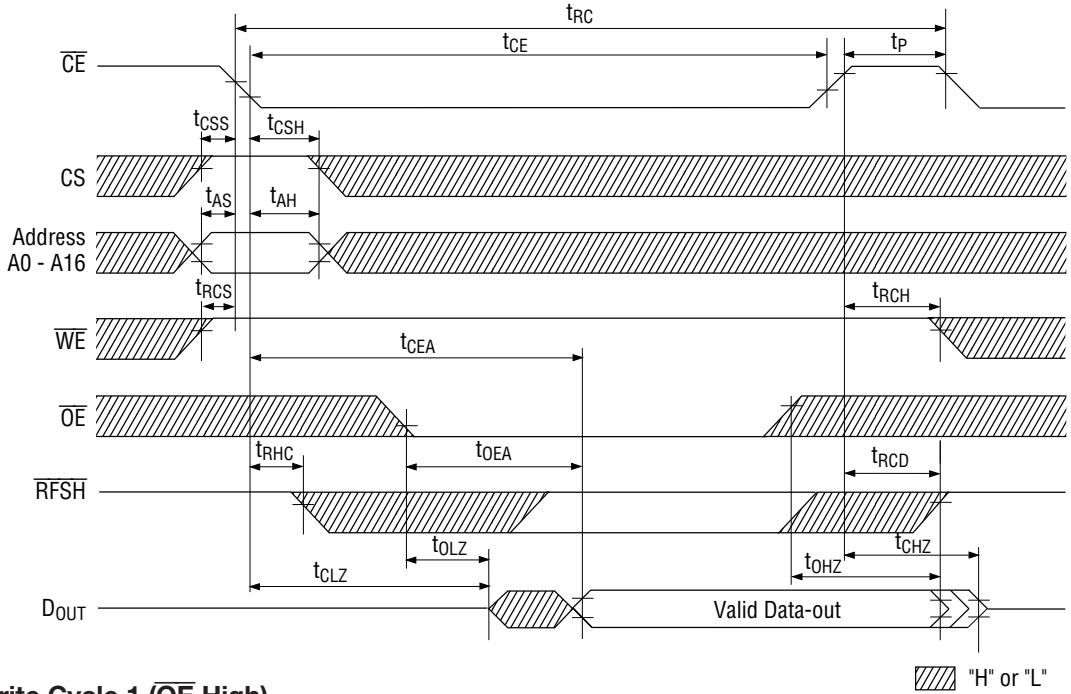
Measurement condition: Input pulse level .....  $V_{IH} = 2.4\text{ V}$ ,  $V_{IL} = 0.4\text{ V}$   
 Output reference level.....  $V_{OH} = 2.0\text{ V}$ ,  $V_{OL} = 0.8\text{ V}$   
 Rising and falling time..... 5 ns  
 Output load ..... 1 TTL + 100 pF  
 Input timing reference level..... High = 2.2 V, Low = 0.8 V  
 ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $T_a = 0^\circ\text{C to } 70^\circ\text{C}$ )

Parameter	Symbol	MSM548128BL-70		MSM548128BL-80		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read Write Cycle Time	$t_{RC}$	120	—	130	—	ns	
Random Read Modify Write Cycle Time	$t_{RWC}$	170	—	190	—	ns	
$\overline{CE}$ Access Time	$t_{CEA}$	—	70	—	80	ns	
$\overline{OE}$ Access Time	$t_{OEA}$	—	30	—	30	ns	
Chip Disable to Output in High-Z	$t_{CHZ}$	—	30	—	30	ns	6
$\overline{CE}$ to Output in Low-Z	$t_{CLZ}$	25	—	25	—	ns	
$\overline{OE}$ Disable to Output in High-Z	$t_{OHZ}$	—	20	—	25	ns	6
$\overline{OE}$ Output in Low-Z	$t_{OLZ}$	0	—	0	—	ns	
$\overline{CE}$ Pulse Width	$t_{CE}$	70n	10 $\mu$	80n	10 $\mu$	s	
$\overline{CE}$ Precharge Time	$t_P$	40	—	40	—	ns	
Address Set-up Time	$t_{AS}$	0	—	0	—	ns	
Address Hold Time	$t_{AH}$	25	—	30	—	ns	
Read Command Set-up Time	$t_{RCS}$	0	—	0	—	ns	
Read Command Hold Time	$t_{RCH}$	0	—	0	—	ns	
$\overline{RFSH}$ Command Hold Time	$t_{RHC}$	15	—	15	—	ns	
$\overline{RFSH}$ Delay Time (Standby Mode)	$t_{RCD}$	—	5	—	5	ns	
CS Set-up Time	$t_{CSS}$	0	—	0	—	ns	
CS Hold Time	$t_{CSH}$	25	—	30	—	ns	
Write Command Pulse Width	$t_{WP}$	25	—	30	—	ns	
Chip Enable Time	$t_{CW}$	70	—	80	—	ns	
Input Data Set-up Time	$t_{DW}$	25	—	25	—	ns	
Input Data Hold Time	$t_{DH}$	0	—	0	—	ns	
Output Active from End of Write	$t_{OW}$	5	—	5	—	ns	
Write Enable to Output in High-Z	$t_{WHZ}$	—	20	—	25	ns	6
Transition Time	$t_T$	3	50	3	50	ns	11
$\overline{RFSH}$ Delay Time from $\overline{CE}$	$t_{RFD}$	40	—	40	—	ns	
$\overline{RFSH}$ Precharge Time	$t_{FP}$	30	—	30	—	ns	
$\overline{RFSH}$ Pulse Width (Auto-refresh)	$t_{FAP}$	30n	8 $\mu$	30n	8 $\mu$	s	
Auto-refresh Cycle Time	$t_{FC}$	120	—	130	—	ns	
$\overline{RFSH}$ Pulse Width (Self-refresh)	$t_{FAS}$	8	—	8	—	$\mu$ s	
$\overline{CE}$ Delay Time from $\overline{RFSH}$ in Self-refresh Mode	$t_{RFS}$	150	—	160	—	ns	
$\overline{CE}$ Delay Time from $\overline{RFSH}$ in Auto-refresh Mode	$t_{RFA}$	0	—	0	—	ns	
Refresh Period (512 cycle/8 ms)	$t_{REF}$	—	8	—	8	ms	

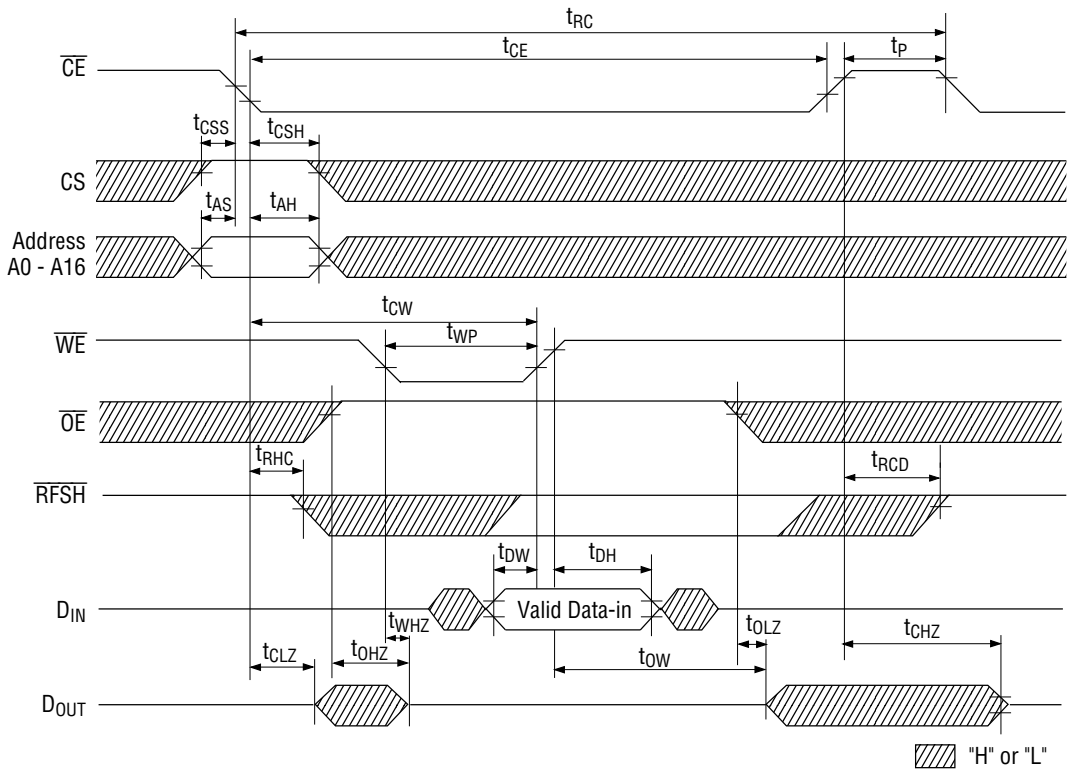
- Notes:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
  2. All voltages are referenced to ground.
  3.  $I_{CC1}$  depends on output loading. Specified values are obtained with the output open.
  4. An initial pause of 100  $\mu$ s is required after power-up followed by more than 8 initial cycles before proper device operation is achieved.
  5. AC measurements assume  $t_T = 5$  ns.
  6.  $t_{CHZ}$ ,  $t_{WHZ}$  and  $t_{OHZ}$  define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
  7. In write cycles, the input data is latched at the earlier rising point of either  $\overline{CE}$  or  $\overline{WE}$ . Write operation is achieved when both  $\overline{CE}$  and  $\overline{WE}$  are low.
  8. The I/O state remains at high impedance after  $\overline{CE}$  goes low if the transition occurs at the same time as or after the falling edge of  $\overline{WE}$ .
  9. Use  $\overline{WE}$  or  $\overline{OE}$  or both signals to disable the output before input data is applied during a write cycle when the input is not the same.
  10. Data input must be set to floating state before I/O becomes low impedance by  $\overline{WE}$  or  $\overline{OE}$  or both.
  11.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are input timing reference levels for measurement. The transition time is measured between  $V_{IL}$  and  $V_{IH}$ .
  12. 512-cycle refresh must be applied within 15  $\mu$ s after the end of self refreshing to satisfy 512 cycles/8 ms.

### TIMING WAVEFORM

#### Read Cycle

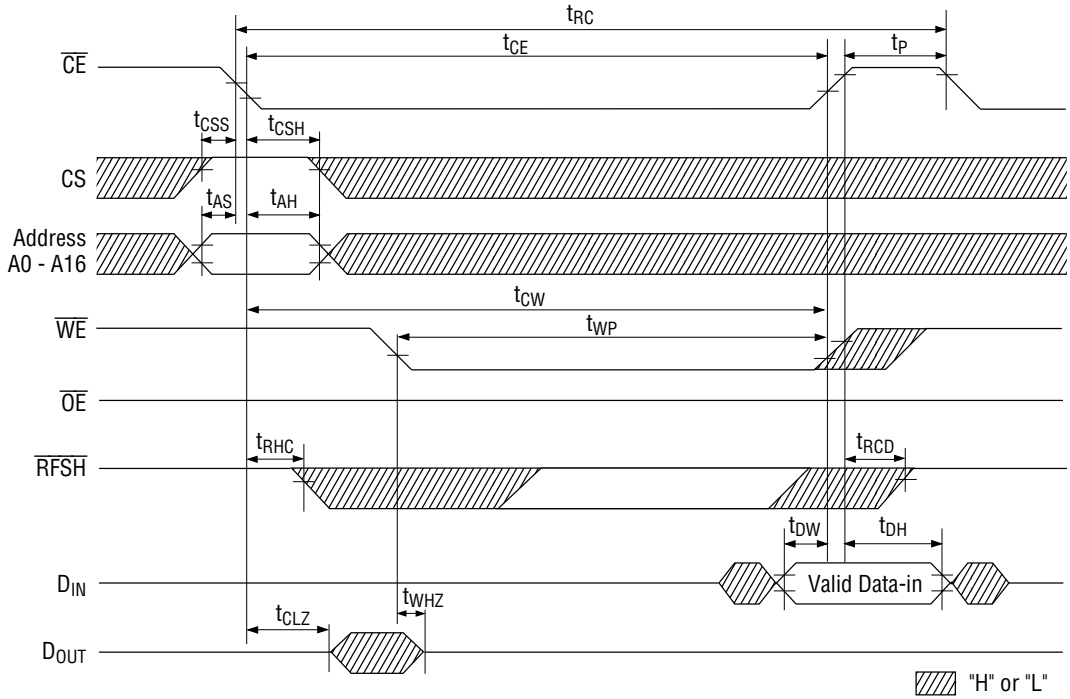


#### Write Cycle 1 ( $\overline{OE}$ High)

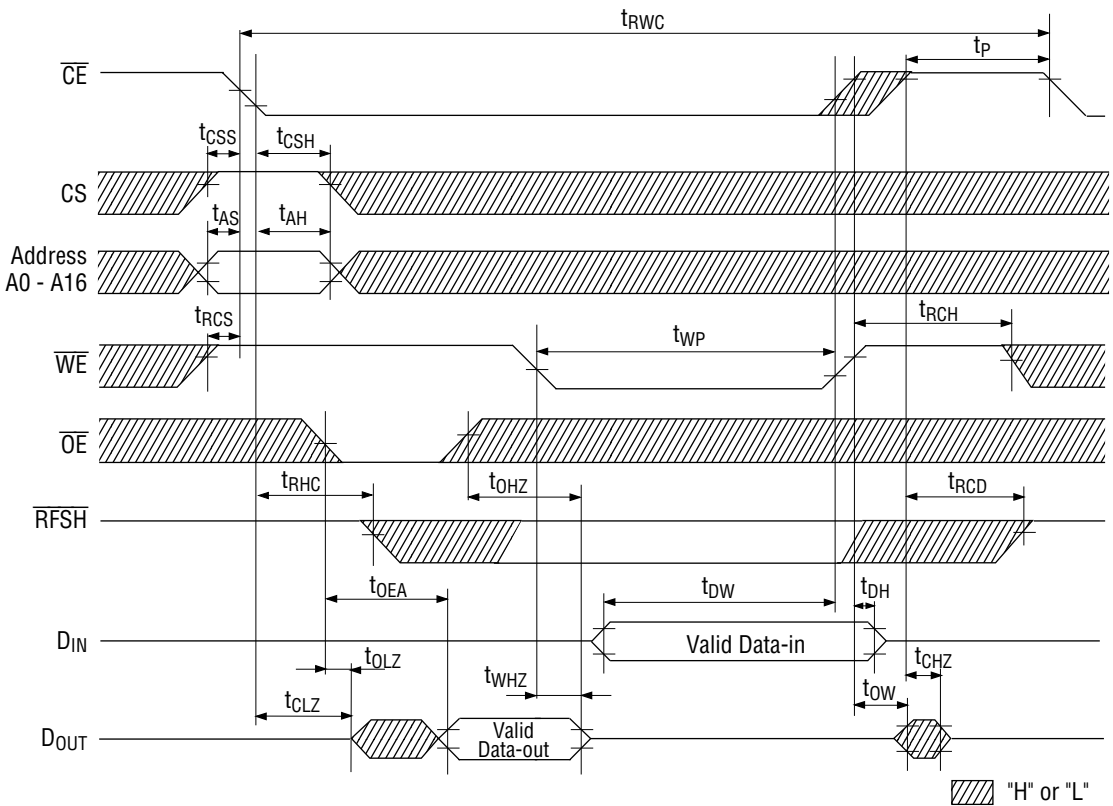




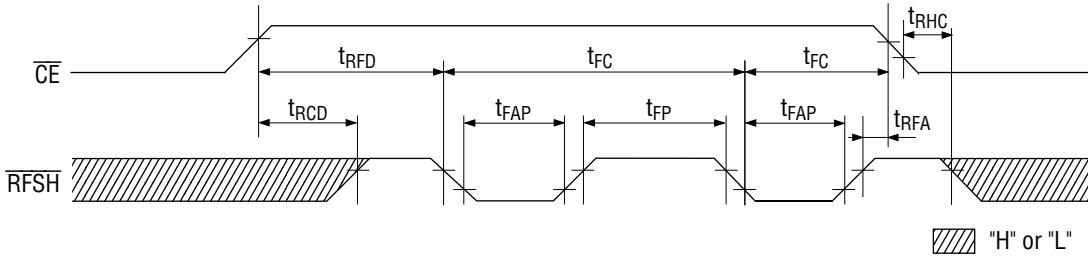
**Write Cycle 2 ( $\overline{OE}$  Low)**



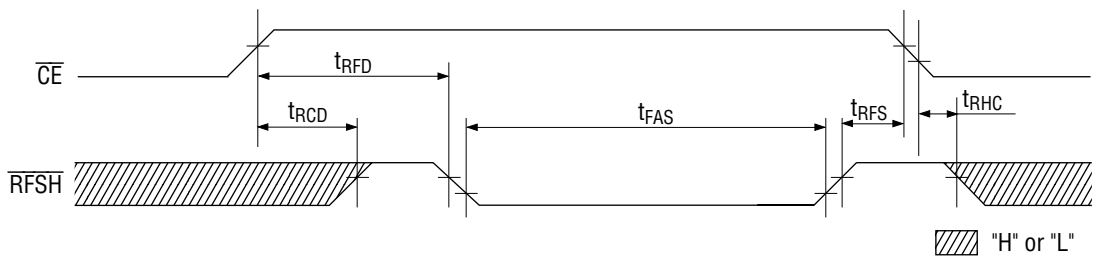
**Read Modify Write Cycle**



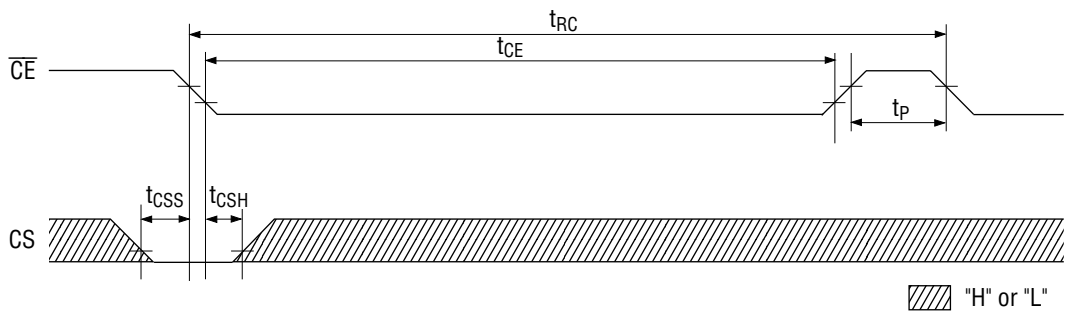
**Auto Refresh Cycle**



**Self Refresh Cycle**

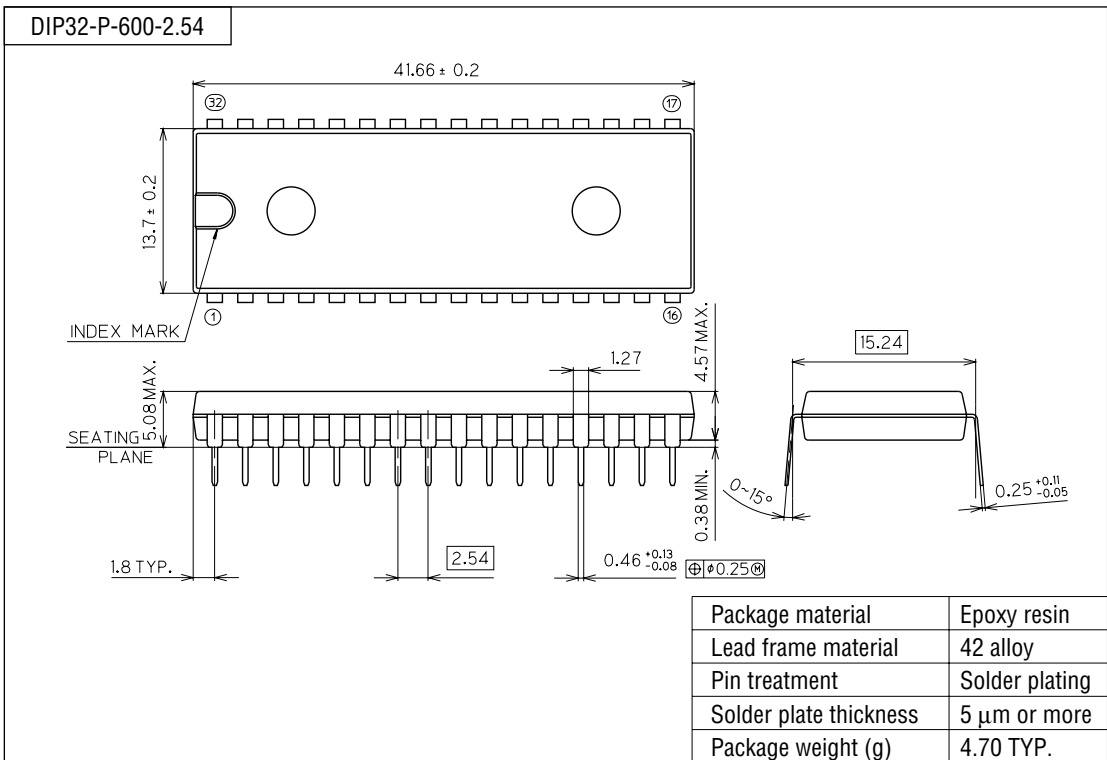


**CS Standby Mode**

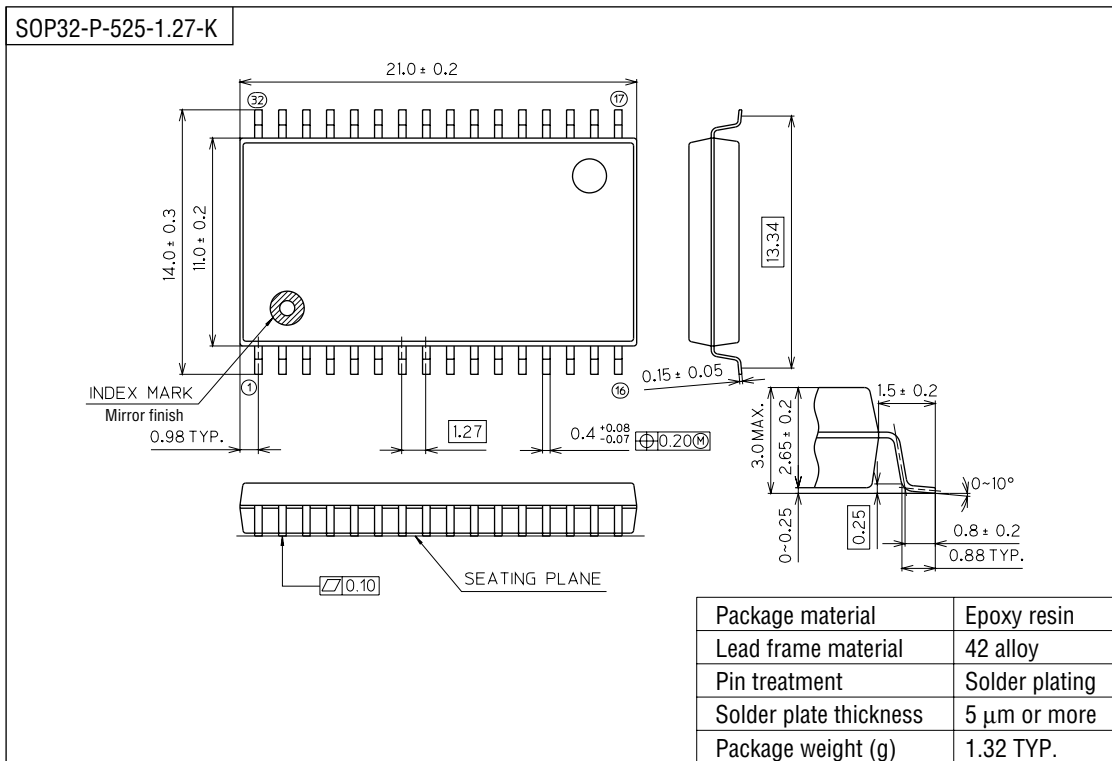


PACKAGE DIMENSIONS

(Unit : mm)



(Unit : mm)



### Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).