

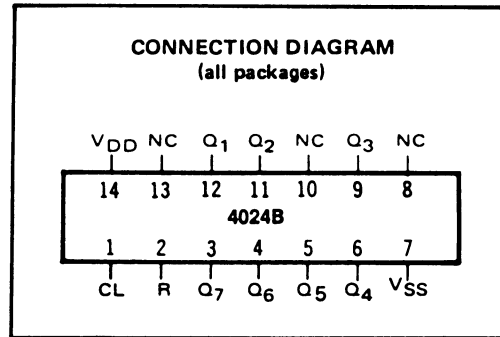
## CMOS 7-STAGE BINARY COUNTER

### FEATURES

- ◆ 7 Fully Static Stages
- ◆ Buffered Outputs Available from All Stages
- ◆ Common Reset Line
- ◆ 8 MHz Counting Rate @ 10Vdc
- ◆ All Inputs Buffered

### DESCRIPTION

The 4024B is a single chip monolithic medium scale integrated circuit containing N-Channel and P-Channel enhancement-mode MOS transistors. Seven single-phase clocked counting stages are provided with the Q output of each stage accessible. The Counter is reset to "zero" by a high level on the Reset input. Each counter stage is a static master-slave flip-flop. The counter state is advanced one count on the negative-going transition of each input pulse.



### TRUTH TABLE

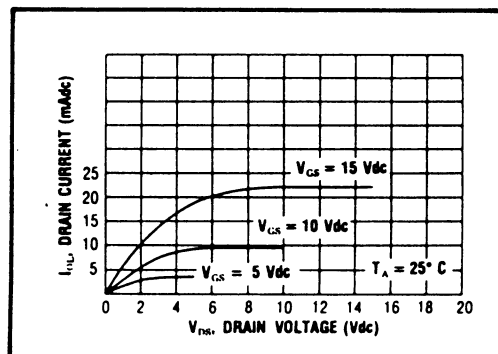
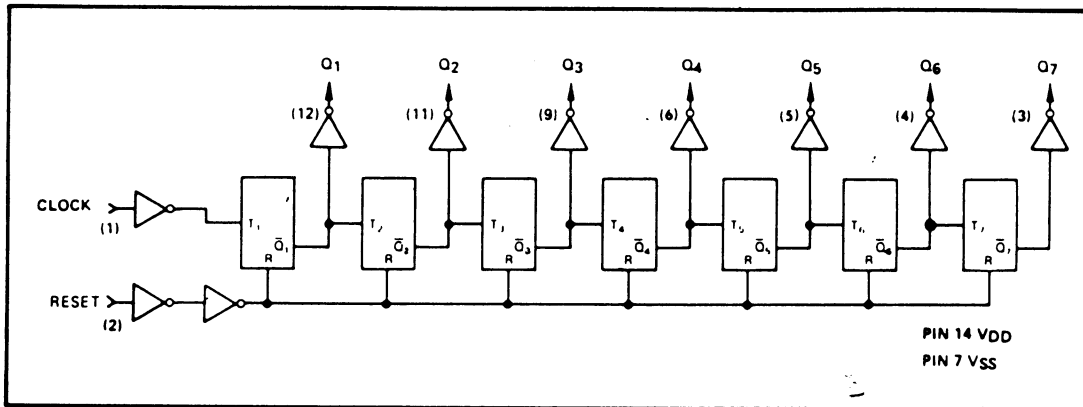
Clock	Reset	State
0	0	No Change
0	1	All Outputs Low
1	0	No Change
1	1	All Outputs Low
	0	No Change
	1	All Outputs Low
	0	Advance One Count
	1	All Outputs Low

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	$T_A$	-55 to +125	°C
		-40 to +85	°C

### LOGIC DIAGRAM



Typical N-Channel  
Sink Current Characteristics

## ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS <sup>1</sup>

PARAMETER	V <sub>DD</sub> (Vdc)	CONDITIONS	T <sub>LOW</sub> <sup>2</sup>		+25°C			T <sub>HIGH</sub> <sup>2</sup>		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I <sub>DD</sub>	V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub> All valid input combinations	-	5	-	0.05	5	-	150	μA <sub>dc</sub>
	5		-	10	-	0.1	10	-	300	
	10		-	20	-	0.2	20	-	600	

NOTES: <sup>1</sup> Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications"

<sup>2</sup> T<sub>LOW</sub> = -55°C for C

= -40°C for E

T<sub>HIGH</sub> = +125°C for C

= + 85°C for E

DYNAMIC CHARACTERISTICS (C<sub>L</sub> = 50 pF, T<sub>A</sub> = 25°C)

PARAMETER	V <sub>DD</sub> (Vdc)	Min.	Typ.	Max.	Units
<b>CLOCKED OPERATION</b>					
PROPAGATION DELAY TIME Clock to Q <sub>1</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	5	-	180	ns
		10	-	80	
		15	-	65	
Q <sub>i</sub> to Q <sub>i+1</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	5	-	100	ns
		10	-	40	
		15	-	30	
OUTPUT TRANSITION TIME	t <sub>TLH</sub> , t <sub>THL</sub>	5	-	100	ns
		10	-	50	
		15	-	40	
MINIMUM CLOCK PULSE WIDTH	PW <sub>CL</sub>	5	-	120	ns
		10	-	60	
		15	-	45	
MAXIMUM CLOCK FREQUENCY	f <sub>CL</sub>	5	2	4	MHz
		10	5	10	
		15	6	12	
MAXIMUM CLOCK RISE AND FALL TIME	t <sub>rCL</sub> , t <sub>fCL</sub>	5	15	-	μs
		10	10	-	
		15	5	-	
<b>RESET OPERATION</b>					
PROPAGATION DELAY TIME	t <sub>PHL</sub>	5	-	200	ns
		10	-	100	
		15	-	80	
MINIMUM RESET PULSE WIDTH	PW <sub>R</sub>	5	-	200	ns
		10	-	100	
		15	-	80	
RESET REMOVAL TIME	t <sub>rem</sub>	5	-	200	ns
		10	-	100	
		15	-	80	

## TYPICAL COUNTER STAGE

