

HB56AW172E Series

1,048,576-word × 72-bit (ECC) High Density Dynamic RAM
Module

HITACHI

ADE-203-252A (Z)

Rev.1.0

Jun. 13, 1996

Description

The HB56AW172E belongs to 8 Byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 4 and 8 Byte processor applications.

The HB56AW172E is a $1\text{M} \times 72$ dynamic RAM module, mounted 18 pieces of 4-Mbit DRAM (HM51W4400BTT) sealed in TSOP package and 2 pieces of 16-bit BiCMOS line driver (74LVT16244DGG) sealed in TSSOP package.

An outline of the HB56AW172E is 168-pin socket type package (dual lead out).

Therefore, the HB56AW172E makes high density mounting possible without surface mount technology. The HB56AW172E provides common data inputs and outputs.

Decoupling capacitors are mounted beside each TSOP on the its module board.

Features

- 168-pin socket type package (dual lead out)
 - Lead pitch: 1.27 mm
- Single 3.3 V (± 0.3 V) supply
- High speed
 - Access time: $t_{\text{RAC}} = 60/70/80$ ns (max)
 - Access time: $t_{\text{CAC}} = 20/25/25$ ns (max)
- Low power dissipation
 - Active mode: 5.22/4.58/3.93 W (max)
 - Standby mode (TTL): 166 mW (max)
- Buffered input except RAS and DQ
- 4 byte interleave enabled, dual address input (A0/B0)
- Fast page mode capability
- 1,024 refresh cycle: 16 ms

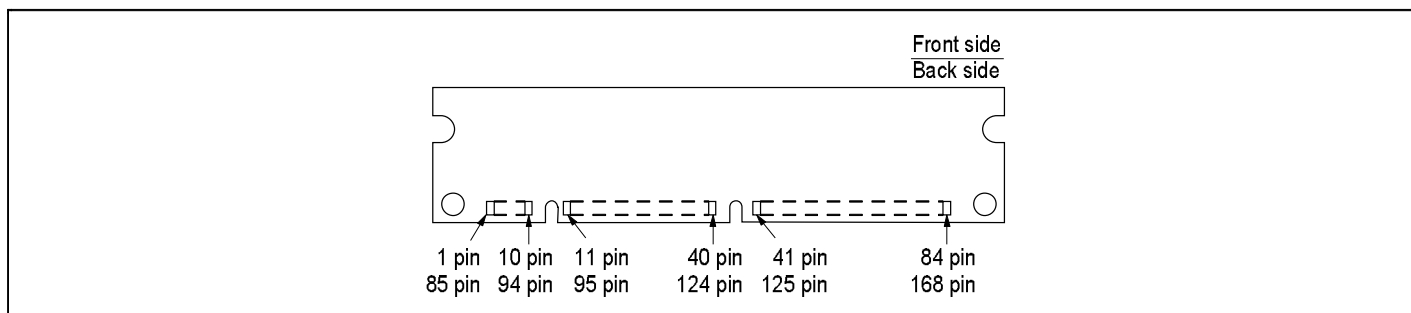
HB56AW172E Series

- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- TTL compatible

Ordering Information

Type No.	Access time	Package	Contact pad
HB56AW172E-6B	60 ns	168-pin dual lead out socket type	Gold
HB56AW172E -7B	70 ns		
HB56AW172E -8B	80 ns		

Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ0	44	$\overline{\text{OE}}2$	86	DQ36	128	NC
3	DQ1	45	$\overline{\text{RE}}2$	87	DQ37	129	NC
4	DQ2	46	$\overline{\text{CE}}4$	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	V_{CC}	48	$\overline{\text{WE}}2$	90	V_{CC}	132	$\overline{\text{PDE}}$
7	DQ4	49	V_{CC}	91	DQ40	133	V_{CC}
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54

Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
11	DQ8	53	DQ19	95	DQ44	137	DQ55
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	V _{CC}	101	DQ49	143	V _{CC}
18	V _{CC}	60	DQ24	102	V _{CC}	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	V _{SS}	65	DQ25	107	V _{SS}	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	$\overline{WE0}$	69	DQ28	111	NC	153	DQ64
28	$\overline{CE0}$	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ66
30	$\overline{RE0}$	72	DQ31	114	NC	156	DQ67
31	$\overline{OE0}$	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ32	116	V _{SS}	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
34	A2	76	DQ34	118	A3	160	DQ70
35	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	PD1	121	A9	163	PD2
38	NC	80	PD3	122	NC	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	V _{CC}	82	PD7	124	V _{CC}	166	PD8
41	NC	83	ID0 (V _{SS})	125	NC	167	ID1 (V _{SS})
42	NC	84	V _{CC}	126	B0	168	V _{CC}

HB56AW172E Series

Pin Description

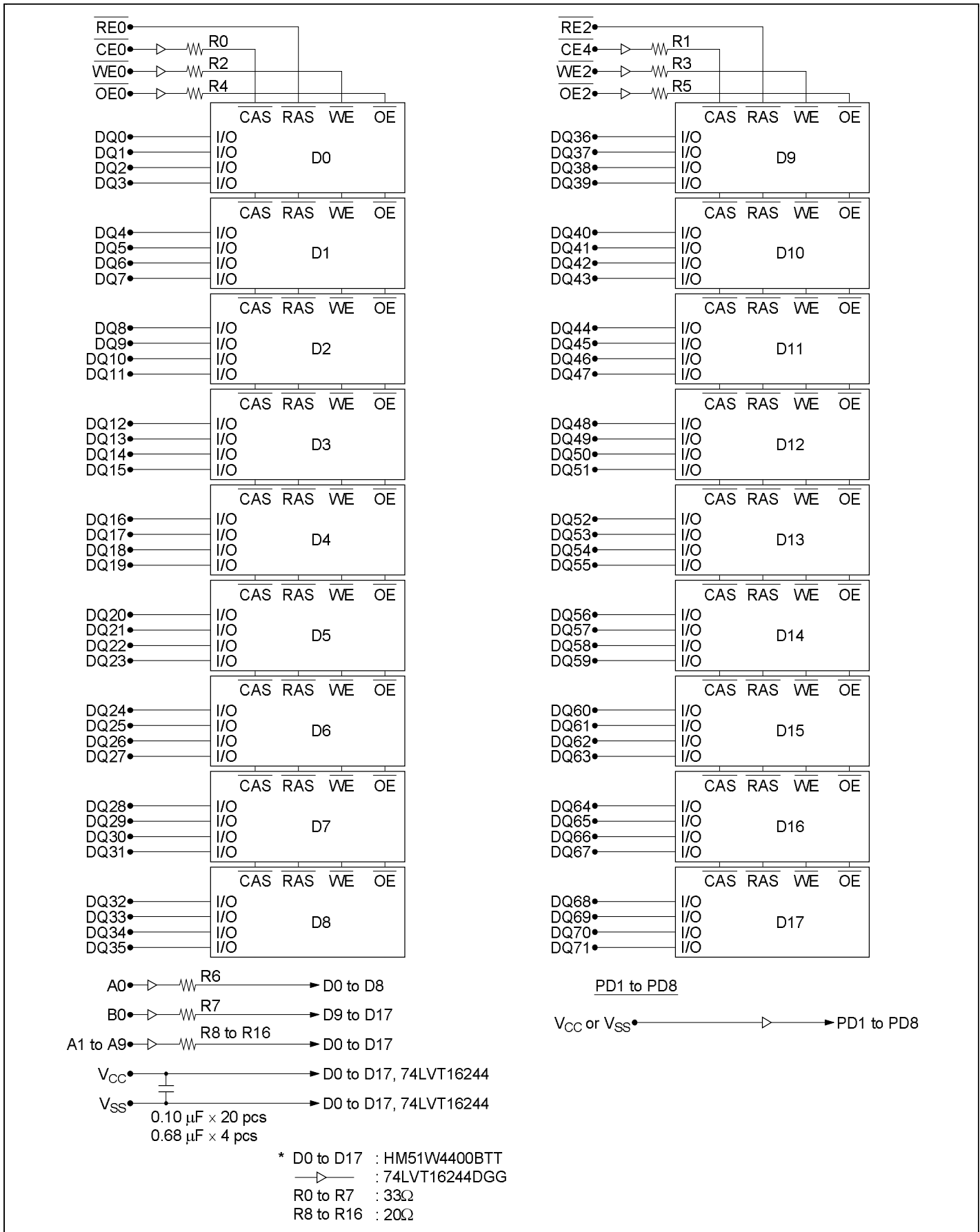
Pin name	Function
A0 to A9, B0	Address input: A0 to A9, B0 Row address: A0 to A9, B0 Column address: A0 to A9, B0 Refresh address: A0 to A9, B0
DQ0 to DQ71	Data-in/Data-out
$\overline{RE0}$, $\overline{RE2}$	Row address strobe
$\overline{CE0}$, $\overline{CE4}$	Column address strobe
$\overline{WE0}$, $\overline{WE2}$	Read/Write enable
$\overline{OE0}$, $\overline{OE2}$	Output enable
V_{CC}	Power supply
V_{SS}	Ground
PD1 to PD8	Presence detect
ID0, ID1	ID bit
\overline{PDE}	Presence detect enable
NC	No connection

Presence Detect Pin Assignment

Pin name	Pin No.	$\overline{PDE} = \text{Low}$			$\overline{PDE} = \text{High}$
		-6B	-7B	-8B	All
PD1	79	0	0	0	High-Z
PD2	163	0	0	0	High-Z
PD3	80	1	1	1	High-Z
PD4	164	0	0	0	High-Z
PD5	81	0	0	0	High-Z
PD6	165	1	0	1	High-Z
PD7	82	1	1	0	High-Z
PD8	166	0	0	0	High-Z

Note: 1: High-Level (Driver Output)
0: Low Level (Driver Output)

Block Diagram



HB56AW172E Series

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_t	19	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.4	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	-0.3	—	0.8	V	1

Note: 1. All voltage referenced to V_{SS} .

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	-6B		-7B		-8B		Unit	Test condition	Note
		Min	Max	Min	Max	Min	Max			
Operating current	I _{CC1}	—	1450	—	1270	—	1090	mA	t _{RC} = min	1, 2
Standby current	I _{CC2}	—	46	—	46	—	46	mA	TTL interface RAS, CAS = V _{IH} Dout = High-Z	
		—	28	—	28	—	28	mA	CMOS interface RAS, CAS ≥ V _{CC} - 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	1450	—	1270	—	1090	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	82	—	82	—	82	mA	RAS = V _{IH} CAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	1450	—	1270	—	1090	mA	t _{RC} = min	
Fast page mode current	I _{CC7}	—	1270	—	1090	—	910	mA	t _{PC} = min	1, 3
Input leakage current	I _{LI}	-10	10	-10	10	-10	10	μA	0 V ≤ Vin ≤ 4.6 V	
Output leakage current	I _{LO}	-10	10	-10	10	-10	10	μA	0 V ≤ Vout ≤ 4.6 V Dout = disable	
Output high voltage	V _{OH}	2.4	V _{CC}	2.4	V _{CC}	2.4	V _{CC}	V	High Iout = -2 mA	
Output low voltage	V _{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while RAS = V_{IL}.

3. Address can be changed once or less while CAS = V_{IH}.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{I1}	—	20	pF	1
Input capacitance (CAS, WE, OE)	C _{I2}	—	20	pF	1
Input capacitance (RAS)	C _{I3}	—	78	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. CAS = V_{IH} to disable Dout.

HB56AW172E Series

AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$) *¹, *¹⁴, *¹⁵

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	110	—	130	—	150	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	—	50	—	60	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	15	10000	20	10000	20	10000	ns	
Row address setup time	t_{ASR}	5	—	5	—	5	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	15	—	15	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	40	20	45	20	55	ns	8
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	25	15	30	15	35	ns	9
$\overline{\text{RAS}}$ hold time	t_{RSH}	20	—	25	—	25	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	60	—	70	—	80	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	15	—	15	—	15	—	ns	
$\overline{\text{OE}}$ to Din delay time	t_{ODD}	20	—	25	—	25	—	ns	
$\overline{\text{OE}}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{\text{CAS}}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	7
Refresh period	t_{REF}	—	16	—	16	—	16	ms	17

Read Cycle

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	—	70	—	80	ns	2, 3
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	—	25	—	25	ns	3, 4, 13
Access time from address	t_{AA}	—	35	—	40	—	45	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	t_{OAC}	—	20	—	25	—	25	ns	3
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	16
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	16
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	35	—	40	—	45	—	ns	
Output buffer turn-off time	t_{OFF1}	0	20	0	25	0	25	ns	6
Output buffer turn-off to $\overline{\text{OE}}$	t_{OFF2}	0	20	0	25	0	25	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	20	—	25	—	25	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	20	—	20	—	ns	

Write Cycle

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	10
Write command hold time	t_{WCH}	15	—	15	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20	—	25	—	25	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	—	20	—	20	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in hold time	t_{DH}	20	—	20	—	20	—	ns	11

HB56AW172E Series

Read-Modify-Write Cycle

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	150	—	180	—	200	—	ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	85	—	100	—	110	—	ns	10
\overline{CAS} to \overline{WE} delay time	t_{CWD}	35	—	45	—	45	—	ns	10
Column address to \overline{WE} delay time	t_{AWD}	50	—	60	—	65	—	ns	10
\overline{OE} hold time from \overline{WE}	t_{OEh}	15	—	20	—	20	—	ns	

Refresh Cycle

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
\overline{CAS} setup time (CBR refresh cycle)	t_{CSR}	15	—	15	—	15	—	ns	
\overline{CAS} hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	10	—	ns	
\overline{WE} setup time	t_{WS}	5	—	5	—	5	—	ns	
\overline{WE} hold time	t_{WH}	10	—	10	—	10	—	ns	
\overline{RAS} precharge to \overline{CAS} hold time	t_{RPC}	10	—	10	—	10	—	ns	
\overline{CAS} precharge time in normal mode	t_{CPN}	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	40	—	45	—	50	—	ns	
\overline{CAS} precharge time	t_{CP}	10	—	10	—	10	—	ns	
Fast page mode \overline{RAS} pulse width	t_{RASC}	—	100000	—	100000	—	100000	ns	12
Access time from \overline{CAS} precharge	t_{ACP}	—	40	—	45	—	50	ns	3, 13
\overline{RAS} hold time from \overline{CAS} precharge	t_{RHCP}	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Parameter	Symbol	-6B		-7B		-8B		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Fast page mode read-modify-write cycle time	t_{PCM}	80	—	95	—	100	—	ns	
\overline{WE} delay time from \overline{CAS} precharge	t_{CPW}	55	—	65	—	70	—	ns	10

Notes: 1. AC measurements assume $t_T = 5$ ns.

2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
6. $t_{OFF}(\text{max})$ defines the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
10. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referred to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
12. t_{RASc} defines \overline{RAS} pulse width in Fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (\overline{RAS} -only refresh or \overline{CAS} -before- \overline{RAS} refresh cycle). If the internal refresh counter is used, a minimum of eight \overline{CAS} -before- \overline{RAS} refresh cycle is required.
15. In delayed write or read-modify-write cycles, \overline{OE} must disable output buffer prior to applying data to the device.
16. Either t_{RCH} or t_{RRH} must be satisfied.
17. t_{REF} is determined by 1,204 refresh cycle.

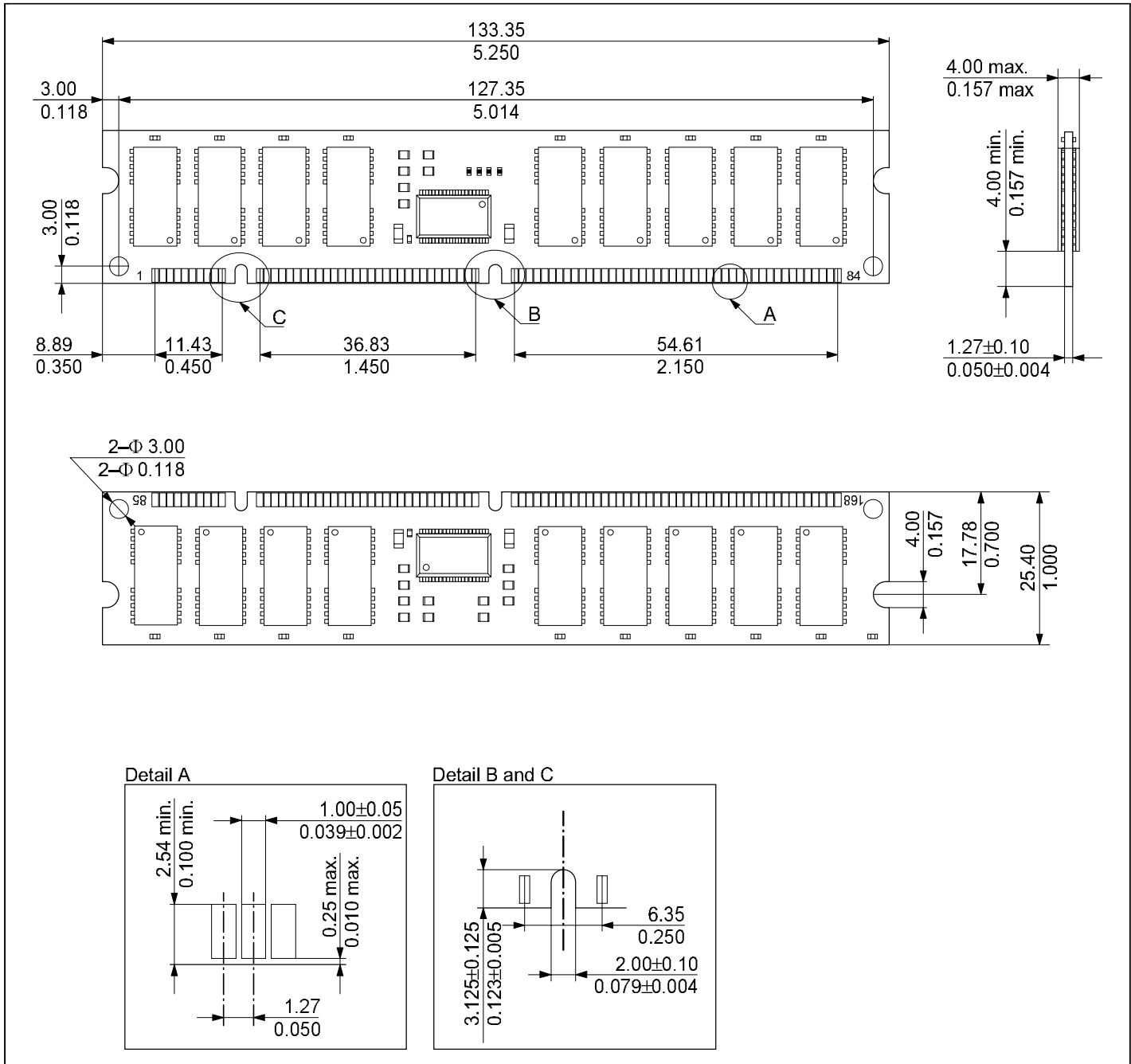
Timing Waveform

Refer to the HB56G236B/SB Series.

HB56AW172E Series

Physical Outline

Unit: mm/inch



When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. **MEDICAL APPLICATIONS:** Hitachi's products are not authorized for use in **MEDICAL APPLICATIONS** without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in **MEDICAL APPLICATIONS**.

HITACHI

Hitachi, Ltd.

Semiconductor & IC Div.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan
Tel: Tokyo (03) 3270-2111
Fax: (03) 3270-5109

For further information write to:

Hitachi America, Ltd.
Semiconductor & IC Div.
2000 Sierra Point Parkway
Brisbane, CA. 94005-1835
U S A
Tel: 415-589-8300
Fax: 415-583-4207

Hitachi Europe GmbH
Electronic Components Group
Continental Europe
Dornacher Straße 3
D-85622 Feldkirchen
München
Tel: 089-9 91 80-0
Fax: 089-9 29 30 00

Hitachi Europe Ltd.
Electronic Components Div.
Northern Europe Headquarters
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA
United Kingdom
Tel: 0628-585000
Fax: 0628-778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 0104
Tel: 535-2100
Fax: 535-1533

Hitachi Asia (Hong Kong) Ltd.
Unit 706, North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon
Hong Kong
Tel: 27359218
Fax: 27306071