

- **Organization**
 TM124BBK32H/I . . . 1 048 576 × 32
 TM248CBK32H/I . . . 2 097 152 × 32
- **Single 5-V Power Supply (±10% Tolerance)**
- **72-Pin Single In-Line Memory Module (SIMM) for Use With Socket**
- **TM124BBK32H/I – Uses Two 16M-Bit DRAMs in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248CBK32H/I – Uses Four 16M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
 16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL-Compatible**
- **3-State Output**
- **Common $\overline{\text{CAS}}$ Control for Eight Common Data-In and Data-Out Lines in Four Blocks**
- **Enhanced Page-Mode Operation With $\overline{\text{CAS}}$ -Before-RAS (CBR), RAS-Only, and Hidden Refresh**

- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME †RAC (MAX)	ACCESS TIME ‡AA (MAX)	ACCESS TIME ‡CAC (MAX)	READ OR WRITE CYCLE (MIN)
*124BBK32H/I-50	50 ns	25 ns	13 ns	90 ns
*124BBK32H/I-60	60 ns	30 ns	15 ns	110 ns
*124BBK32H/I-70	70 ns	35 ns	18 ns	130 ns
*248CBK32H/I-50	50 ns	25 ns	13 ns	90 ns
*248CBK32H/I-60	60 ns	30 ns	15 ns	110 ns
*248CBK32H/I-70	70 ns	35 ns	18 ns	130 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range**
 0°C to 70°C
- **Gold-Tabbed Versions Available:†**
 TM124BBK32H
 TM248CBK32H
- **Tin-Lead (Solder) Tabbed Versions Available:**
 TM124BBK32I
 TM248CBK32I

description

TM124BBK32H/I

The TM124BBK32H/I is a 32M-bit dynamic random-access memory (DRAM) module organized as four times 1048576 × 8 in a 72-pin SIMM. The SIMM is composed of two TMS418160ADZ, 1 048 576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160ADZ is described in the TMS418160A data sheet (literature number SMKS891). The TM124BBK32H/I SIMM is available in the single-sided BK-leadless module for use with sockets.

TM248CBK32H/I

The TM248CBK32H/I is a 64M-bit DRAM organized as four times 2 097 152 × 8 in a 72-pin SIMM. The SIMM is composed of four TMS418160ADZ, 1048576 × 16-bit DRAMs, each in a 42-lead plastic SOJ package mounted on a substrate with decoupling capacitors. The TMS418160ADZ is described in the TMS418160A data sheet (literature number SMKS891). The TM248CBK32H/I SIMM is available in the double-sided BK-leadless module for use with sockets.

operation

The TM124BBK32H/I operates as two TMS418160ADZ DRAMs, connected as shown in the functional block diagram and Table 1. The TM248CBK32H/I operates as four TMS418160ADZ DRAMs connected as shown in the functional block diagram and Table 1. The common I/O feature dictates the use of early-write cycles to prevent contention on D and Q.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

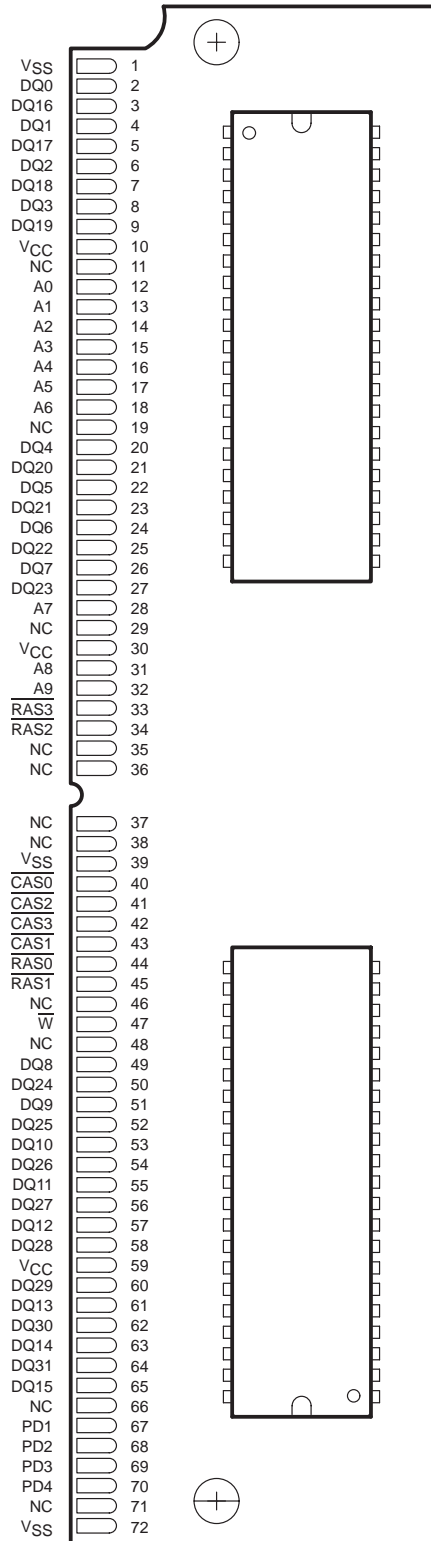


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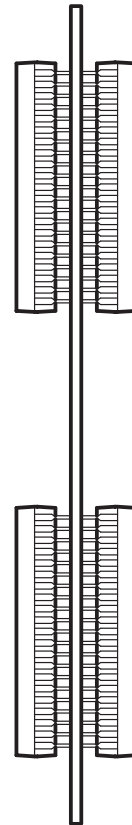
BK SINGLE-IN-LINE MEMORY MODULE
(TOP VIEW)



TM124BBK32H/I
(SIDE VIEW)



TM248CBK32H/I
(SIDE VIEW)



PIN NOMENCLATURE	
A0–A9	Address Inputs
CAS0–CAS3	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1–PD4	Presence Detects
RAS0–RAS3	Row-Address Strobe
VCC	5-V Supply
VSS	Ground
W	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		PD1 (67)	PD2 (68)	PD3 (69)	PD4 (70)
TM124BBK32H/I	50 ns	VSS	VSS	VSS	VSS
	60 ns	VSS	VSS	NC	NC
	70 ns	VSS	VSS	VSS	NC
TM248CBK32H/I	50 ns	NC	NC	VSS	VSS
	60 ns	NC	NC	NC	NC
	70 ns	NC	NC	VSS	NC

operation (continued)

Table 1. Connection Table

DATA BLOCK	RASx		CASx
	SIDE 1	SIDE 2†	
DQ0–DQ7	RAS0	RAS1	CAS0
DQ8–DQ15	RAS0	RAS1	CAS1
DQ16–DQ23	RAS2	RAS3	CAS2
DQ24–DQ31	RAS2	RAS3	CAS3

† Side 2 applies to the TM248CBK32H/I only.

single in-line memory module and components

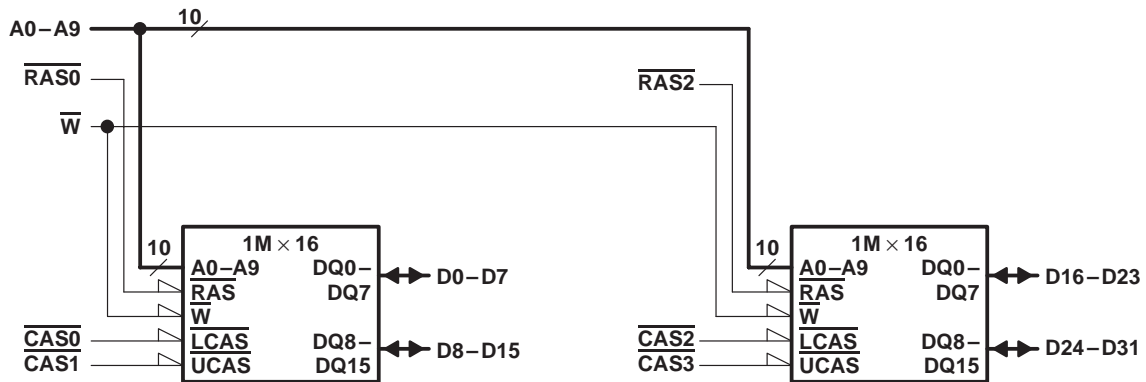
PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage

Bypass capacitors: Multilayer ceramic

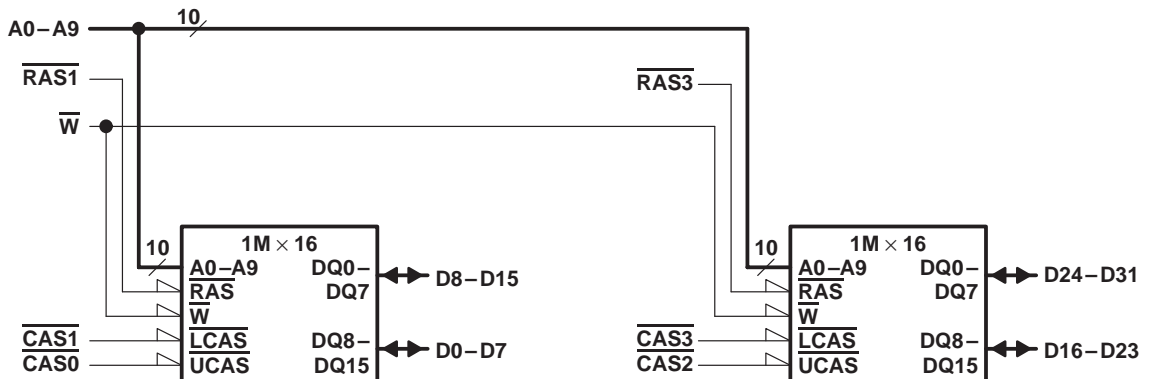
Contact area for TM124BBK32H and TM248CBK32H: Nickel plate and gold plate over copper

Contact area for TM124BBK32I and TM248CBK32I: Nickel plate and tin/lead over copper

functional block diagram (TM124BBK32H/I and TM248CBK32H/I, side 1)



functional block diagram (TM248CBK32H/I, side 2)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	– 1 V to 7 V
Voltage range on any pin (see Note 1)	– 1 V to 7 V
Short-circuit output current	50 mA
Power dissipation: TM124BBK32H, TM124BBK32I	2 W
TM248CBK32H, TM248CBK32I	4 W
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	– 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2.4		6.5	V
V_{IL} Low-level input voltage (see Note 2)	– 1		0.8	V
T_A Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡	'124BBK32H/I-50		'124BBK32H/I-60		'124BBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH} High-level output voltage	$I_{OH} = -5$ mA	2.4		2.4		2.4		V
V_{OL} Low-level output voltage	$I_{OL} = 4.2$ mA		0.4		0.4		0.4	V
I_I Input current (leakage)	$V_{CC} = 5.5$ V, $V_I = 0$ V to 6.5 V, All other pins = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O Output current (leakage)	$V_{CC} = 5.5$ V, $V_O = 0$ V to V_{CC} , CAS high		± 10		± 10		± 10	µA
I_{CC1} Read- or write-cycle current	$V_{CC} = 5.5$ V, Minimum cycle		360		320		300	mA
I_{CC2} Standby current	$V_{IH} = 2.4$ V (TTL), After 1 memory cycle, RAS and CAS high		4		4		4	mA
	$V_{IH} = V_{CC} - 0.2$ V (CMOS), After 1 memory cycle, RAS and CAS high		2		2		2	mA
I_{CC3} Average refresh current (RAS only or CBR)	$V_{CC} = 5.5$ V, Minimum cycle, RAS cycling, CAS high (RAS only); RAS low after CAS low (CBR)		360		320		300	mA
I_{CC4} Average page current	$V_{CC} = 5.5$ V, $t_{PC} = \text{MIN}$, RAS low, CAS cycling		220		180		160	mA

‡ For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	'248CBK32H/I-50		'248CBK32H/I-60		'248CBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH} High-level output voltage	I _{OH} = -5 mA	2.4		2.4		2.4		V
V _{OL} Low-level output voltage	I _{OL} = 4.2 mA		0.4		0.4		0.4	V
I _I Input current (leakage)	V _{CC} = 5.5 V, V _I = 0 V to 6.5 V, All other pins = 0 V to V _{CC}		± 10		± 10		± 10	µA
I _O Output current (leakage)	V _{CC} = 5.5 V, V _O = 0 V to V _{CC} , $\overline{\text{CAS}}$ high		± 20		± 20		± 20	µA
I _{CC1} Read- or write-cycle current (see Note 3)	V _{CC} = 5.5 V, Minimum cycle		368		328		308	mA
I _{CC2} Standby current	V _{IH} = 2.4 V (TTL), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		8		8		8	mA
	V _{IH} = V _{CC} - 0.2 V (CMOS), After 1 memory cycle, $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ high		4		4		4	mA
I _{CC3} Average refresh current ($\overline{\text{RAS}}$ only or CBR) (see Note 3)	V _{CC} = 5.5 V, Minimum cycle, $\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ high ($\overline{\text{RAS}}$ only); $\overline{\text{RAS}}$ low after $\overline{\text{CAS}}$ low (CBR)		720		640		600	mA
I _{CC4} Average page current (see Note 4)	V _{CC} = 5.5 V, $\overline{\text{RAS}}$ low, t _{PC} = MIN, $\overline{\text{CAS}}$ cycling		440		360		320	mA

† For test conditions shown as MIN/MAX, use the appropriate value specified under recommended operating conditions.

- NOTES: 3. Measured with a maximum of one address change while $\overline{\text{RAS}}$ = V_{IL}
 4. Measured with a maximum of one address change while $\overline{\text{CAS}}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 5)

PARAMETER	'124BBK32H/I		'248CBK32H/I		UNIT
	MIN	MAX	MIN	MAX	
C _{i(A)} Input capacitance, A0–A9		10		20	pF
C _{i(R)} Input capacitance, $\overline{\text{RAS}}$ inputs		7		7	pF
C _{i(C)} Input capacitance, $\overline{\text{CAS}}$ inputs		7		14	pF
C _{i(W)} Input capacitance, $\overline{\text{W}}$		14		28	pF
C _{o(DQ)} Output capacitance on DQ0–DQ31		7		14	pF

NOTE 5: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.



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switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	'124BBK32H/I-50 '248CBK32H/I-50		'124BBK32H/I-60 '248CBK32H/I-60		'124BBK32H/I-70 '248CBK32H/I-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AA} Access time from column address	25		30		35		ns
t _{CAC} Access time from $\overline{\text{CAS}}$ low	13		15		18		ns
t _{RAC} Access time from $\overline{\text{RAS}}$ low	50		60		70		ns
t _{CPA} Access time from column precharge	30		35		40		ns
t _{CLZ} $\overline{\text{CAS}}$ to output in the low-impedance state	0		0		0		ns
t _{OH} Output disable time from start of $\overline{\text{CAS}}$ high	3		3		3		ns
t _{OFF} Output disable time after $\overline{\text{CAS}}$ high (see Note 6)	0	13	0	15	0	18	ns

NOTE 6: t_{OFF} is specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

	'124BBK32H/I-50 '248CBK32H/I-50		'124BBK32H/I-60 '248CBK32H/I-60		'124BBK32H/I-70 '248CBK32H/I-70		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
t _{RC} Cycle time, random read or write (see Note 7)	90		110		130		ns
t _{RWC} Cycle time, read-write	131		155		181		ns
t _{PC} Cycle time, page-mode read or write (see Notes 7 and 8)	35		40		45		ns
t _{RASP} Pulse duration, page mode, $\overline{\text{RAS}}$ low	50	100 000	60	100 000	70	100 000	ns
t _{RAS} Pulse duration, nonpage mode, $\overline{\text{RAS}}$ low	50	10 000	60	10 000	70	10 000	ns
t _{CAS} Pulse duration, $\overline{\text{CAS}}$ low	13	10 000	15	10 000	18	10 000	ns
t _{CP} Pulse duration, $\overline{\text{CAS}}$ high	8		10		10		ns
t _{RP} Pulse duration, $\overline{\text{RAS}}$ high (precharge)	30		40		50		ns
t _{WP} Pulse duration, $\overline{\text{W}}$ low	10		10		10		ns
t _{ASC} Setup time, column address before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{ASR} Setup time, row address before $\overline{\text{RAS}}$ low	0		0		0		ns
t _{DS} Setup time, data before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{RCS} Setup time, $\overline{\text{W}}$ high before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CWL} Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ high	13		15		18		ns
t _{RWL} Setup time, $\overline{\text{W}}$ low before $\overline{\text{RAS}}$ high	13		15		18		ns
t _{WCS} Setup time, $\overline{\text{W}}$ low before $\overline{\text{CAS}}$ low	0		0		0		ns
t _{CAH} Hold time, column address after $\overline{\text{CAS}}$ low	10		10		15		ns
t _{RHCP} Hold time, $\overline{\text{RAS}}$ high from $\overline{\text{CAS}}$ precharge	30		35		40		ns
t _{DH} Hold time, data after $\overline{\text{CAS}}$ low	10		10		15		ns
t _{RAH} Hold time, row address after $\overline{\text{RAS}}$ low	8		10		10		ns
t _{RCH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{CAS}}$ high (see Note 9)	0		0		0		ns
t _{RRH} Hold time, $\overline{\text{W}}$ high after $\overline{\text{RAS}}$ high (see Note 9)	0		0		0		ns

- NOTES: 7. All cycles assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be ≥ t_{CP}.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.



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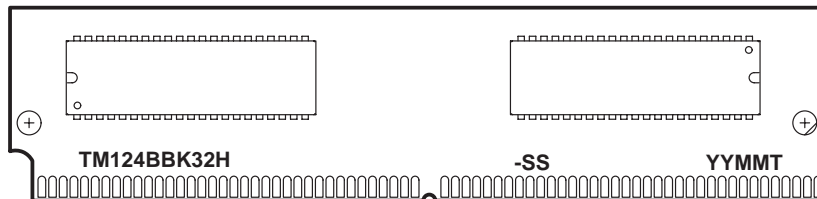
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timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124BBK32H/I-50 '248CBK32H/I-50		'124BBK32H/I-60 '248CBK32H/I-60		'124BBK32H/I-70 '248CBK32H/I-70		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _{WCH}	Hold time, \overline{W} low after \overline{CAS} low	10		10		15		ns
t _{CHR}	Delay time, \overline{RAS} low to \overline{CAS} high (CBR refresh only)	10		10		10		ns
t _{CRP}	Delay time, \overline{CAS} high to \overline{RAS} low	5		5		5		ns
t _{CSH}	Delay time, \overline{RAS} low to \overline{CAS} high	50		60		70		ns
t _{CSR}	Delay time, \overline{CAS} low to \overline{RAS} low (CBR refresh only)	5		5		5		ns
t _{RAD}	Delay time, \overline{RAS} low to column address (see Note 10)	13	25	15	30	15	35	ns
t _{RAL}	Delay time, column address to \overline{RAS} high	25		30		35		ns
t _{CAL}	Delay time, column address to \overline{CAS} high	25		30		35		ns
t _{RCD}	Delay time, \overline{RAS} low to \overline{CAS} low (see Note 10)	18	37	20	45	20	52	ns
t _{RPC}	Delay time, \overline{RAS} high to \overline{CAS} low (CBR only)	5		5		5		ns
t _{RSH}	Delay time, \overline{CAS} low to \overline{RAS} high	13		15		18		ns
t _{REF}	Refresh time interval		16		16		16	ms
t _T	Transition time	2	30	2	30	2	30	ns

NOTE 10: The maximum value is specified only to ensure access time.

device symbolization (TM124BBK32H/I illustrated)



- YY = Year Code
- MM = Month Code
- T = Assembly Site Code
- SS = Speed Code

NOTE A: Location of symbolization may vary.

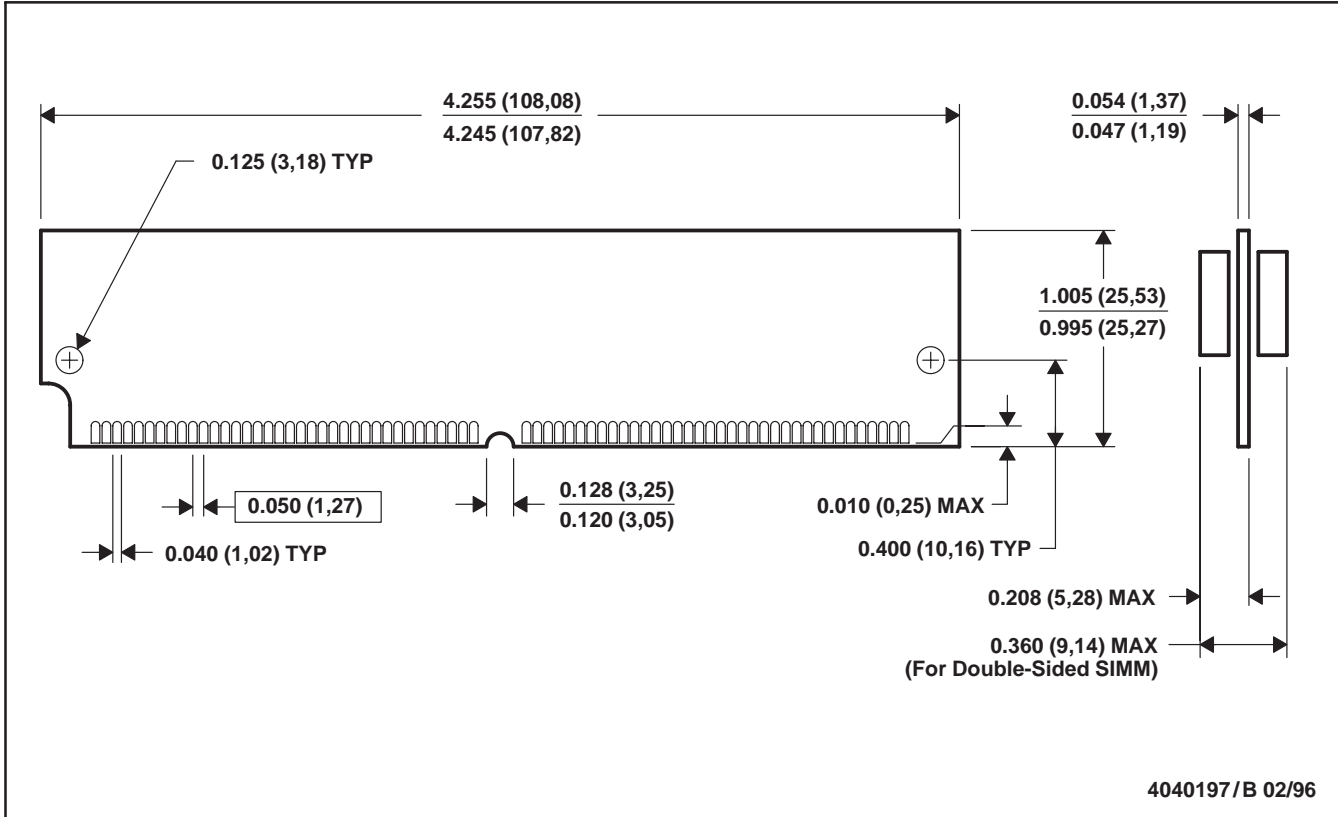
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MECHANICAL DATA

BK (R-PSIM-N72)

SINGLE-IN-LINE MEMORY MODULE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

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