



2.488 GBPS SONET/SDH TRANSCEIVER WITH INTERNAL LOOP TIMING

FEATURES

- 2.488-Gbps SONET/SDH transceiver with dual differential serial I/O
- Fully integrated CDR, MUX, DEMUX, and CMU
- Selectable LVPECL/CMOS 16-bit, 155.52-Mbps interface to framer or network processor
- On-chip PLL-based clock generator
- Line and system loopback modes
- Loss-of-signal output (LOS_B) and input (LOS_IB)
- TX and RX lock detect
- Elastic buffering with FIFO overflow alarm
- Selectable 77.76/155.52-MHz reference clock
- Selectable RX clock and RX data squelch on LOS
- Selectable loop timing mode
- Single 2.5V or dual 2.5V/3.3V supplies
- Power dissipation: 1.2W typical
- 14 × 20 mm, 128-pin PQFP package
- Standard CMOS fabrication process

SUMMARY OF BENEFITS

- Low power consumption eliminates external heat sinks, fans for system airflow, and expensive high current power supplies.
- Supports SONET dual-fiber ring architecture.
- High integration reduces design cycle and time to market.
- Provides increased port density per board and system.
- CMOS-based device uses the most effective silicon economy of scale.
- Meets SONET jitter requirements.
- Features low jitter: 3 mUI_{rms} typical.

APPLICATIONS

- OC-48/STM-16 transmission equipment
- SONET/SDH optical modules
- ADD/DROP multiplexers
- Digital cross-connects
- ATM switch backbone
- SONET/SDH test equipment
- Terabit and edge routers

BCM8211 Application Block Diagram

