



# TOSHIBA Bi-CMOS Constant Current Interface Driver

## TB62707F

8 Bit Constant Current LED Driver with Latch Function

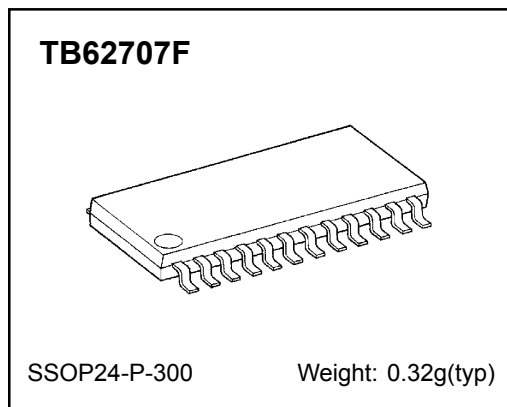
### Product Description:

The TB62707F is specifically designed for LED display applications. The Bi-CMOS device has 8 Bi-polar constant current output channels and includes CMOS latch function.

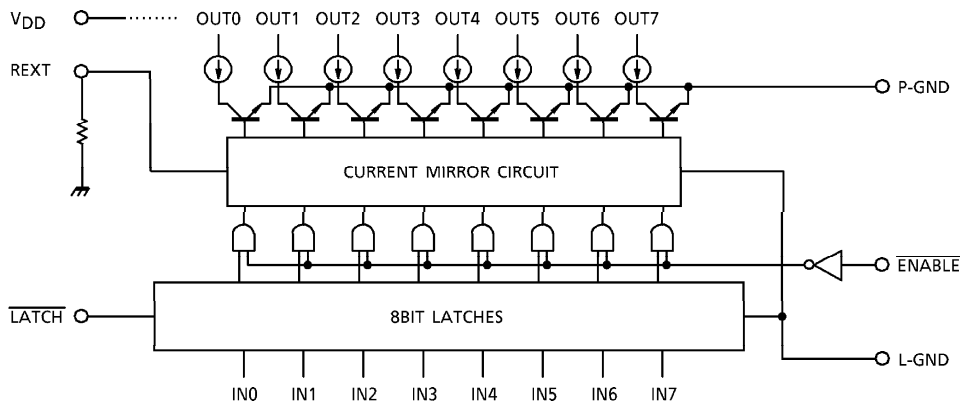
The LED drive current is programmed by the installation of a single resistor per device. Current is programmable from 5-90mA and is held constant across all 8 outputs effectively compensating for the inherent circuit and component variables which affect the brightness of the LEDs.

### Features:

- 8 Constant Current Output Channels
- Current Programmable from 5-90mA
- 5V CMOS Compatible Inputs
- Surface Mount Package



### Block Diagram:



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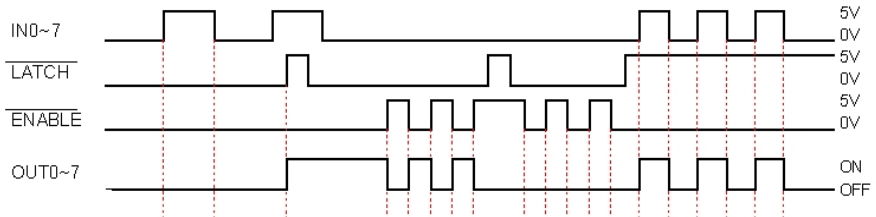
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### Timing Diagram:



#### Latches are:

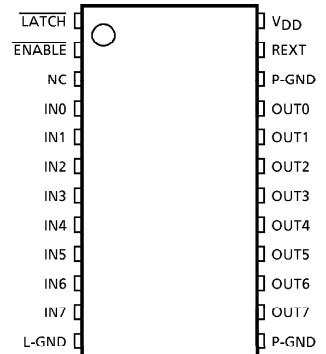
1. Level Sensitive ( Not edge sensitive )
2. Through the Data D to Q when LATCH signal is "Hi".
3. Hold the Data Q when LATCH signal is "Lo".

#### Output are:

All outputs are ON when Q of latches are "Hi", and all outputs are OFF when Q of latches are "Lo".

### Terminal Description & Pin Out:

PIN No.	PIN NAME	FUNCTION
12	L-GND	GND terminal for control logic.
13,22	P-GND	GND terminal for output constant current drivers.
4~11	IN0~7	Input terminal of a parallel-data for latches.
1	LATCH	Input terminal of a data strobe. Latches passes data with "H" level input of LATCH-terminal, and hold data with "L" level input.
14~21	OUT0~7	Output terminals.
2	ENABLE	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of ENABLE-terminal, and do on with "L" level input.
23	R-EXT	Input terminal of connects with a resistor for to set up all output current.
24	VDD	5V Supply voltage terminal



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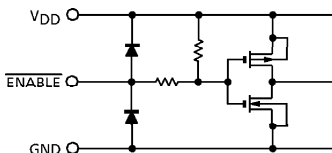
## TB62707F

Truth Table:

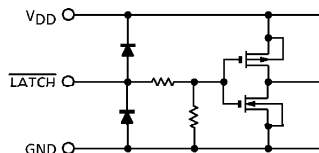
IN0-7	LATCH	ENABLE	OUT0-7
L	L	L	OFF
H	L	L	OFF
L	H	L	OFF
H	H	L	ON
L		L	OFF
H		L	ON
H		H	OFF

Equivalent Circuit of Inputs and Outputs:

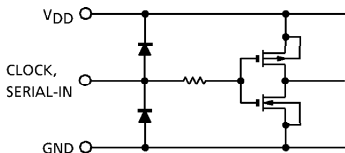
1. ENABLE terminal



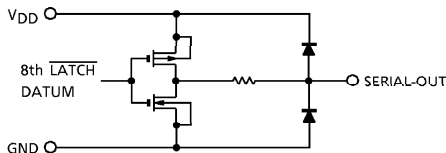
2. LATCH terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



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### Maximum Ratings:

CHARACTER	SYMBOL	RATING	UNIT
Supply Voltage	VDD	+7.0	V
Output Voltage	VOUT	-0.5~+17.0	V
Output Current	IOUT	+90	mA
Input Voltage	VIN	-0.3~VDD + 0.3	V
GND Terminal Current	IGND	720	mA
Power Dissipation	PD	0.78	W
Operating Temperature	Topr	-40~+85	°C
Storage Temperature	Tstg	-55~+150	°C

\* On 50 x 50 x 1.66mm 30% Copper, Glass Epoxy PWB  
Ambient Temperature Derated 6.66mW/°C above 25°C

### Recommended Operating Condition:

CHARACTER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	VDD		4.5	5.0	5.5	V
Output Voltage	VOUT		—	—	15.0	V
Output Current	IOUT	DC 1 Circuit	5	—	88	mA
	IOH	SERIAL-OUT	—	—	-1.0	mA
	IOL	SERIAL-OUT	—	—	1.0	mA
Input Voltage	VIH		0.7VDD	—	VDD+0.3	V
	VIL		-0.3	—	0.3VDD	V
LATCH Pulse Width INPUT Pulse Width ENABLE Pulse Width	tw LAT	VDD=4.5 ~ 5.5V	100	—	—	ns
	tw IN		4500	—	—	ns
	tw EN		4500	—	—	ns
Set-up Time for LATCH	tsetup(L)		100	—	—	ns
Hold Time for ENABLE	thold(L)		100	—	—	ns
Power Dissipation	P <sub>o</sub>		ON PCB, Ta=85°C	—	—	0.6

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# TOSHIBA Bi-CMOS

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### Electrical Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" level	V <sub>IH</sub>	—	—	0.7V <sub>DD</sub>	—	V <sub>DD</sub>	V
	"L" level	V <sub>IL</sub>	—	—	GND	—	0.3V <sub>DD</sub>	
Output Leakage Current		I <sub>OH</sub>	—	VOH=15.0V	—	—	10	μA
Output Voltage	SERIAL--OUT	V <sub>OL</sub>	—	I <sub>OL</sub> =+1.0mA	—	—	0.4	V
		V <sub>OH</sub>	—	I <sub>OH</sub> =-1.0mA	4.6	—	—	V
Output Current 1		I <sub>OL1</sub>	—	V <sub>CE</sub> =0.7V	REXT=620Ω (include Current Matching)	35.7	42	48.3
		I <sub>OL2</sub>	—	V <sub>CE</sub> =0.4V		68	80	
Current Skew		dI <sub>OL1</sub>	—	I <sub>O</sub> =40mA, V <sub>CE</sub> =0.4V	REXT=620Ω	—	±1.5	±6.0
Output Current 2		I <sub>OL3</sub>	—	V <sub>CE</sub> =0.4V	REXT=330Ω (include Current Matching)	64.2	75.5	86.8
		I <sub>OL4</sub>	—	V <sub>CE</sub> =0.7V		63.8	75.0	
Current Skew		dI <sub>OL2</sub>	—	I <sub>O</sub> =75mA, V <sub>CE</sub> =0.7V	REXT=330Ω	—	±1.5	±5.0
Supply Voltage Regulation		% / V <sub>DD</sub>	—	REXT=470Ω Ta=40~+85°C	—	5	—	% / V
Supply Current	"OFF"	I <sub>IDD (off) 1</sub>	—	REXT=OPEN OUT-8=off	—	0.6	1.2	mA
		I <sub>IDD (off) 2</sub>	—	REXT=500Ω OUT-8=off	6	8	10	
		I <sub>IDD (off) 3</sub>	—	REXT=280Ω OUT-8=off	12	15	18	
	"ON"	I <sub>IDD (on)1</sub>	—	REXT=500Ω OUT-8=on	8	13	20	
		I <sub>IDD (on)2</sub>	—	REXT=280Ω OUT-8=on	18	25	35	
Reference Voltage		U <sub>ref</sub>	—	—	—	1.26	—	V

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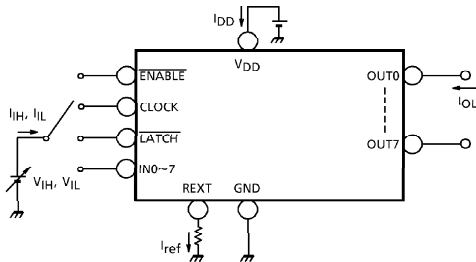


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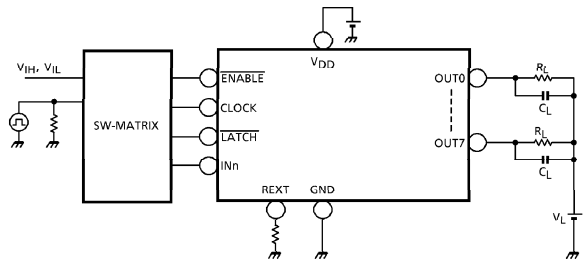
### Switching Characteristics:

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	INn-OUTn	tpLH	—	VDD = 5.0V VCE = 0.4V VIH = VDD VIL = GND REXT = 470Ω IOUT = 40mA VL = 3.0V RL = 65Ω CL = 10.5pF	—	600	1200	ns
	LATCH-OUTn				—	600	1200	ns
	ENABLE-OUTn				—	600	1200	ns
Propagation Delay Time ("H" to "L")	INn-OUTn	tpHL	—		—	300	1200	ns
	LATCH-OUTn				—	300	1200	ns
	ENABLE-OUTn				—	300	1200	ns
Pulse Width	/ENABLE	tw ENA	—		—	2000	3500	ns
	/LATCH	tw LAT	—		—	25	50	ns
	/IN	tw IN	—		—	2000	3500	ns
Set-up Time for Latch	L-H	tsetup LAT	—		—	25	50	ns
	H-L		—	—	25	50	ns	
Hold Time for LATCH & CLOCK	L-H	thold LAT	—	—	0	15	ns	
	H-L		—	—	0	15	ns	
Maximum CLOCK Rise Time		tr	—	—	—	10	μs	
Maximum CLOCK Fall Time		tf	—	—	—	10	μs	
Output Rise Time		tor	—	—	200	1000	1200	ns
Output Fall Time		tof	—	—	200	1000	1200	ns

### DC Characteristic Test Circuit:



### AC Characteristic Test Circuit:



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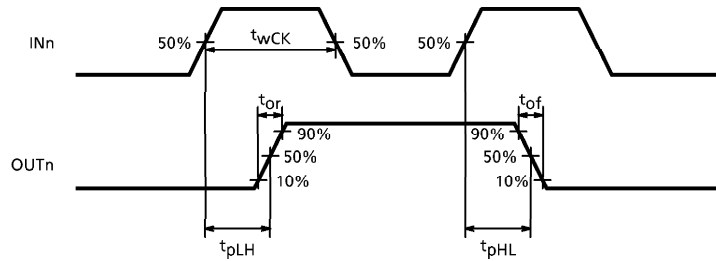


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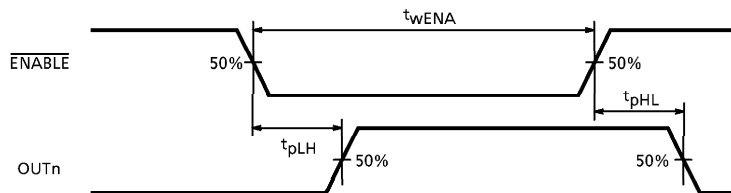
## TB62707F

Timing Wave Form:

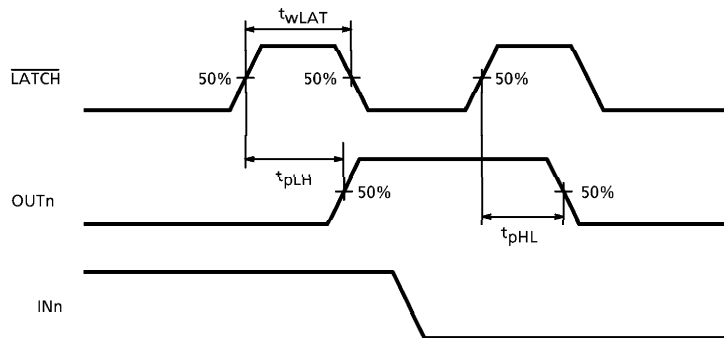
### 1. INn-OUTn



### 2. $\overline{\text{ENABLE}}$ -OUTn



### 3. $\overline{\text{LATCH}}$ -OUTn



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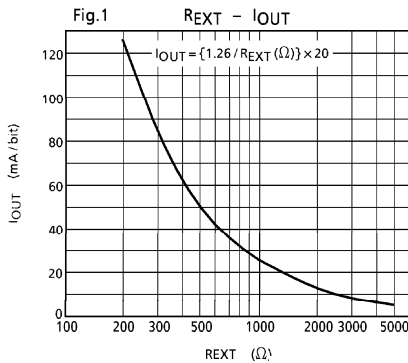
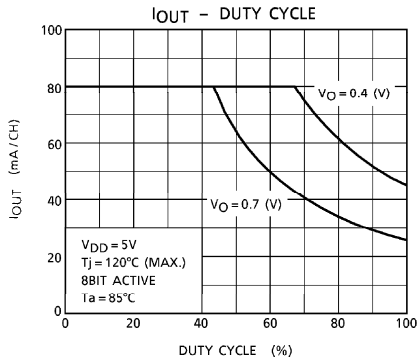
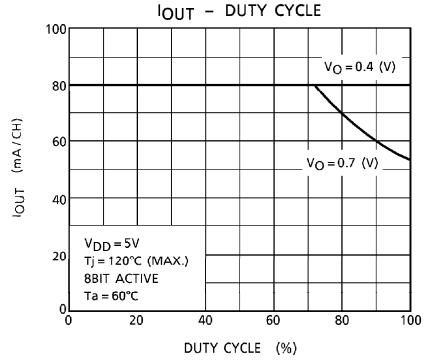
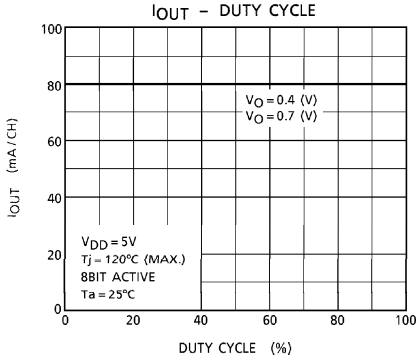
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Graphs:



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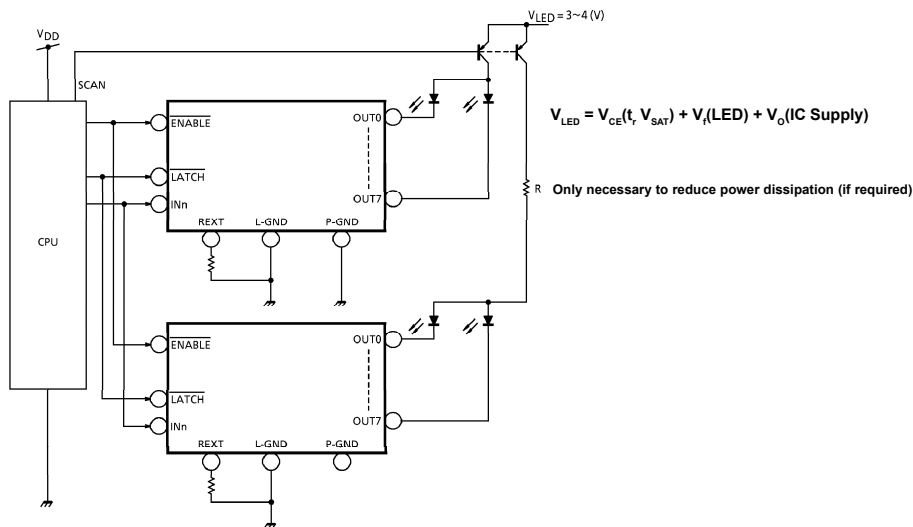




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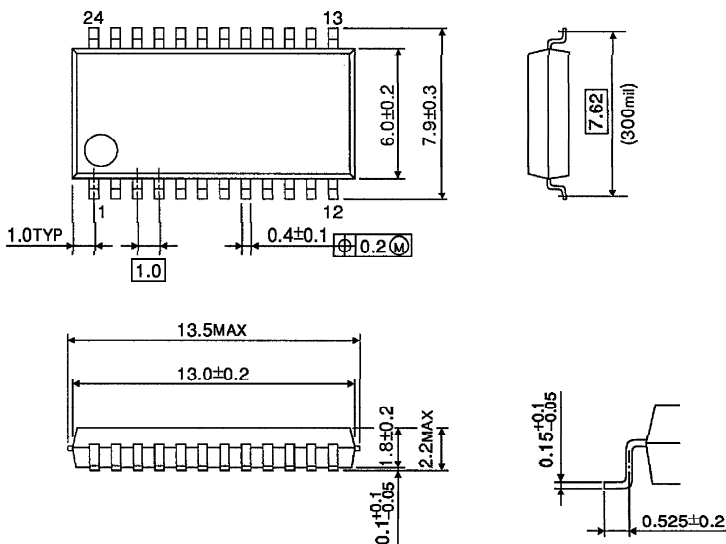
### Application Circuit:



### Outline Drawing:

SSOP24-P-300-1.00

Unit : mm



Weight : 0.32g (Typ.)

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