TEXAS INSTRUMENTS

PCI2050

PCI-to-PCI Bridge

Implementation Guide

August 2000

MSDS PCI

SCPU009

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1 Introduction

This document is provided to assist platform developers who are using the PCI2050 PCI-to-PCI bridge controller.

Chapter 2 is a list of the features of the PCI2050.

Chapter 3 is a listing of the device terminals, with corresponding signal names for each terminal.

Chapter 4 is the electrical guidelines. This chapter explains the pullup resistors and voltage level capacitors required for proper implementation of the PCI2050. The PCI specification requires all signals to be driven to a known level. This is accomplished with pullup resistors or by the PCI device. Some small capacitors are recommended on the power connections of the PCI2050. This is standard practice in board design to provide a stable supply voltage when large loads are placed on the system.

Chapter 5 describes a number of functional considerations in implementing a PCI2050 solution, including proper use of an external arbiter with the PCI2050, an explanation of how PCI interrupts and IDSEL mappings interrelate, how to implement PCI hot-swap with the PCI2050, implementing PCI power management, and an an explanation of the GPIO interface.

2 PCI2050 Feature Set

The PCI2050 provides the following features.

- Supports PCI Local Bus Specification Revision 2.2 and PCI-PCI Bridge Specification 1.1
- 3.3-V core logic with universal PCI interfaces compatible with 3.3-V and 5.0-V PCI signaling environments
- Supports two 32-bit, 33-MHz PCI buses
- Provides internal arbitration for up to nine external secondary bus masters with programmable control
- Provides ten secondary PCI bus clock outputs
- Supports sustained pass-through bandwidth of 132 MBps
- Packaged in high technology 208-terminal LQFP or 209-terminal MicroStar BGA™ package
- Support for PCI clock run on both buses
- External arbiter option
- Support for bus locking
- Support for CompactPCI™ hot-swap
- Independent read and write buffers for each direction
- Provides VGA/palette decoding options

3 Terminal Assignments

Table 3–1. 208-Pin LQFP Signal Names Sorted by Terminal Number

PDV NO.	GHK NO.	SIGNAL NAME	PDV NO.	GHK NO.	SIGNAL NAME	PDV NO.	GHK NO.	SIGNAL NAME	PDV NO.	GHK NO.	SIGNAL NAME
1	D1	V_{CC}	44	P2	BPCCE	87	V12	P_LOCK	130	K17	TDO
2	E3	S_REQ1	45	N5	P_CLK	88	U12	P_PERR	131	K15	V_{CC}
3	F5	S_REQ2	46	P3	P_GNT	89	P12	P_SERR	132	K14	TMS
4	G6	S_REQ3	47	R1	P_REQ	90	R12	P_PAR	133	J19	TCLK
5	E2	S_REQ4	48	P6	GND	91	W13	V_{CC}	134	J18	TRST
6	E1	S_REQ5	49	R2	P_AD31	92	V13	P_C/BE1	135	J17	S_V_{CCP}
7	F3	S_REQ6	50	P5	P_AD30	93	U13	P_AD15	136	J14	GND
8	F2	S_REQ7	51	R3	V_{CC}	94	P13	GND	137	J15	S_AD0
9	G5	S_REQ8	52	T1	GND	95	W14	P_AD14	138	H19	S_AD1
10	F1	S_GNT0	53	W4	V_{CC}	96	V14	P_AD13	139	H18	V_{CC}
11	H6	S_GNT1	54	U5	GND	97	R13	V_{CC}	140	H17	S_AD2
12	G3	GND	55	R6	P_AD29	98	U14	P_AD12	141	H14	S_AD3
13	G2	S_GNT2	56	P7	V_{CC}	99	W15	P_AD11	142	H15	GND
14	G1	S_GNT3	57	V5	P_AD28	100	P14	GND	143	G19	S_AD4
15	H5	S_GNT4	58	W5	P_AD27	101	V15	P_AD10	144	G18	S_AD5
16	H3	S_GNT5	59	U6	GND	102	R14	NC	145	G17	V_{CC}
17	H2	S_GNT6	60	V6	P_AD26	103	U15	V_{CC}	146	G14	S_AD6
18	H1	S_GNT7	61	R7	P_AD25	104	W16	GND	147	F19	S_AD7
19	J1	S_GNT8	62	W6	V_{CC}	105	T19	V_{CC}	148	F18	GND
20	J2	GND	63	P8	P_AD24	106	R17	MS1	149	G15	S_C/BE0
21	J3	S_CLK	64	U7	P_C/BE3	107	P15	P_AD9	150	F17	S_AD8
22	J5	S_RST	65	V7	P_IDSEL	108	N14	V_{CC}	151	E19	V_{CC}
23	J6	S_CFN	66	W7	GND	109	R18	P_AD8	152	F14	S_AD9
24	K1	HSSWITCH/GPIO3	67	R8	P_AD23	110	R19	P_C/BE0	153	E18	S_M66ENA
25	K2	GPIO2	68	U8	P_AD22	111	P17	GND	154	F15	S_AD10
26	K3	V_{CC}	69	V8	V_{CC}	112	P18	P_AD7	155	E17	MS0
27	K5	GPIO1	70	W8	P_AD21	113	N15	P_AD6	156	D19	GND
28	K6	GPIO0	71	W9	P_AD20	114	P19	V_{CC}	157	A16	V_{CC}
29	L1	S_CLKOUT0	72	V9	GND	115	M14	P_AD5	158	C15	GND
30	L2	S_CLKOUT1	73	U9	P_AD19	116	N17	P_AD4	159	E14	S_AD11
31	L3	GND	74	R9	P_AD18	117	N18	GND	160	F13	GND
32	L6	S_CLKOUT2	75	P9	V_{CC}	118	N19	P_AD3	161	B15	S_AD12
33	L5	S_CLKOUT3	76	W10	P_AD17	119	M15	P_AD2	162	A15	S_AD13
34	M1	V_{CC}	77	V10	P_AD16	120	M17	V_{CC}	163	C14	V_{CC}
35	M2	S_CLKOUT4	78	U10	GND	121	M18	P_AD1	164	B14	S_AD14
36	M3	S_CLKOUT5	79	R10	P_C/BE2	122	M19	P_AD0	165	E13	S_AD15
37	M6	GND	80	P10	P_FRAME	123	L19	GND	166	A14	GND
38	M5	S_CLKOUT6	81	W11	V_{CC}	124	L18	P_V_{CCP}	167	F12	S_C/BE1
39	N1	S_CLKOUT7	82	V11	P_IRDY	125	L17	NC	168	C13	S_PAR
40	N2	V_{CC}	83	U11	P_TRDY	126	L15	MSK_IN	169	B13	S_SERR
41	N3	S_CLKOUT8	84	P11	P_DEVSEL	127	L14	HSENUM	170	A13	V_{CC}
42	N6	S_CLKOUT9	85	R11	P_STOP	128	K19	HSLED	171	E12	S_PERR
43	P1	P_RST	86	W12	GND	129	K18	TDI	172	C12	S_LOCK

Table 3–1. 208-Pin LQFP Signal Names Sorted by Terminal Number (continued)

PDV NO.	GHK NO.	SIGNAL NAME	PDV NO.	GHK NO.	SIGNAL NAME	PDV NO.	GHK NO.	SIGNAL NAME	PDV NO.	GHK NO.	SIGNAL NAME
173	B12	S_STOP	182	C10	S_AD16	191	B8	S_AD22	200	B6	S_AD27
174	A12	GND	183	E10	S_AD17	192	C8	S_AD23	201	E7	S_AD28
175	A11	S_DEVSEL	184	F10	V_{CC}	193	F8	GND	202	C6	V_{CC}
176	B11	S_TRDY	185	A9	S_AD18	194	E8	S_C/BE3	203	A5	S_AD29
177	C11	S_IRDY	186	B9	S_AD19	195	A7	S_AD24	204	F6	S_AD30
178	E11	V_{CC}	187	C9	GND	196	B7	V_{CC}	205	B5	GND
179	F11	S_FRAME	188	F9	S_AD20	197	C7	S_AD25	206	E6	S_AD31
180	A10	S_C/BE2	189	E9	S_AD21	198	F7	S_AD26	207	C5	S_REQ0
181	B10	GND	190	A8	V_{CC}	199	A6	GND	208	A4	V_{CC}

4 Electrical Guidelines

4.1 Pullup Resistors

This discussion on PCI pullup requirements is taken from the *PCI Local Bus Specification Rev 2.2*, and is provided for reference in designing in the PCI2050.

PCI control signals always require pullup resistors on the motherboard (NOT the expansion board) to ensure that they contain stable values when no agent is actively driving the bus. This includes, $\overline{\text{FRAME}}$, $\overline{\text{TRDY}}$, $\overline{\text{IRDY}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{STOP}}$, $\overline{\text{SERR}}$, $\overline{\text{PERR}}$, $\overline{\text{LOCK}}$, $\overline{\text{INTA}}$, $\overline{\text{INTB}}$, $\overline{\text{INTC}}$, $\overline{\text{INTD}}$, and when used, $\overline{\text{REQ64}}$, and $\overline{\text{ACK64}}$. The point-to-point and shared 32-bit signals do not require pullups; bus parking ensures their stability.

Table 4–1. Minimum and Typical PCI Pullup Resistor Values

SIGNALING RAIL	R_{MIN}	$R_{TYPICAL}$	R_{MAX}
5.0 V	963 Ω	2.7 kΩ at 10%	Dependent on number of loads. See equation 1.
3.3 V	2.42 kΩ	8.2 kΩ at 10%	Dependent on number of loads. See equation 1.

Equation to calculate R_{MAX}:

$$R_{MAX} = \left[V_{CC(MIN)} - V_X\right] \Big/ \left[\text{num\_loads} \times I_{IH}\right] \quad (1)$$

Where:

V_X = 2.7 V for 5.0-V signaling and V_X = 2.3 V for 3.3-V signaling.

In addition to those specified by PCI, the table below contains both PCI control signals and other PCI2050 specific signals which should have pullup (keeper) resistors. Texas Instruments also recommends, when possible, that the signals be pulled up to 3.3 V to reduce leakage current.

Table 4–2. PCI2050 Pullups

TERMINAL NAME	TERMINAL NO.		TERMINAL NAME	TERMINAL NO.		TERMINAL NAME	TERMINAL NO.	
	PDV	GHK		PDV	GHK		PDV	GHK
$\overline{\text{S\_DEVSEL}}$	175	A11	$\overline{\text{S\_REQ1}}$	2	E3	$\overline{\text{S\_REQ7}}$	8	F2
$\overline{\text{S\_FRAME}}$	179	F11	$\overline{\text{S\_REQ2}}$	3	F5	$\overline{\text{S\_REQ8}}$	9	G5
$\overline{\text{S\_IRDY}}$	177	C11	$\overline{\text{S\_REQ3}}$	4	G6	$\overline{\text{S\_RST}}$	22	J5
$\overline{\text{S\_LOCK}}$	172	C12	$\overline{\text{S\_REQ4}}$	5	E2	$\overline{\text{S\_SERR}}$	169	B13
$\overline{\text{S\_PERR}}$	171	E12	$\overline{\text{S\_REQ5}}$	6	E1	$\overline{\text{S\_STOP}}$	173	B12
$\overline{\text{S\_REQ0}}$	207	C5	$\overline{\text{S\_REQ6}}$	7	F3	$\overline{\text{S\_TRDY}}$	176	B11

The signals in Table 4–3 may need pullups. The designer should refer to the section related to the signal to determine if a pullup resistor is necessary.

Table 4–3. Optional Pullups

TERMINAL NAME	TERMINAL NO.		REFER TO SECTION ON	TERMINAL NAME	TERMINAL NO.		REFER TO SECTION ON
	PDV	GHK			PDV	GHK	
$\overline{\text{S\_CFN}}$	23	J6	External arbiter	GPIO2	25	K2	GPIO interface
$\overline{\text{HSENUM}}$	127	L14	cPCI hot swap	GPIO1	27	K5	GPIO interface
$\overline{\text{HS\_SWITCH}}$/GPIO3	24	K1	cPCI hot swap GPIO interface	GPIO0	28	K6	GPIO interface

The signals listed in Table 4–4 can be hardwired to GND or 3.3 V, if they are not going to be used in the design. Texas Instruments strongly recommends that all active-low signals listed in Table 4–4 be hardwired to 3.3 V. All other signals can be hardwired to GND or 3.3 V.

Table 4–4. Signals Which Could Be Hardwired to GND or 3.3 V

TERMINAL NAME	TERMINAL NO.		TERMINAL NAME	TERMINAL NO.		TERMINAL NAME	TERMINAL NO.	
	PDV	GHK		PDV	GHK		PDV	GHK
$\overline{\text{S\_CFN}}$	23	J6	$\overline{\text{S\_REQ4}}$	5	E2	$\overline{\text{HS\_SWITCH}}$/GPIO3	24	K1
$\overline{\text{S\_REQ0}}$	207	C5	$\overline{\text{S\_REQ5}}$	6	E1	GPIO1	27	K5
$\overline{\text{S\_REQ1}}$	2	E3	$\overline{\text{S\_REQ6}}$	7	F3	MSK_IN	126	L15
$\overline{\text{S\_REQ2}}$	3	F5	$\overline{\text{S\_REQ7}}$	8	F2			
$\overline{\text{S\_REQ3}}$	4	G6	$\overline{\text{S\_REQ8}}$	9	G5			

4.2 Power and Signal Levels

The PCI2050 supports both 3.3-V and 5.0-V signaling environments. This is accomplished by the P_VCCP and S_VCCP clamping rails. These two rails are not power rails. They only clamp the signals at the rail voltage (3.3 V or 5.0 V). All I/O buffers are powered by the V_{CC} rail. Because V_{CC} powers both the core and the I/O buffers, it must always be at 3.3 V. The table below depicts the signaling combinations supported by the PCI2050 and the P_VCCP and S_VCCP voltages needed to operate in these signaling environments.

Table 4–5. V_{CC} Combinations Based on Signaling Environment

PRIMARY BUS SIGNALING ENVIRONMENT [V]	SECONDARY BUS SIGNALING ENVIRONMENT [V]	P_VCCP [V]	S_VCC [V]	VCC [V]
5.0	5.0	5.0	5.0	3.3
5.0	3.3	5.0	3.3	3.3
3.3	5.0	3.3	5.0	3.3
3.3	3.3	3.3	3.3	3.3

Table 4–6 contains the power measurements for the PCI2050. The measurements were taken under the following conditions: 33-MHz PCI bus clock, V_{CC} = 3.3 V, P_VCCP = 5.0 V, and S_VCCP = 5.0 V.

Table 4–6. PCI2050 Power Measurements

DEVICE STATE	I_{VCC} (mA)	I_{P_VCCP} (μA)	I_{S_VCCP} (μA)
D0	55	500	500
D1	50	500	500
D2	15	500	$\overline{500}$
$D3_{Hot}$	15	500	500

4.3 Bypass Capacitors

Standard design rules for the supply bypass should be followed. Low-inductance ceramic-chip capacitors are best for bypass capacitors. A value of 0.1 μF is recommended for each of the power supply terminals V_{CC}, P_VCCP, and S_VCCP.

4.4 Secondary Clocks

The PCI2050 has ten secondary clocks based on the primary PCI clock. Each secondary clock can be enabled or disabled through the secondary clock control register located at PCI offset 68h. We suggest the configuration software or BIOS disable any clocks which are not in use to conserve power. When a secondary clock is disabled, the PCI2050 will drive the clock signal low, until the clock is reenabled. Texas Instruments also recommends the use of a 50-Ω series terminator resistor to be connected to each secondary clock to reduce reflections.

The primary clock and the secondary clocks have the following relationships:

- They all operate at the same frequency.
- The maximum clock frequency is 33 MHz.
- The skew between P_CLK and S_CLKOUT0–S_CLKOUT9 has a range of 2.72 ns at 0°C to 5.8 ns at 115°C.
- The skew between secondary clocks is less than 0.1 ns with similar loading.

To ensure that the skew between the S_CLK input and the clock inputs to the secondary devices is minimized, the trace length between S_CLKOUT9 and S_CLK should match the trace length of the other S_CLKOUT traces. If one or more of the S_CLKOUT terminals is being routed to a socket, then the clock trace lengths to the built-on devices should be 2.5 inches longer than the clock traces to the sockets.

5 Functional Considerations

5.1 External Arbiter

The PCI2050 allows an external arbiter to be used in place of the default internal arbiter. This function is controlled by $\overline{\text{S\_CFN}}$. In order to use an external arbiter with the PCI2050, $\overline{\text{S\_CFN}}$ must be pulled up with a 10-kΩ resistor or hardwired to 3.3 V. If an external arbiter is not going to be used (the PCI2050 internal arbiter will be used instead), then $\overline{\text{S\_CFN}}$ must be hardwired to GND.

When an external secondary bus arbiter is used, the PCI2050 internally reconfigures the $\overline{\text{S\_REQ0}}$ and $\overline{\text{S\_GNT0}}$ signals so that $\overline{\text{S\_REQ0}}$ becomes the secondary bus master grant for the bridge and the $\overline{\text{S\_GNT0}}$ becomes the secondary bus master request for the PCI2050. This is done because $\overline{\text{S\_REQ0}}$ is an input and can be used to provide the grant input to the bridge, and $\overline{\text{S\_GNT0}}$ is an output and can provide the request output from the bridge.

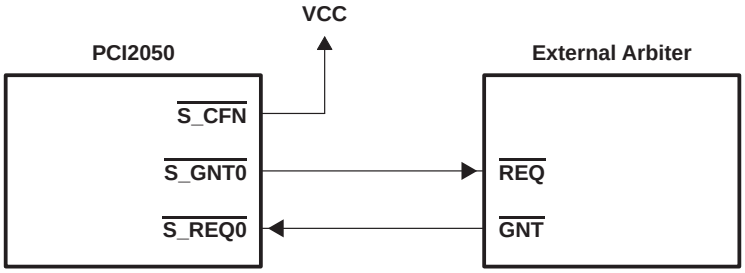

Figure 5–1. External Arbiter

When an external arbiter is used, all unused secondary bus grant outputs ($\overline{\text{S\_GNT8}}$–$\overline{\text{SGNT1}}$) are in a high-impedance state. Any unused secondary bus request lines ($\overline{\text{S\_REQ8}}$–$\overline{\text{S\_REQ1}}$) should be pulled high or hardwired to 3.3 V, to prevent the inputs from oscillating.

5.2 PCI Interrupts and IDSEL Mapping

The PCI2050 can support up to nine devices on the secondary side. Each device IDSEL should be connected to a secondary address line (S_AD31–S_AD16). In order to reduce capacitive load on the secondary address line, the connection can be made through a 1-kΩ series resistor.

Because the PCI2050 is a bridge device, all parallel PCI interrupts on the secondary interface must be routed as sideband signals to the PCI interrupts on the primary interface. When using multiple devices behind the PCI2050, a device ID and how the PCI interrupts are routed should be very important considerations in a design. Some operating systems like Windows 95™, expect a device PCI interrupt to be routed to a specific interrupt on the motherboard based on its ID number. For example, if a device ID is 4 and its PCI $\overline{\text{INTA}}$ is routed to PCI $\overline{\text{INTB}}$ on the motherboard, Windows 95™ will not configure the device properly. In order to reduce any chance of incompatibilities, we suggest the designer implement the interrupt routing scheme outlined in Section 2.2.6 of the *PCI Local Bus Specification Revision 2.2*. Table 5–1 summarizes Section 2.2.6.

Windows 95 is a trademark of Microsoft Corporation.

Table 5–1. Interrupt Routing

DEVICE NUMBER ON SECONDARY BUS	INTERRUPT TERMINAL ON DEVICE	INTERRUPT TERMINAL ON CONNECTOR
0, 4, 8, 16, 20, 24, 28	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$
1, 5, 9, 13, 17, 21, 25, 29	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$
2, 6, 10, 14, 18, 22, 26, 30	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTC}}$ $\overline{\text{INTD}}$ $\overline{\text{INTA}}$ $\overline{\text{INTB}}$
3, 7, 11, 15, 19, 23, 27, 31	$\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$ $\overline{\text{INTD}}$	$\overline{\text{INTD}}$ $\overline{\text{INTA}}$ $\overline{\text{INTB}}$ $\overline{\text{INTC}}$

5.3 Mode Selection

The PCI2050 can be programmed to operate in three separate modes: TI compact PCI mode, TI power management mode, and Intel™ 21150 compatible mode. Table 5–2 lists the mode-select-terminal logic values corresponding to each operating mode.

Table 5–2. Mode Select Terminals Definition

MS0	MS1	MODE
0	0	TI hot-swap
0	1	TI power management
1	X	Intel™ 21150 compatible

5.3.1 CompactPCI Hot-Swap Mode

In CompactPCI hot-swap mode, the PCI2050 $\overline{\text{HS\_SWITCH}}$/GPIO3 and $\overline{\text{HSENUM}}$ must be pulled up to ensure the proper functionality of the hot-swap logic.

5.4 PCI Power Management

When using the PCI2050 in a power managed environment, it is important to remember that $\overline{\text{PME}}$ and 3.3 $\underline{\text{Vaux}}$ are sideband signals as far as the bridge is concerned. If any devices on the secondary bus need $\overline{\text{PME}}$ or 3.3 Vaux, these signals must be routed around the bridge.

5.5 GPIO Interface

The PCI2050 GPIO terminals default to inputs, after reset, and should be pulled up to prevent oscillation if this interface is not going to be used.

Intel is a trademark of Intel Corporation.

5.5.1 Serial Clock Mask

GPIO0 and GPIO2 provides the control signals to two external 74F166 shift registers to shift in the serial clock mask. If the external shift registers are not used, MSK_IN can be tied low to enable all secondary clocks, or tied high to disable all secondary clocks.

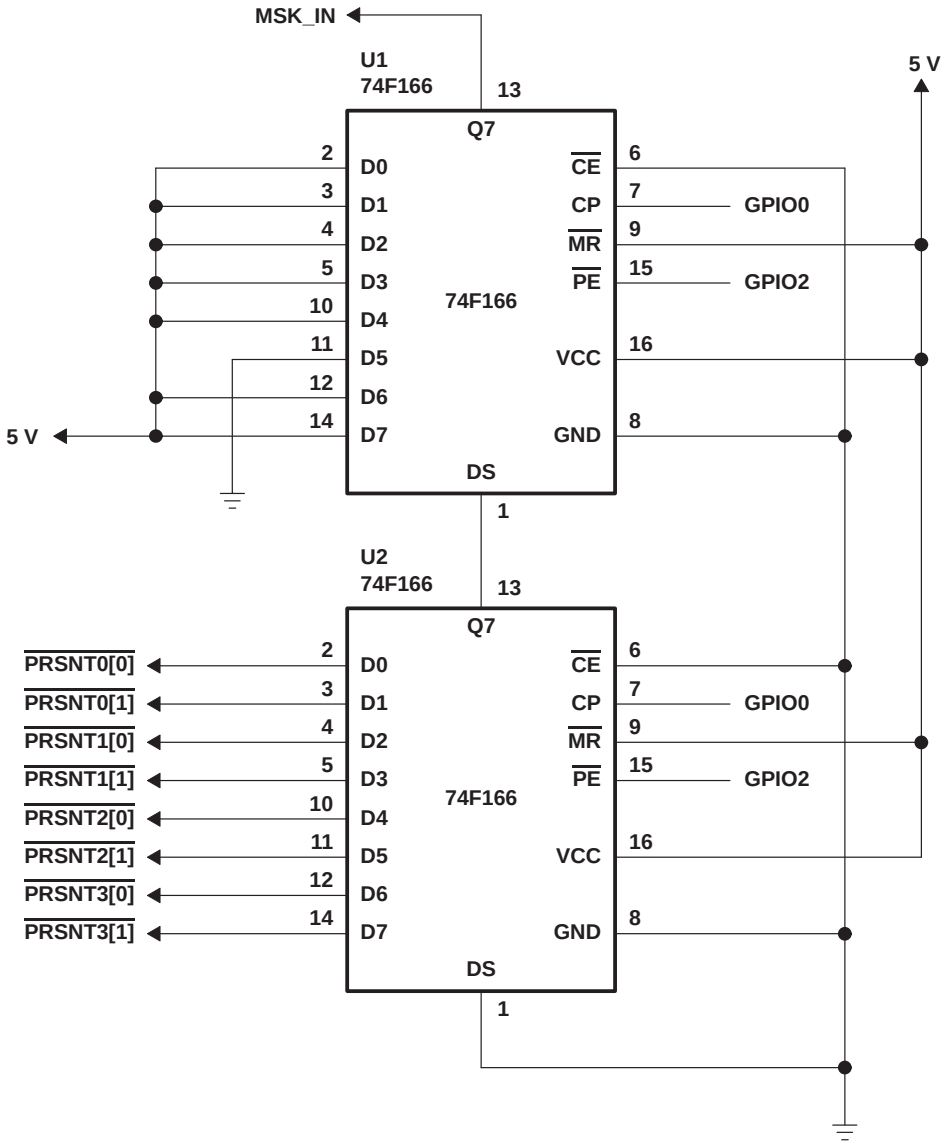

Figure 5–2. Serial Clock Mask Circuit

5.6 Sample Schematics

For sample schematics, see the *PCI2050 EVM Users Guide*, (TI Literature Number SCPU005).