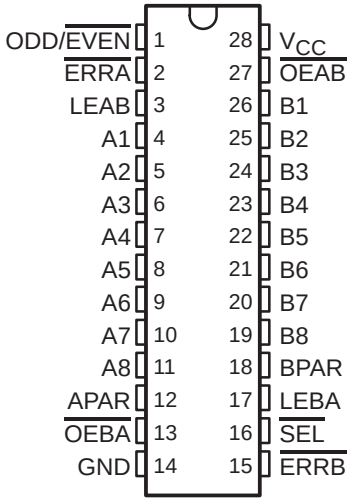
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Option to Select Generate Parity and Check or Feed-Through Data/Parity in A-to-B or B-to-A Directions**
- **Simultaneously Generates and Checks Parity**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



description

The SN74BCT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data buses in either direction. It has a current-sinking capability of 24 mA at the A bus and 64 mA at the B bus.

The SN74BCT899 features independent latch-enable (LEAB or $\overline{\text{LEBA}}$) inputs, a select ($\overline{\text{SEL}}$) input for ODD/$\overline{\text{EVEN}}$ parity, and separate error-signal ($\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$) outputs for checking parity.

The SN74BCT899 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

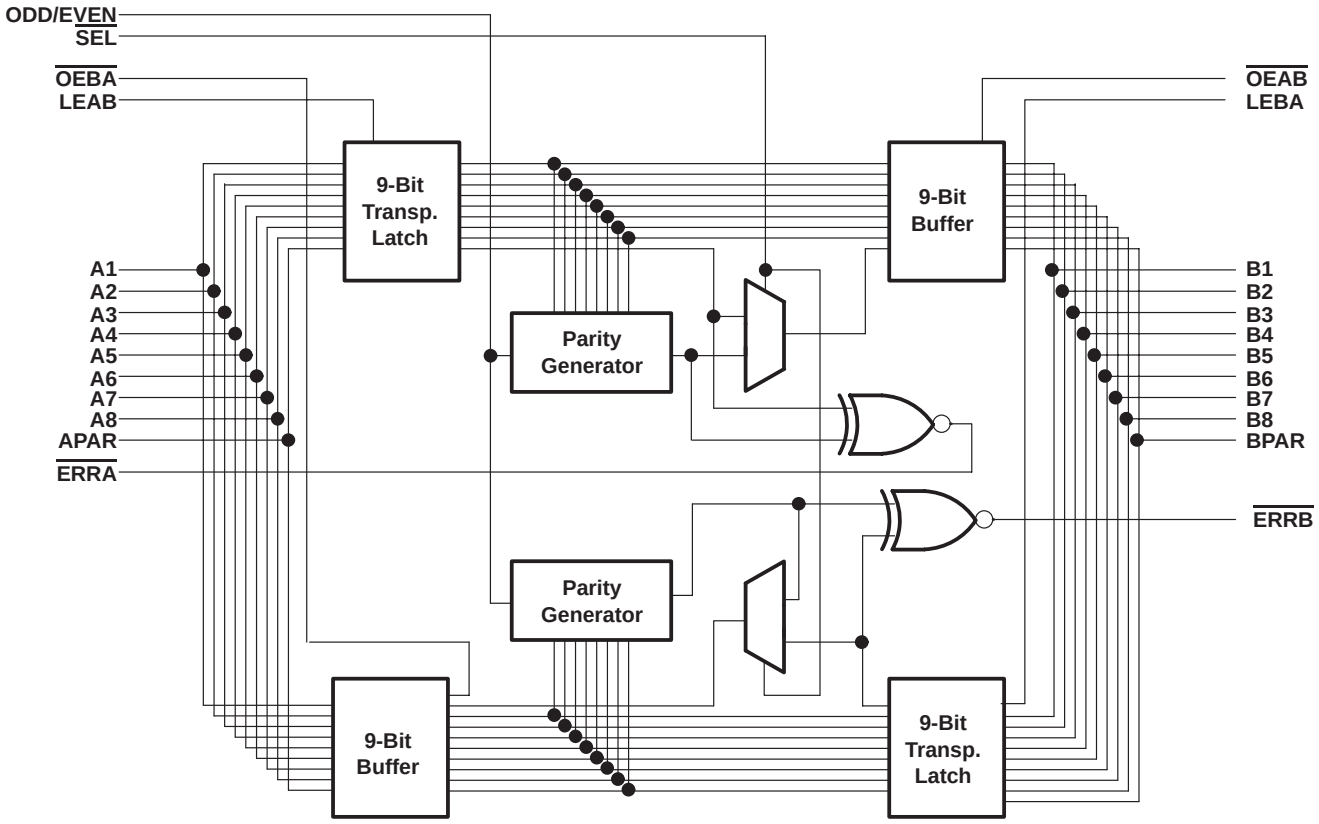
INPUTS					OPERATION OR FUNCTION
$\overline{OEAB}$	$\overline{OEBA}$	$\overline{SEL}$	LEAB	LEBA	
H	H	X	X	X	Buses A and B are in the high-impedance state.
H	L	L	X	H	Generates parity from B1 – B8 based on ODD/$\overline{EVEN}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	L	H	H	Generates parity from B1 – B8 based on ODD/$\overline{EVEN}$. Generated parity → APAR. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
H	L	L	X	L	Generates parity from B-latch data based on ODD/$\overline{EVEN}$. Generated parity → APAR. Generated parity checked against latched BPAR and output as $\overline{ERRB}$.
H	L	H	X	H	BPAR /B1 – B8 → APAR/A1 – A8 feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$.
H	L	H	H	H	BPAR /B1 – B8 → APAR/A1 – A8 feed-through mode. Generated parity checked against BPAR and output as $\overline{ERRB}$. Generated parity also fed back through the A latch for generate/check as $\overline{ERRA}$.
L	H	L	H	X	Generates parity from A1 – A8 based on ODD/$\overline{EVEN}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	L	H	H	Generates parity from A1 – A8 based on ODD/$\overline{EVEN}$. Generated parity → BPAR. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.
L	H	L	L	X	Generates parity from A-latch data based on ODD/$\overline{EVEN}$. Generated parity → BPAR. Generated parity checked against latched APAR and output as $\overline{ERRA}$.
L	H	H	H	X	APAR /A1 – A8 → BPAR/B1–B8 feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$.
L	H	H	H	X	APAR /A1 – A8 → BPAR/B1–B8 feed-through mode. Generated parity checked against APAR and output as $\overline{ERRA}$. Generated parity also fed back through the B latch for generate/check as $\overline{ERRB}$.
L	L	X	X	X	Output to A bus and B bus

PARITY FUNCTION TABLE

INPUTS†			OUTPUTS	
ODD/$\overline{EVEN}$	Σ OF INPUTS A1 – A8 = H	APAR	BPAR‡	$\overline{ERRA}$
L	0, 2, 4, 6, 8	L	L	H
L	1, 3, 5, 7	L	H	L
L	0, 2, 4, 6, 8	H	L	L
L	1, 3, 5, 7	H	H	H
H	0, 2, 4, 6, 8	L	H	L
H	1, 3, 5, 7	L	L	H
H	0, 2, 4, 6, 8	H	H	H
H	1, 3, 5, 7	H	L	L

† If LE = H, current A1 – A8 and APAR data is used. If LE = L, latched A1–A8 and APAR data is used.
‡ This is the value of BPAR if $\overline{SEL}$ = L. If $\overline{SEL}$ = H, BPAR = APAR.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O . . . . . 128 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	A1–A8			–3	mA
		B1–B8			–15	
I_{OL}	Low-level output current	A1–A8			24	mA
		B1–B8			64	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
T_A	Operating free-air temperature		0		70	°C

NOTE 2: Unused or floating pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}			V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	A1–A8, APAR, $\overline{ERRA}$, $\overline{ERRB}$		V_{CC} = 4.75 V,	I_{OH} = –1 mA	2.7	3.4		V
			V_{CC} = 4.5 V	I_{OH} = –1 mA	2.5	3.4		
				I_{OH} = –3 mA	2.4	3.3		
	B1–B8, BPAR		V_{CC} = 4.75 V,	I_{OH} = –3 mA	2.7	3.4		
			V_{CC} = 4.5 V	I_{OH} = –3 mA	2.4	3.4		
				I_{OH} = –12 mA				
				I_{OH} = –15 mA	2	3.1		
V_{OL}	A1–A8, APAR, $\overline{ERRA}$, $\overline{ERRB}$		V_{CC} = 4.5 V	I_{OL} = 20 mA				V
				I_{OL} = 24 mA		0.35	0.5	
	B1–B8, BPAR			I_{OL} = 48 mA				
				I_{OL} = 64 mA		0.42	0.55	
I_I‡			V_{CC} = 5.5 V,	V_I = 5.5 V			100	µA
I_{IH}‡			V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}‡			V_{CC} = 5.5 V,	V_I = 0.5 V			–20	µA
I_{OS}§	A1–A8, APAR, $\overline{ERRA}$, $\overline{ERRB}$		V_{CC} = 5.5 V,	V_O = 0	–60		–150	mA
	B1–B8, BPAR				–100		–225	
I_{CC}	Outputs high	A to B	V_{CC} = 5.5 V,	Outputs open		0.5	2	mA
		B to A				0.5	2	
	Outputs low	A to B				43	69	
		B to A				22	34	
	Outputs disabled, $\overline{ERR}$ outputs low	A to B				6	10	
		B to A				6	10	
	Outputs disabled, $\overline{ERR}$ outputs high	A to B				0.5	2	
		B to A				0.5	2	
C_i			V_{CC} = 5 V,	V_I = 0.5 V		6.5		pF
C_{io}	A ports		V_{CC} = 5 V,	V_O = 0.5 V		10.5		pF
	B ports					12.5		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration		5		5		ns
t_{su}	Setup time before LE↓	Data high or low	4.5		4.5		ns
t_h	Hold time after LE↓	Data high or low	1.5		1.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	1.9	6	7.6	1.9	9.1	ns
t_{PHL}			1.8	5.2	6.8	1.8	8.1	
t_{PLH}	A or B	BPAR or APAR	4.3	11	13	4.3	16.1	ns
t_{PHL}			4.5	10.7	12.7	4.5	15.3	
t_{PLH}	APAR or BPAR	BPAR or APAR	2.2	5.2	6.7	2.2	8	ns
t_{PHL}			1.7	4.7	6.3	1.7	7.6	
t_{PLH}	A, APAR, or B, BPAR	$\overline{ERRA}$ or $\overline{ERRB}$	3.4	10.6	12.6	3.4	15.7	ns
t_{PHL}			3.6	10.5	12.5	3.6	15.3	
t_{PLH}	ODD/$\overline{EVEN}$	$\overline{ERRA}$ or $\overline{ERRB}$	4.6	8.8	10.5	4.6	12.8	ns
t_{PHL}			4.1	8.4	10.2	4.1	12.8	
t_{PLH}	ODD/$\overline{EVEN}$	BPAR or APAR	4.5	9	10.7	4.5	13.1	ns
t_{PHL}			4.4	8.5	10.7	4.4	13.3	
t_{PLH}	$\overline{SEL}$	BPAR or APAR	1.4	4.6	6.2	1.4	7.7	ns
t_{PHL}			1.6	4.4	5.9	1.6	7.1	
t_{PLH}	LEAB OR LEBA	B or A	2.6	7.6	9.3	2.6	10.9	ns
t_{PHL}			3.3	6.5	8.2	3.3	9.3	
t_{PLH}	LEAB OR LEBA	BPAR or APAR (parity feed-through)	3	6.7	8.3	3	9.9	ns
t_{PHL}			3	6.1	7.7	3	8.7	
t_{PLH}	LEAB OR LEBA	BPAR or APAR (parity generated)	5.2	10.2	12.1	5.2	14.8	ns
t_{PHL}			5.1	8.9	10.7	5.1	12.5	
t_{PLH}	LEAB OR LEBA	$\overline{ERRB}$ or $\overline{ERRA}$	5.3	10.3	12.3	5.3	14.9	ns
t_{PHL}			5	9.2	11	5	12.9	
t_{PZH}	OEAB or OEBA	B or A	1.8	5.6	7.2	1.8	9	ns
t_{PZL}			2.1	10.5	12.2	2.1	13.9	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2.9	6.4	8.1	2.9	9.8	ns
t_{PLZ}			2.1	5.5	7.1	2.1	8.1	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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