TENTATIVE

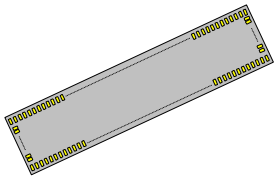
160COMMON x 128RGB LCD DRIVER FOR 65,536-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6855** is a 160COMMONx128RGB LCD driver for 65,536-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 327,680-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 64 or 32 grayscales from a built-in grayscale palette, and the LSI achieves 65,536 colors (64x32x32).

In addition, the **NJU6855** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE

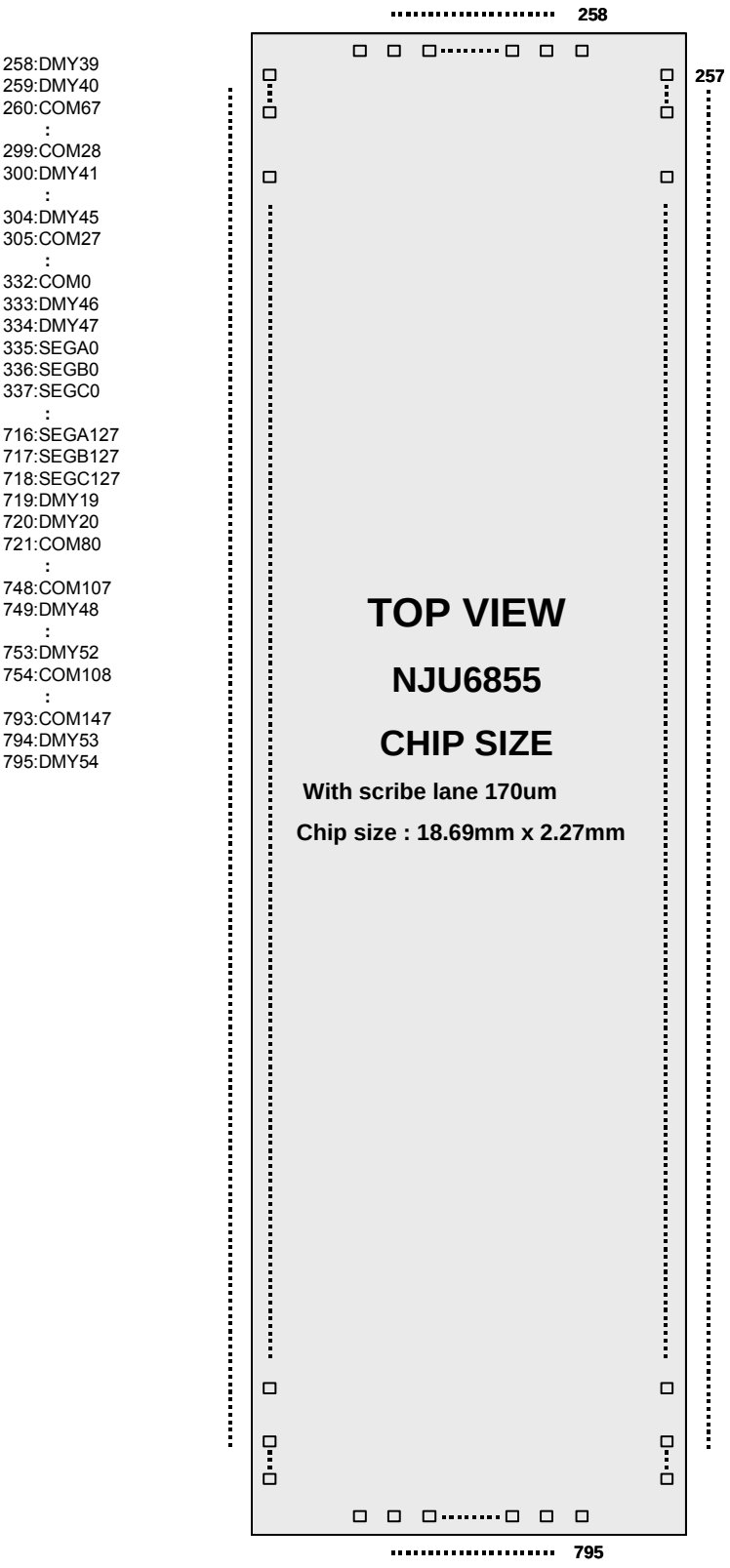


BUMP CHIP

■ FEATURES

- 65,536-color STN LCD driver
- Built-in LCD Drivers : 160-common x 128RGB (384-segment drivers)
- Built-in Display Data RAM (DDRAM) : 327,680 bits for Graphic Display
- Programmable Display Mode
  - 64 grayscales(Green)
  - 32 grayscales(Red, Blue)
- 2 Areas Partial Display
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 7 times
- Programmable Contrast Control : 256-step Electronic Volume Register (EVR)
- Various Useful Instructions
- Low Operating Current
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip

■ PAD LOCATION



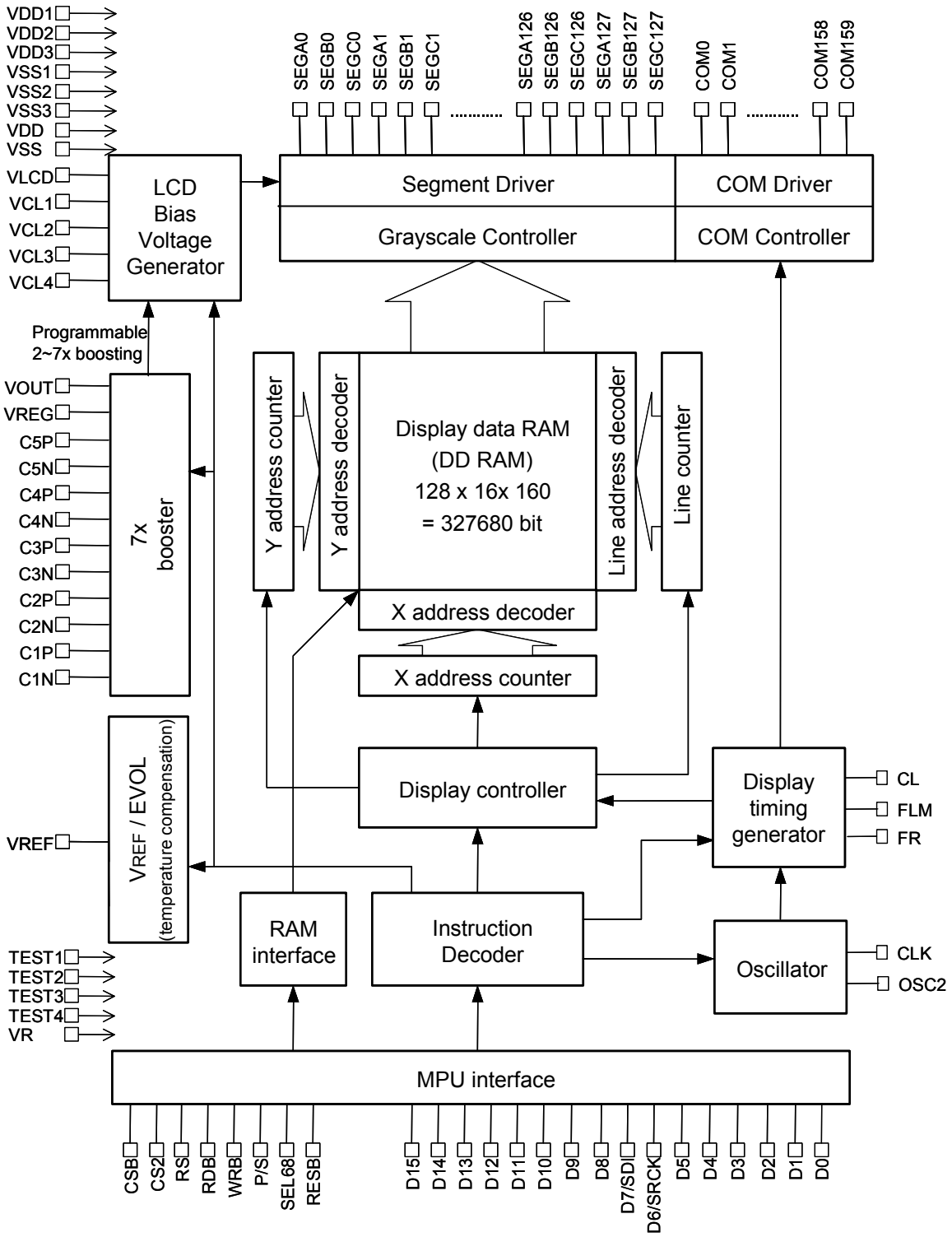
258:DMY39
259:DMY40
260:COM67
:
299:COM28
300:DMY41
:
304:DMY45
305:COM27
:
332:COM0
333:DMY46
334:DMY47
335:SEGA0
336:SEGB0
337:SEGC0
:
716:SEGA127
717:SEGB127
718:SEGC127
719:DMY19
720:DMY20
721:COM80
:
748:COM107
749:DMY48
:
753:DMY52
754:COM108
:
793:COM147
794:DMY53
795:DMY54

1:DMY1
2:DMY2
3:DMY3
4:COM148
:
15:COM159
16:DMY(ATRIM0)
:
30:DMY16
31:TEST1
32:TEST2
33:TEST3
34:TEST3
35:TEST4
36:TEST4
37:VREF
38:VREF
39:OSC2
40:OSC2
41:CLK
42:CLK
43:RESB
44:RESB
45:CS2
46:CS2
47:VDD
48:VDD
49:CSB
50:CSB
51:VSS
52:VSS
53:RS
54:RS
55:P/S
56:P/S
57:VDD
58:VDD
59:VSS
60:VSS
61:SEL68
62:SEL68
63:WRB
64:WRB
65:RDB
66:RDB
67:D0
68:D0
69:D1
70:D1
71:D2
72:D2
73:D3
74:D3
75:D4
76:D4
77:D5
78:D5
79:D6
80:D6
81:D7
82:D7
83:D8
84:D8
85:D9
86:D9
87:D10
88:D10
89:D11
90:D11
91:D12
92:D12
93:D13
94:D13
95:D14
96:D14

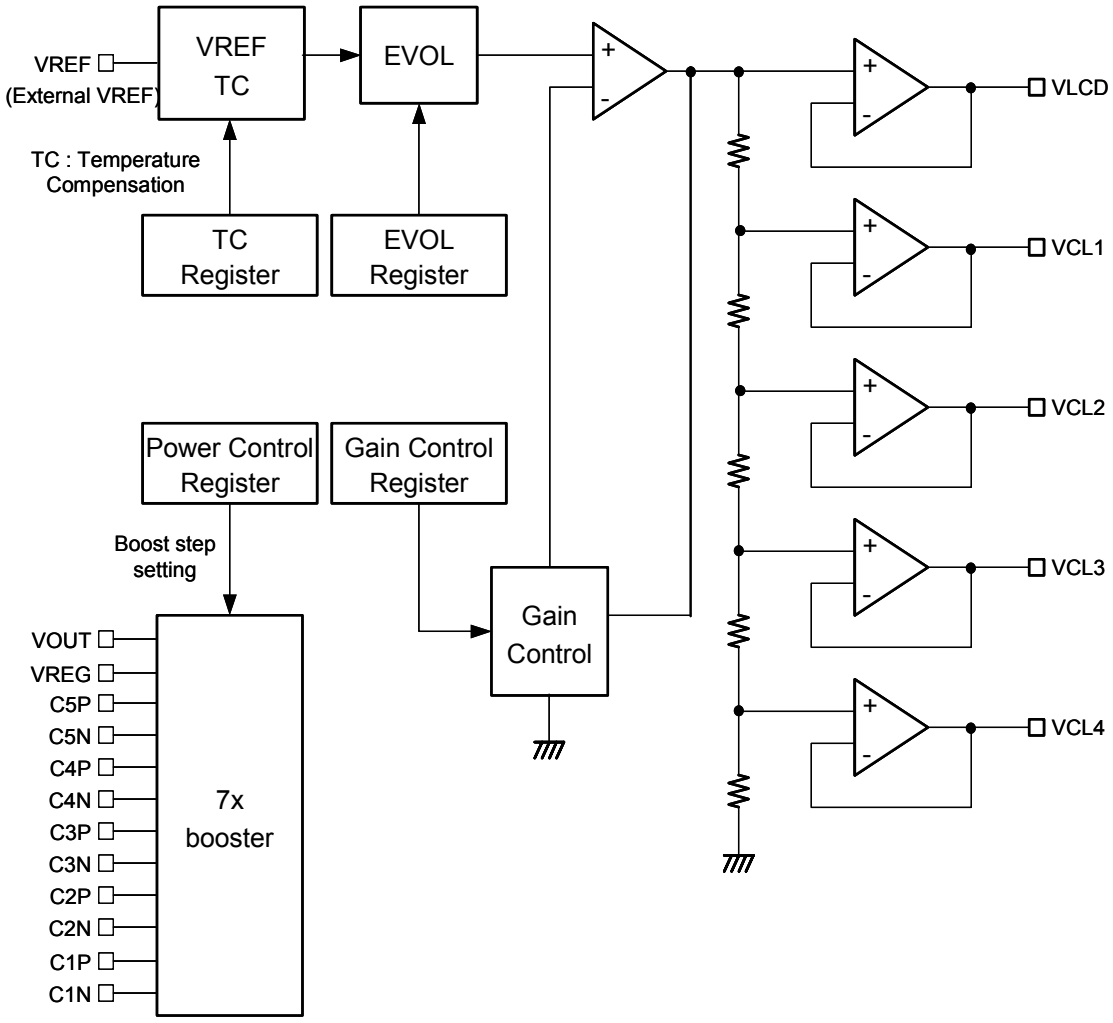
97:D15
98:D15
99:CL
100:CL
101:FLM
102:FLM
103:FR
104:FR
105:VDD1
:
110:VDD1
111:VSS1
:
116:VSS1
117:VDD2
:
122:VDD2
123:VSS2
:
128:VSS2
129:VR
130:VR
131:VLCD
:
135:VLCD
136:VCL1
:
140:VCL1
141:VCL2
:
145:VCL2
146:VCL3
:
150:VCL3
151:VCL4
:
155:VCL4
156:VDD3
:
161:VDD3
162:VSS3
:
167:VSS3
168:VOUT
:
172:VOUT
173:C5P
:
177:C5P
178:C5N
:
182:C5N
183:C4P
:
187:C4P
188:C4N
:
192:C4N
193:C3P
:
197:C3P
198:C3N
:
202:C3N
203:VREG
:
207:VREG
208:C2P
:
212:C2P
213:C2N
:
217:C2N
218:C1P
:

222:C1P
223:C1N
:
227:C1N
228:DMY21
:
242:DMY35
243:COM79
:
254:COM68
255:DMY36
:
257:DMY38

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

Power Supply

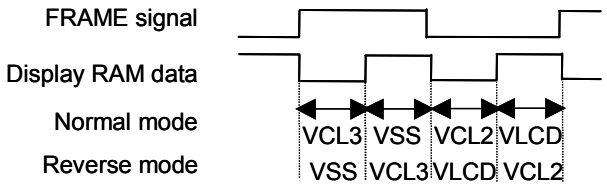
No.	Terminal	I/O	Description
105-110	V_{DD1}	Power	Power Supply for Logic Circuit
117-122	V_{DD2}	Power	Power Supply for Analog Circuit
156-161	V_{DD3}	Power	Power Supply for Voltage Booster
47-48 57-58	V_{DD}	Power	Power Supply for Logic Circuit(Internally connected to VDD1) External power supply is not allowed
51-52 59-60	V_{SS}	Power	GND for Logic Circuit (internally connected to VSS1) External power supply is not allowed.
111-116	V_{SS1}	Power	GND for Logic Circuit
123-128	V_{ss2}	Power	GND for Analog Circuit
162-167	V_{SS3}	Power	GND for Voltage Booster(or high voltage)
131-135 136-140 141-145 146-150 151-155	VLCD VCL1 ~VCL4	Power/O	LCD Bias Voltage When the internal LCD power supply is used, LCD bias voltages (VLCD and VCL1~VCL4) are generated by the built-in Voltage Booster, and capacitors must be connected between these pins and GND for stabilizing. When the external LCD power supply is used, LCD bias voltages must maintain the following shown relationship: VSS < VCL4 < VCL3 < VCL2 < VCL1 < VLCD
218-222 223-227	C1P, C1N	O	Capacitor Connection for Voltage Booster
208-212 213-217	C2P, C2N	O	Capacitor Connection for Voltage Booster
193-197 198-202	C3P, C3N	O	Capacitor Connection for Voltage Booster
183-187 188-192	C4P, C4N	O	Capacitor Connection for Voltage Booster
173-177 178-182	C5P, C5N	O	Capacitor Connection for Voltage Booster
168-172	VOUT	Power/O	High Voltage Power Supply(from external power) Internal Voltage Booster output (2x~7x boosting)
203-207	V_{REG}	Power/O	High Voltage Power Supply(from external power) Internal Voltage Booster output(2x boosting)
37-38	V_{REF}	I	External Reference Voltage Input Pin When TSEL<2:0> is “101” or “110” or “111”, external reference voltage is used. Set to “L” or “H” when not used.

MPU Interface

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Description</th></tr>
<tr><td>79-80
81-82
67-78</td><td>D6/SRCK
D7/SDI
D0-D5</td><td>I/O
I/O
I/O</td><td>Parallel Interface
D_7 to D_0: 8-bit Bi-directional Bus(P/S="H")

Serial Interface
SDI: Serial Data Input
SRCK: Shift Clock</td></tr>
<tr><td>83-98</td><td>D8-D15</td><td>I/O</td><td>8-bit Bidirectional Bus
In the 16-bit data bus mode, D15~D8 assigned to upper 8-bit data.
In the serial interface mode or 8-bit parallel interface mode, D15-D8 should be fixed to "H" or "L".</td></tr>
<tr><td>49-50
45-46</td><td>CSB, CS2</td><td>I</td><td>Chip Select
Active "L"</td></tr>
<tr><td>53-54</td><td>RS</td><td>I</td><td>Register Select
Interprets transferred data as display data or instruction
<table>
<tr><th>RS</th><th>H</th><th>L</th></tr>
<tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr>
</table></td></tr>
<tr><td>65-66</td><td>RDB(E)</td><td>I</td><td>80-series MPU Interface (P/S="H", SEL68="L")
Data Read (RDb) Signal: Active "L"
68-series MPU Interface (P/S="H", SEL68="H")
Enable Signal: Active "H"</td></tr>
<tr><td>63-64</td><td>WRB(R/WB)</td><td>I</td><td>80-series MPU Interface (P/S="H", SEL68="L")
Data Write (WRb) Signal: Active "L"
68-series MPU Interface (P/S="H", SEL68="H")
Data Read or Write (R/W) Signal
<table>
<tr><th>R/W</th><th>H</th><th>L</th></tr>
<tr><td>Status</td><td>Read</td><td>Write</td></tr>
</table></td></tr>
<tr><td>61-62</td><td>SEL68</td><td>I</td><td>MPU Mode Select
<table>
<tr><th>SEL86</th><th>H</th><th>L</th></tr>
<tr><td>MPU</td><td>68-series</td><td>80-series</td></tr>
</table></td></tr>
<tr><td>55-56</td><td>P/S</td><td>I</td><td>Parallel/Serial Interface Mode Select
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D_0 ~ D_7</td><td>RDB, WRB</td><td>-</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDI (D_7)</td><td>Write Only</td><td>SRCK (D_6)</td></tr>
</table>
In the serial interface mode (P/S="L"), RDB, WRB, D_0-D_5 and D_8-D_{15} should be fixed to "H" or "L",.</td></tr>
<tr><td>43-44</td><td>RESB</td><td>I</td><td>Reset</td></tr>
<tr><td>31</td><td>TEST1</td><td>I</td><td>Test(Only for maker use)
Keep open</td></tr>
<tr><td>32</td><td>TEST2</td><td>O</td><td>Test(Only for maker use)
Keep open</td></tr>
<tr><td>33-34</td><td>TEST3</td><td>I</td><td>Test(Only for maker use)
Keep open</td></tr>
<tr><td>35-36</td><td>TEST4</td><td>O</td><td>Test(Only for maker use)
Keep open</td></tr>
<tr><td>129-130</td><td>VR</td><td>I</td><td>Test(Only for maker use)
Keep open</td></tr>
</table>

LCD Output

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Description</th></tr>
<tr><td>335-718</td><td>$SEGA_0$~
$SEGA_{127}$,
$SEGB_0$~
$SEGB_{127}$,
$SEGC_0$~
$SEGC_{127}$</td><td>O</td><td>Segment Drivers Output
<table>
<tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr>
<tr><td>Normal</td><td>0</td><td>1</td></tr>
<tr><td>Reverse</td><td>1</td><td>0</td></tr>
</table>

</td></tr>
<tr><td>99-100</td><td>CL</td><td>O</td><td>Normally open.</td></tr>
<tr><td>101-102</td><td>FLM</td><td>O</td><td>Normally open.</td></tr>
<tr><td>103-104</td><td>FR</td><td>O</td><td>Normally open.</td></tr>
<tr><td>4-15
243-254
260-299
305-332
721-748
754-793</td><td>COM_0~
COM_{159}</td><td>O</td><td>Common Divers Output
<table>
<tr><th>Data</th><th>FR</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VLCD</td></tr>
<tr><td>L</td><td>H</td><td>VCL4</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td></tr>
<tr><td>L</td><td>L</td><td>VCL1</td></tr>
</table></td></tr>
<tr><td>41-42</td><td>CLK</td><td>I</td><td>External Reference Clock Input
Fix to “L” or “H” when not used</td></tr>
<tr><td>39-40</td><td>OSC2</td><td>O</td><td>Display Timing Clock Output
Internal oscillator wave will be output when MCKSEL is “H”.</td></tr>
</table>

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD1}	V_{SS1}= V_{SS2}= V_{SS3}=0V Ta = +25°C	V_{DD1}	-0.3 to +4.0	V
Supply Voltage (2)	V_{DD2}		V_{DD2}	-0.3 to +4.0	V
Supply Voltage (3)	V_{DD3}		V_{DD3}	-0.3 to +4.0	V
Supply Voltage (4)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +20.0	V
Supply Voltage (6)	VCL1~VCL4		VCL1~VCL4	-0.3 to V_{LCD} + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD1} + 0.3	V
Storage Temperature	T_{stg}			-45 to +125	°C

*1 D0 ~ D15, CSB, CS2, RS, WRB, RDB, CLK, RESB, TEST1~4 terminals
*2 To stabilize the LSI operation, place decoupling capacitors between VDD1 and VSS1, VDD2 and VSS2, VDD3 and VSS3.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD1}	1.7		3.3	V	
	V_{DD2}	V_{DD2}	2.4		3.3	V	
	V_{DD3}	V_{DD3}	2.4		3.3	V	*1
Operating Voltage	V_{OUT}	V_{OUT}	5		18.0	V	*2
	V_{LCD}	V_{LCD}	5		18.0	V	
	V_{REG}	V_{REG}	4.8		6.6	V	
	V_{REF}	V_{REF}	1.0	1.2	1.3	V	*3
Operating Temperature	T_{opr}		-30		85	°C	

*1. When the Voltage booster is used, V_{DD3} should be used within the limit range, and V_{DD2} can be connected to V_{DD3}.
*2. Please keep the relationship as following shown, $V_{OUT} \geq V_{LCD} > VCL1 > VCL2 > VCL3 > VCL4 > V_{SS}$, $V_{OUT} \geq V_{REG} \geq VCL2$, when the internal boosting circuit is not used.
*3. When the internal reference voltage circuit is used, reference voltage V_{REF} should be used within the limit range.

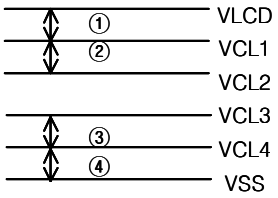
■ DC CHARACTERISTICS

V_{SS} = 0V, V_{DD1}=+1.7 to +3.3V, V_{DD2}=+2.4 to +3.3V, Ta=-30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD1}		V_{DD1}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD1}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD1} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD1} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	IL_I	V_I = V_{SS1} or V_{DD1}			TBD		µA	*4
Output leakage current	IL_O	V_I = V_{SS1} or V_{DD1}			TBD		µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_{LCD} = 10V		1	2	kΩ	*6
			V_{LCD} = 6V		2	4		
Stand-by current	I_{STB}	CSB=V_{DD1}, Ta=25°C	V_{DD1} = 3V		TBD		µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD2} = 3V Ta = 25°C		1572	1850	2127	kHz	*8
	f_{OSC2}			1045	1230	1414		*9
	f_{OSC3}			850	1000	1150		*10
	f_{OSC4}			671.5	790	908.5		*11
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 7)		(N x V_{DD3}) x 0.95			V	*12
Supply current (1)	I_{DD1}	V_{DD3} =2.5V, 7-time booster All ON pattern			TBD		µA	*13
Supply current (2)	I_{DD2}	V_{DD3} =2.5V, 7-time booster Checker pattern			TBD			
Supply current (3)	I_{DD3}	V_{DD3} =3V, 6-time booster All ON pattern			TBD			
Supply current (4)	I_{DD4}	V_{DD3} =3V, 6-time booster Checker pattern			TBD			
Supply current (5)	I_{DD5}	V_{DD3} =3V, 5-time booster All ON pattern			TBD			
Supply current (6)	I_{DD6}	V_{DD3} =3V, 5-time booster Checker pattern			TBD			
Supply current (7)	I_{DD7}	V_{DD3} =3V, 4-time booster All ON pattern			TBD			
Supply current (8)	I_{DD8}	V_{DD3} =3V, 4-time booster Checker pattern			TBD			
Output Voltage	VCL2			-100	0	+100	mV	*14
	VCL3			-100	0	+100		
	VD12			-100	0	+30		
	VD34			-30	0	+30		
	VD24			-30	0	+30		

Applied Terminals (* remark solves)

*1. D0~D15, CSB, RS, RDB, WRB, P/S, SEL68, RESB terminals
*2. D0~D15 terminals
*3. OSC2 terminals
*4. CSB, RS, SEL68, RDB, WRB, P/S, RES, CLK terminals
*5. Applicable at D0~D15 = high impedance state
*6. SEGA0~SEGA127, SEGB0~SEGB127, SEGC0~SEGC127, COM0~COM159 terminals
Resistance when being supplied 0.5V between each output terminals and power terminal (VLCD, VCL1, VCL2, VCL3, and VCL4).
Applicable under bias ratio = 1/9
*7. VDD1 terminal
VDD1 current when source clock is stopped, chip selection (CSB=VDD1) is non- selection state and no load.
*8. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = “00000000”.
*9. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = “01000000”.
*10. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = “10000000”.
*11. Oscillator frequency when internal oscillator circuit is used.
Applicable under MCLK register of oscillator circuit, {MCLK<7:0>} = “11000000”.
*12. VOUT terminal
N x boosting (N=2~7), applicable under internal oscillator circuit and internal power circuit are ON state.
VDD3 = 2.4~3.3V, electric volume is MAX(“11111111”).
bias = 1/5~1/12, no load at LCD driver terminal.
CA_1= CA_2=1.0μF, DCON=“1”, AMPON=“1”
*13. Applicable under internal oscillator circuit and internal power circuit are ON state and no access from CPU.
Electric volume is “11111111”.
Display data is all ON or cross check pattern, and no load at LCD driver terminal.
Test condition: VDD2=VDD3, CA_1=CA_2=1.0μF, DCON=“1”, AMPON=“1”, Ta=25°C.
*14. VLCD, VCL1, VCL2, VCL3 and VCL4 terminals.
VDD3 = 3.0V, VOUT=15.0V, bias = 1/5~1/12, electric volume is “11111111”
Display OFF and no load at LCD drive terminal.
Boosting coefficient N is 5 times.
Test condition: CA_1=CA_2=1.0μF, DCON=“1”, AMPON=“1”.

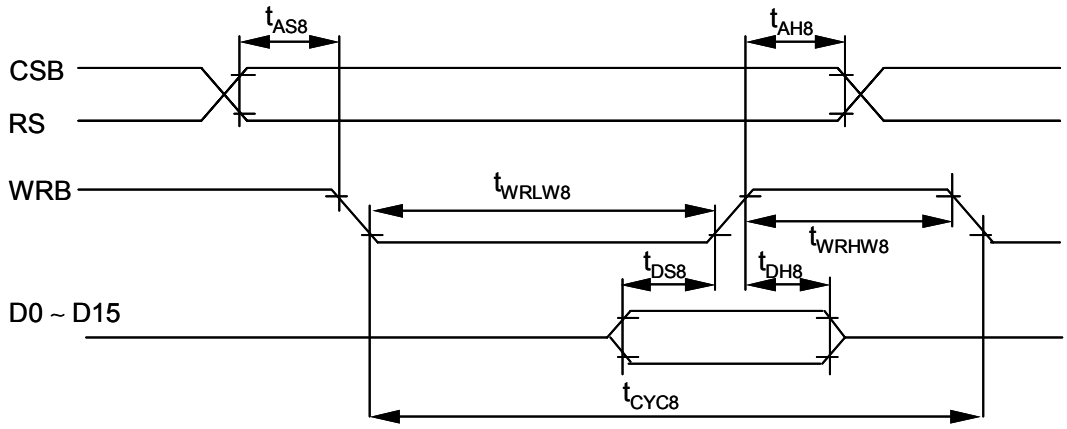


VD12：①−②
VD34：③−④
VD24：②−④

■ AC CHARACTERISTICS

(1) Write operation (80-type MPU)

Write Timing-1



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSB RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		90 35 35		ns ns ns	WRB
Data setup time Data hold time	t_{DS8} t_{DH8}		30 5		ns ns	D_0 to D_{15}

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

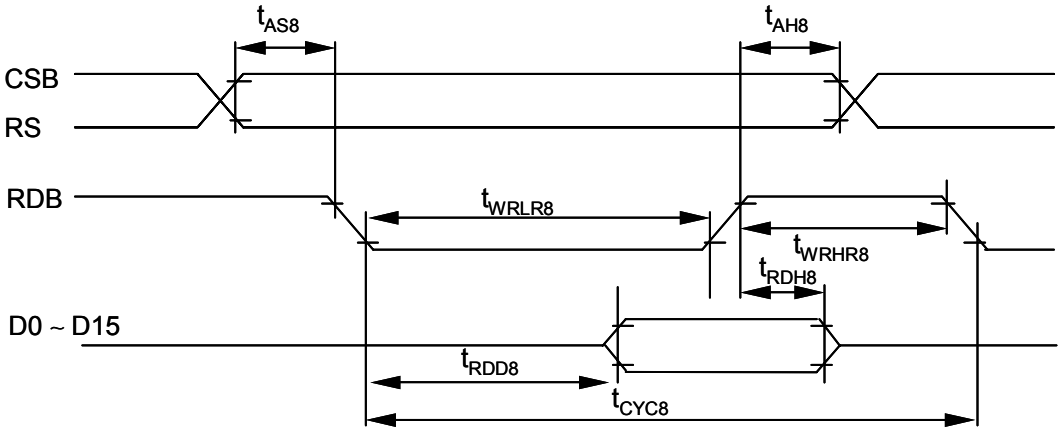
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSB RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		160 70 70		ns ns ns	WRB
Data setup time Data hold time	t_{DS8} t_{DH8}		40 5		ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSB RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLW8} t_{WRHW8}		180 80 80		ns ns ns	WRB
Data setup time Data hold time	t_{DS8} t_{DH8}		70 10		ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(2) Read operation (80-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSB RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDB
Read Data delay time Read Data hold time	T_{RDD8} T_{RDH8}	CL=15pF	 10	60	ns ns	D_0 to D_{15}

(V_{DD}=2.2to 2.5V, Ta=-30 to +85°C)

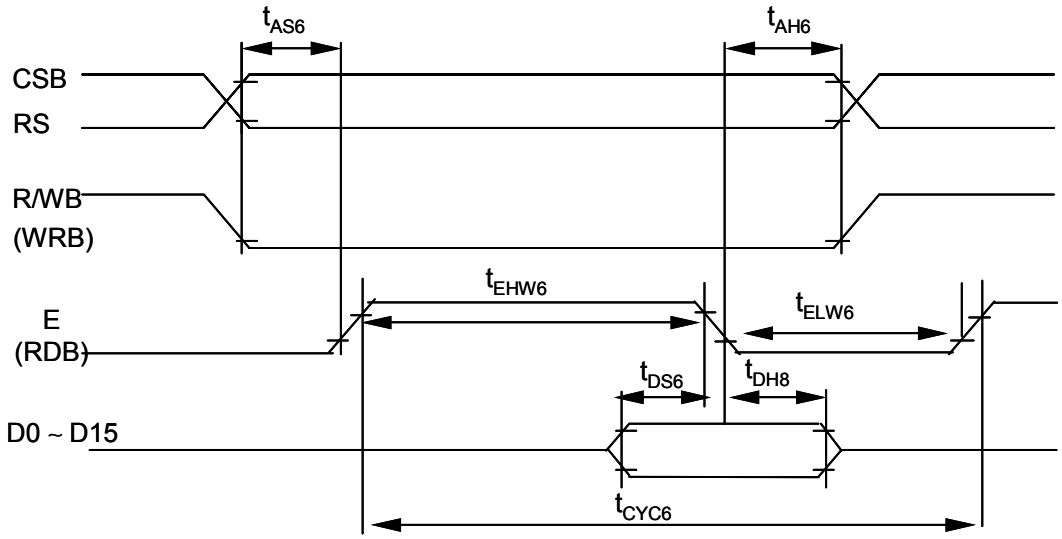
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSB RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		180 80 80		ns ns ns	RDB
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 10	60	ns ns	D_0 to D_{15}

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH8} t_{AS8}		0 0		ns ns	CSB RS
System cycle time Enable "L" level pulse width Enable "H" level pulse width	t_{CYC8} t_{WRLR8} t_{WRHR8}		250 120 120		ns ns ns	RDB
Read Data delay time Read Data hold time	t_{RDD8} t_{RDH8}	CL=15pF	 10	110	ns ns	D_0 to D_{15}

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(3) Write operation (68-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	
Enable ”L” level pulse width	t_{ELW6}		35		ns	E
Enable ”H” level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D_0 to D_{15}
Data hold time	t_{DH6}		5		ns	

(V_{DD1}=2.2 to 2.5V, Ta=-30 to +85°C)

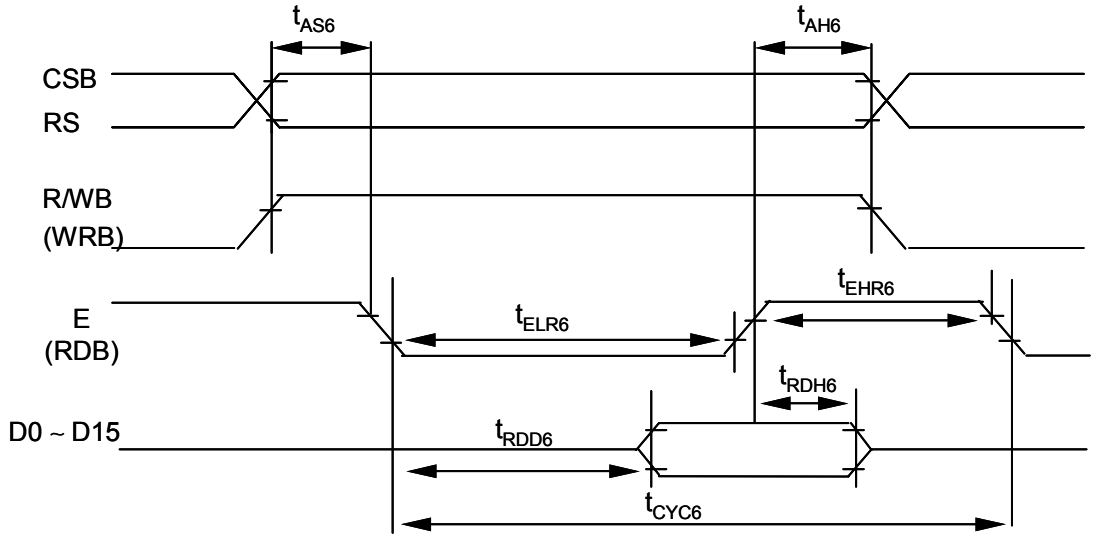
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	
Enable ”L” level pulse width	t_{ELW6}		70		ns	E
Enable ”H” level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D_0 to D_{15}
Data hold time	t_{DH6}		10		ns	

(V_{DD1}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSB
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	
Enable ”L” level pulse width	t_{ELW6}		80		ns	E
Enable ”H” level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D_0 to D_{15}
Data hold time	t_{DH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(4) Read operation (68-type MPU)



(V_{DD1}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSB RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	 0	70	ns ns	D_0 to D_{15}

(V_{DD1}=2.2 to 2.5V, Ta=-30 to +85°C)

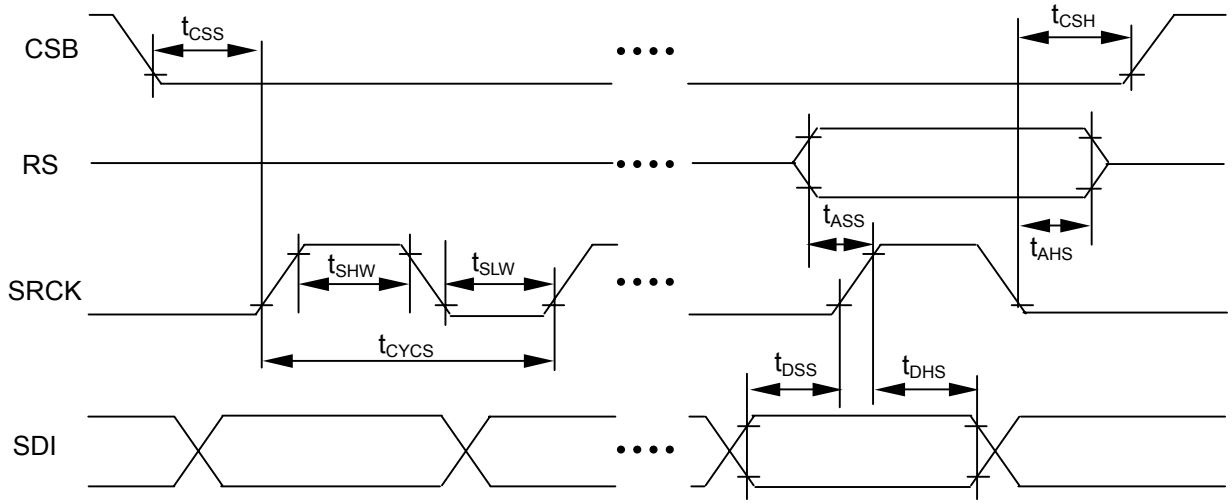
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSB RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		180 80 80		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	 0	70	ns ns	D0 to D15

(V_{DD1}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time Address setup time	t_{AH6} t_{AS6}		0 0		ns ns	CSB RS
System cycle time Enable ”L” level pulse width Enable ”H” level pulse width	t_{CYC6} t_{ELR6} t_{EHR6}		250 120 120		ns ns ns	E
Read Data delay time Read Data hold time	t_{RDD6} t_{RDH6}	CL=15pF	 10	110	ns ns	D0 to D15

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(5) Serial interface



(V_{DD1}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SRCK
SRCK "H" level pulse width	t_{SHW}		20		ns	
SRCK "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDI
Data hold time	t_{DHS}		20		ns	
CSB – SRCK time	t_{CSS}		20		ns	CSB
CSB hold time	t_{CSH}		20		ns	

(V_{DD1}=2.2 to 2.5V, Ta=-30 to +85°C)

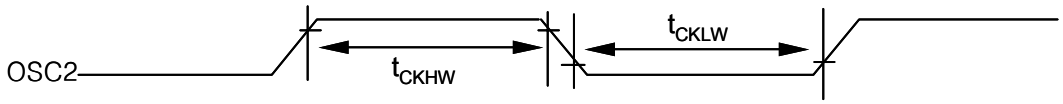
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	SRCK
SRCK "H" level pulse width	t_{SHW}		20		ns	
SRCK "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDI
Data hold time	t_{DHS}		20		ns	
CSB – SRCK time	t_{CSS}		20		ns	CSB
CSB hold time	t_{CSH}		20		ns	

(V_{DD1}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	SRCK
SRCK "H" level pulse width	t_{SHW}		35		ns	
SRCK "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		5		ns	SDI
Data hold time	t_{DHS}		35		ns	
CSB – SRCK time	t_{CSS}		35		ns	CSB
CSB hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(6) Source Clock timing

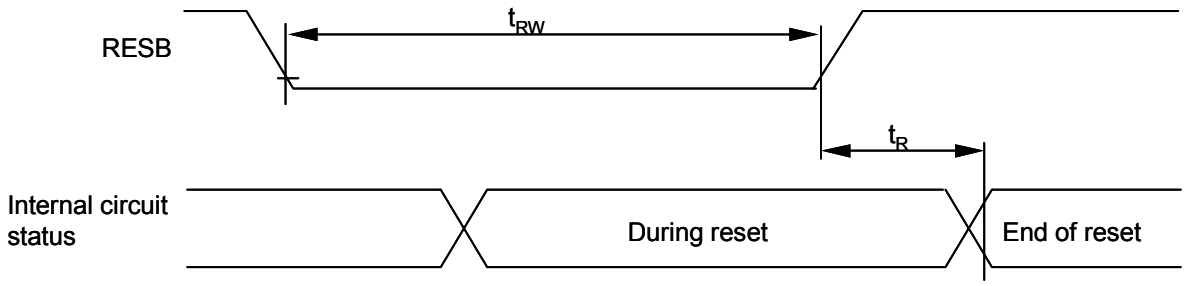


(V_{DD2}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC2 "H" level pulse width (1)	t_{CKHW}	MCLK<7:0>	0.235	0.318	µs	OSC2
OSC2 "L" level pulse width (1)	t_{CKLW}	="00000000"	0.235	0.318	µs	
OSC2 "H" level pulse width (2)	t_{CKHW}	MCLK<7:0>	0.353	0.478	µs	OSC2
OSC2 "L" level pulse width (2)	t_{CKLW}	="01000000"	0.353	0.478	µs	
OSC2 "H" level pulse width (3)	t_{CKHW}	MCLK<7:0>	0.434	0.588	µs	OSC2
OSC2 "L" level pulse width (3)	t_{CKLW}	="10000000"	0.434	0.588	µs	
OSC2 "H" level pulse width (4)	t_{CKHW}	MCLK<7:0>	0.55	0.744	µs	OSC2
OSC2 "L" level pulse width (4)	t_{CKLW}	="11000000"	0.55	0.744	µs	

Note) Each timing is specified based on 20% and 80% of V_{DD1}.

(7) Reset input timing



(V_{DD1}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESB "L" level pulse width	t_{RW}		10.0		µs	RESB

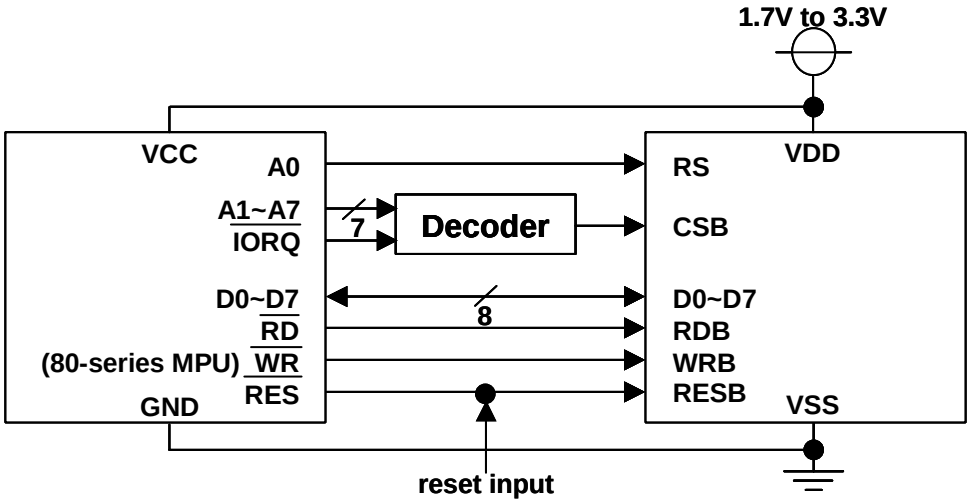
(V_{DD1}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESB "L" level pulse width	t_{RW}		10.0		µs	RESB

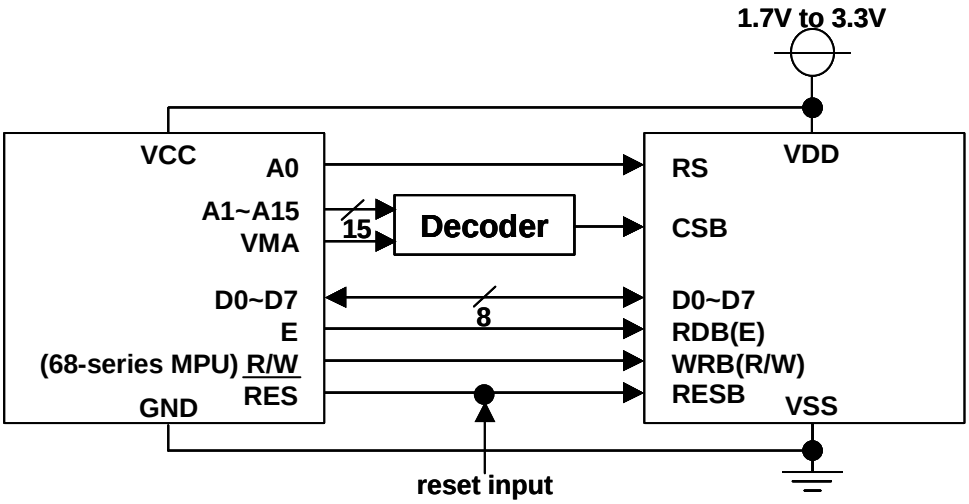
Note) Each timing is specified based on 20% and 80% of V_{DD1}.

■ MPU Connections

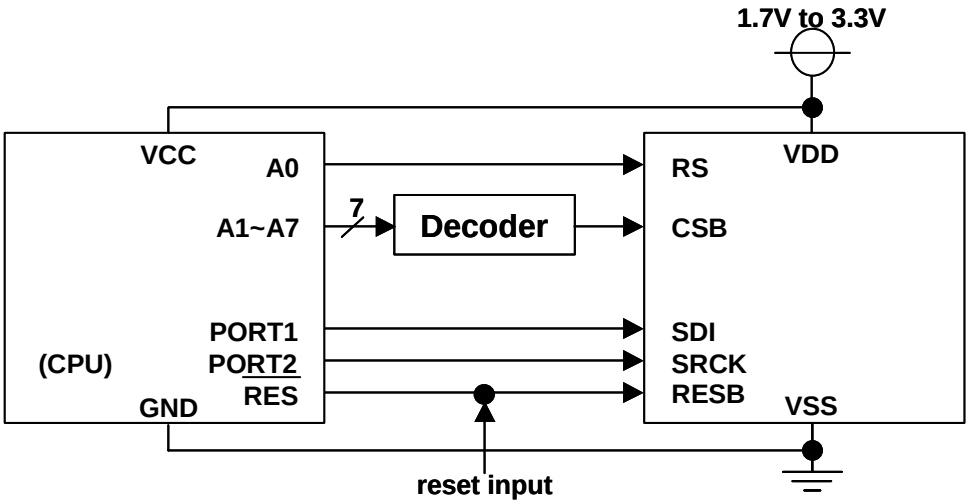
80-type MPU interface



68-type MPU interface



Serial interface



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