MN83901ABG-C

LCD Panel Source Driver

■ Overview

The MN83901ABG-C is an LCD panel source driver that can display an analog video signal on a color TFT LCD panel in products such as LCD TV sets and camcorders.

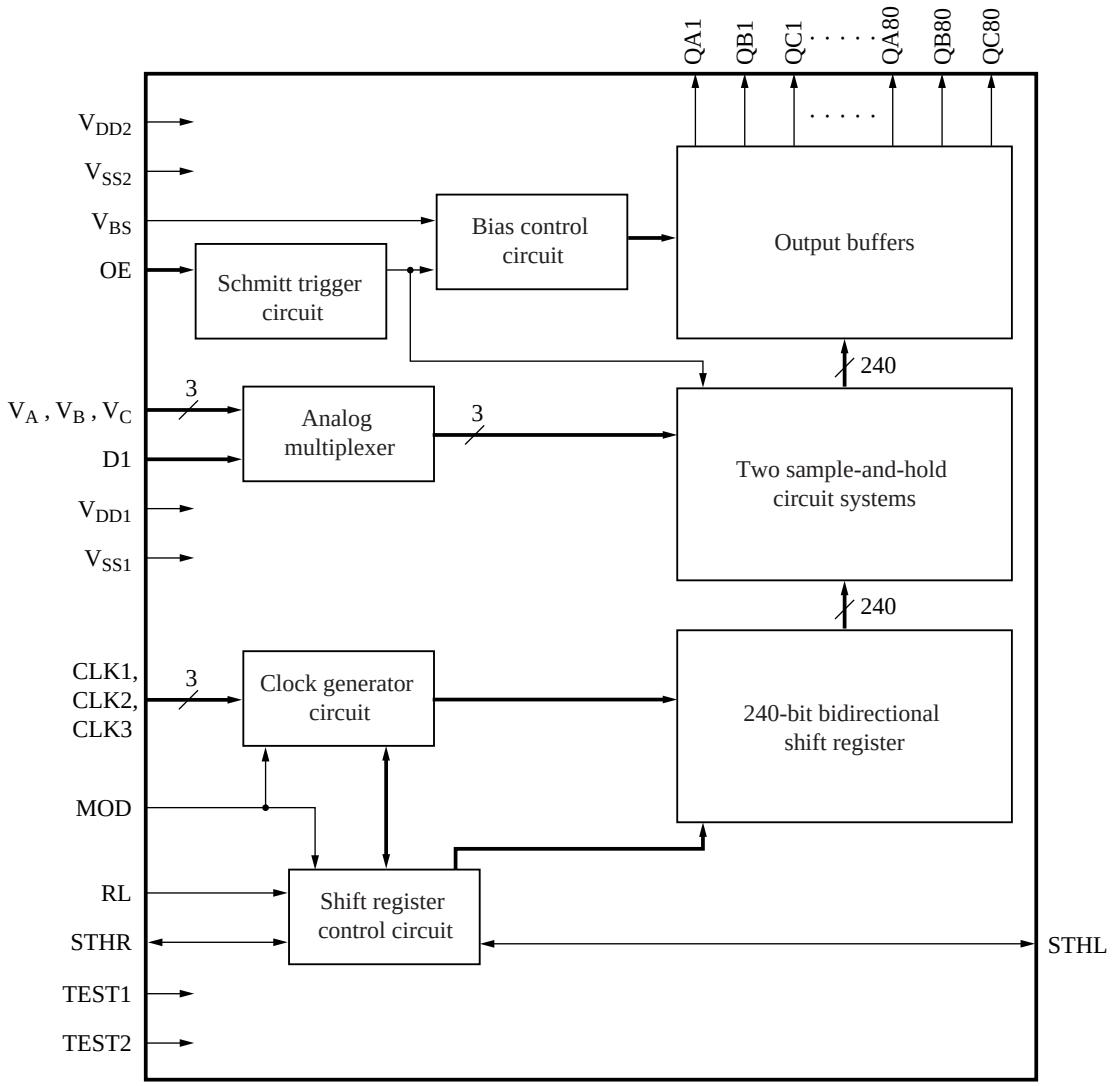
■ Features

- Number of driver outputs: 240 outputs
- Lower power consumption and lower EMI due to a 2.7 to 5.5 V digital power supply system and a 5.0 V analog power supply system.
- Wide dynamic range: 4.6 V (at supply voltage: 5.0 V)
- Low inter-pin variation between output pins: ±20 mV (typical)
- Provides analog RGB signal switching to support both stripe and delta color filter arrays.
- Mode input selects between sequential sampling (CLK1, CLK2, and CLK3 input) and simultaneous sampling (CLK1 input, with CLK2 and CLK3 held at V_{DD1}).
- Schmitt trigger circuit minimizes noise on the OE pin.
- Supports serial cascade connection.
- The clock is automatically stopped after a fixed amount of data is acquired.
- Bidirectional shift register
- Supports mounting in thin-frame panels. (The chip short side length is under 1 mm.)
- Package type: bare chip

■ Applications

- LCD panel driver for LCD TVs and camcorders

■ Block Diagram



■ Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Description</th></tr>
<tr><td>STHR
STHL</td><td>I/O</td><td>Shift data input and output</td><td>Input and output pins for the data handled by the bidirectional shift register. The input and output functions are switched by the RL pin as shown below.
<table>
<tr><th>RL</th><th>STHR</th><th>STHL</th></tr>
<tr><td>High</td><td>I</td><td>O</td></tr>
<tr><td>Low</td><td>O</td><td>I</td></tr>
</table>
1) Input
The data input to the first stage of the shift register.
This data is acquired in synchronization with the rising edge of CLK1.
2) Output
Outputs data for input to the next stage when this IC is connected in cascade (series).
This data is output in synchronization with the rising edge of CLK1.</td></tr>
<tr><td>RL</td><td>I</td><td>Shift direction selection</td><td>This pin specifies the shift direction of the bidirectional shift register.
RL = high : QA1 → QB1 → QC1 · · ·→ QC80
RL = low : QC80 → QB80 → QA80 · · ·→ QA1</td></tr>
<tr><td>CLK1 to
CLK3</td><td>I</td><td>Clock inputs</td><td>Clocks that shift the sample-and-hold signals for the data output to the LCD drive output pins (QA1 to QC80). The relation between these clocks and the output pins is as follows.
1) MOD = low (Sequential sampling mode)
CLK1 : RL = high : QA1 to QA80
RL = low : QC1 to QC80
CLK2 : QB1 to QB80
CLK3 : RL = high : QC1 to QC80
RL = low : QA1 to QA80
2) MOD = high (Simultaneous sampling mode)
CLK1 : QA1 to QA80
: QB1 to QB80
: QC1 to QC80
CLK2 : Connect to V_{DDI}.
CLK3 : Connect to V_{DDI}.</td></tr>
<tr><td>OE</td><td>I</td><td>Output enable</td><td>The rising edge of this signal switches between the two sample-and-hold circuit systems and starts the output of new data. When the output reaches the drive potential, the capacity is automatically lowered, and at the same time the drive potential is held steady.</td></tr>
</table>

■ Pin Descriptions (continued)

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Function</th><th>Description</th></tr>
<tr><td>D1</td><td>I</td><td>Analog signal switching</td><td>Sets which of the analog input signals V_A, V_B, and V_C, are output from which of the QA, QB, and QC outputs.
<table>
<tr><th>D1</th><th>I</th><th>O</th></tr>
<tr><td rowspan="3">Low</td><td>V_A</td><td>QA1 to QA80</td></tr>
<tr><td>V_B</td><td>QB1 to QB80</td></tr>
<tr><td>V_C</td><td>QC1 to QC80</td></tr>
<tr><td rowspan="3">High</td><td>V_A</td><td>QB1 to QB80</td></tr>
<tr><td>V_B</td><td>QC1 to QC80</td></tr>
<tr><td>V_C</td><td>QA1 to QA80</td></tr>
</table></td></tr>
<tr><td>V_{BS}</td><td>I</td><td>Bias adjustment</td><td>The voltage applied to this pin adjusts the output buffer bias and modifies the drive capacity of the LCD drive outputs.</td></tr>
<tr><td>V_A
V_B
V_C</td><td>I</td><td>Analog signal inputs</td><td>Inputs for the analog signals for output from the LCD drive output pins</td></tr>
<tr><td>QA1 to QA80
QB1 to QB80
QC1 to QC80</td><td>O</td><td>LCD drive outputs</td><td>The analog input signals V_A, V_B, or V_C are sampled and held, and those levels are output from these pins.</td></tr>
<tr><td>MOD</td><td>I</td><td>Mode selection input</td><td>Selects whether the sampling of the 3 analog input signals V_A, V_B, and V_C is performed simultaneously or sequentially.
MOD = high: Simultaneous sampling
MOD = low: Sequential sampling</td></tr>
<tr><td>TEST1</td><td>I</td><td>Test input</td><td>Connect to V_{DD1}.</td></tr>
<tr><td>TEST2</td><td>I</td><td>Test input</td><td>Connect to V_{DD1}.</td></tr>
<tr><td>V_{DD1}</td><td>—</td><td>Digital system high potential power supply</td><td>High-level side of the digital (logic) system power supply</td></tr>
<tr><td>V_{DD2}</td><td>—</td><td>Analog system high potential power supply</td><td>High-level side of the analog system power supply used for sample-and-hold and other circuits</td></tr>
<tr><td>V_{SS1}</td><td>—</td><td>Digital system ground</td><td>Digital system ground used for logic and other circuits</td></tr>
<tr><td>V_{SS2}</td><td>—</td><td>Analog system ground</td><td>Analog system ground used for sample-and-hold and other circuits</td></tr>
</table>

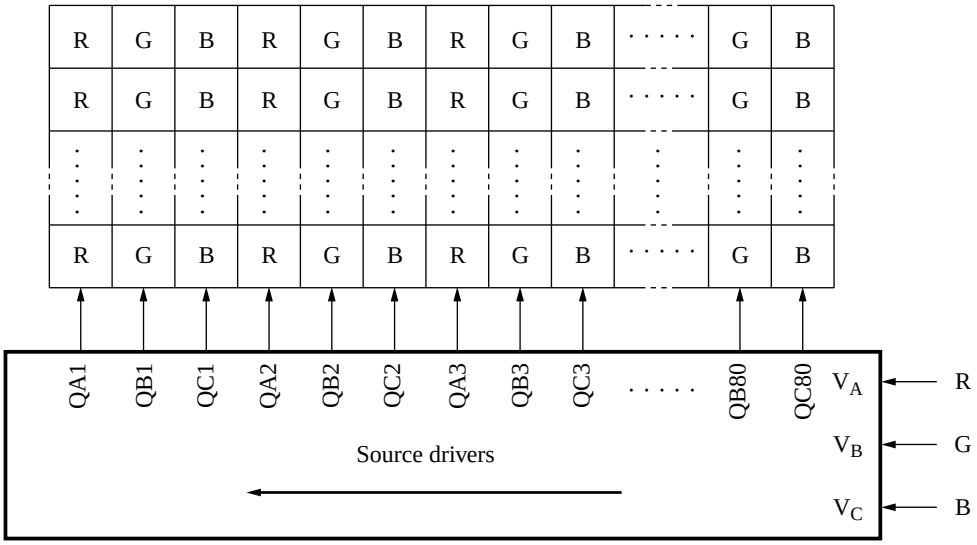
■ Functional Description

1. Output signals

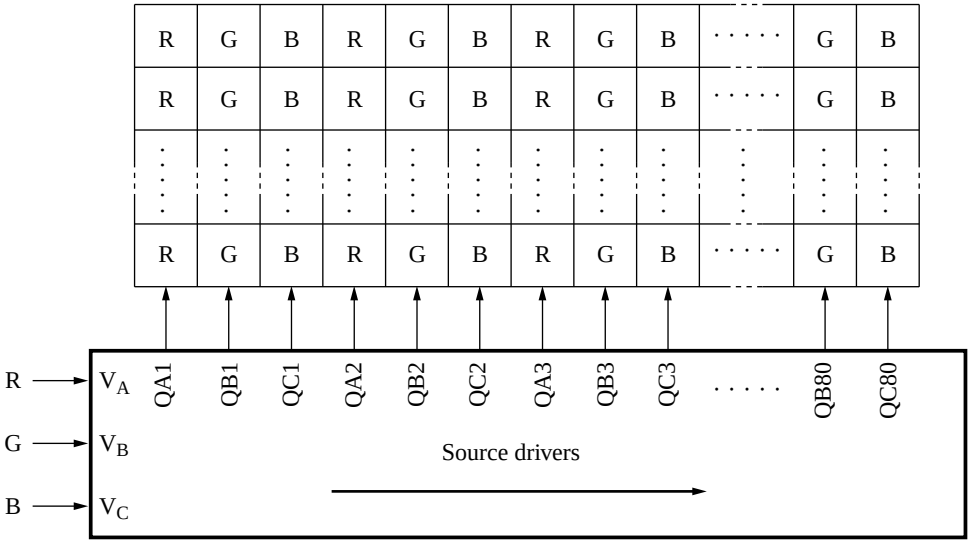
The MN83901ABG-C supports both stripe and delta color filter arrangement LCD panels. The relationship between the input pins and the output pins is switched by the DI pin.

1) Stripe arrangement

- Left-shift mode (RL = low), DI = low



- Right-shift mode (RL = high), DI = low

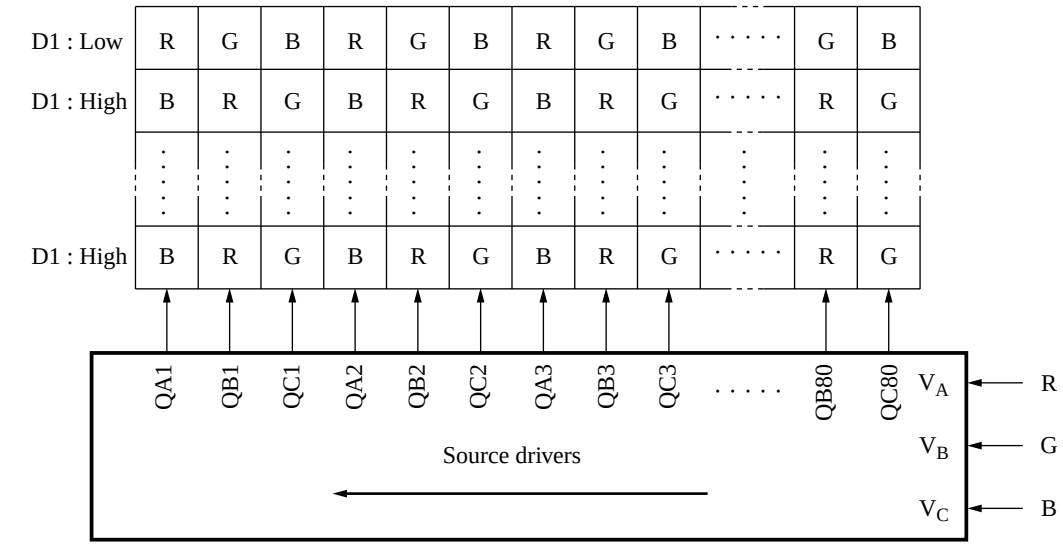


■ Functional Description (continued)

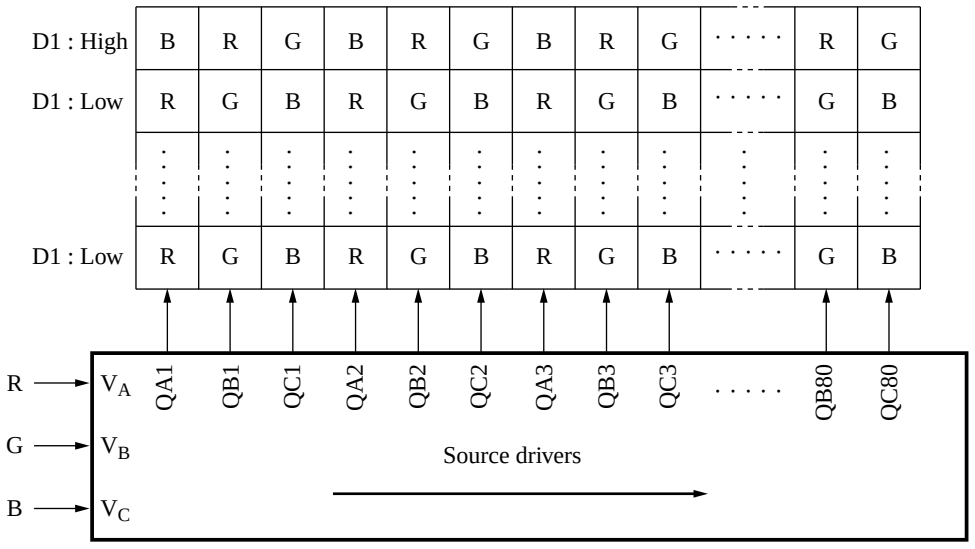
1. Output signals (continued)

2) Delta arrangement

• Left-shift mode (RL = low)



• Right-shift mode (RL = high)

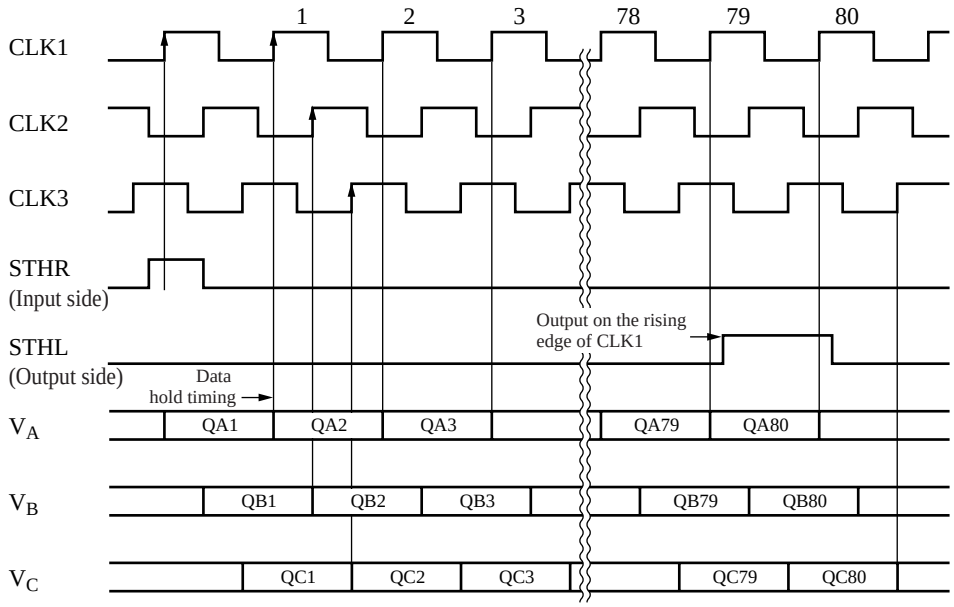


■ Functional Description (continued)

2. Recommended operating timing diagrams

1) QA1 → QC80 transfer mode: DI = low, MOD = low

- Sequential sampling mode



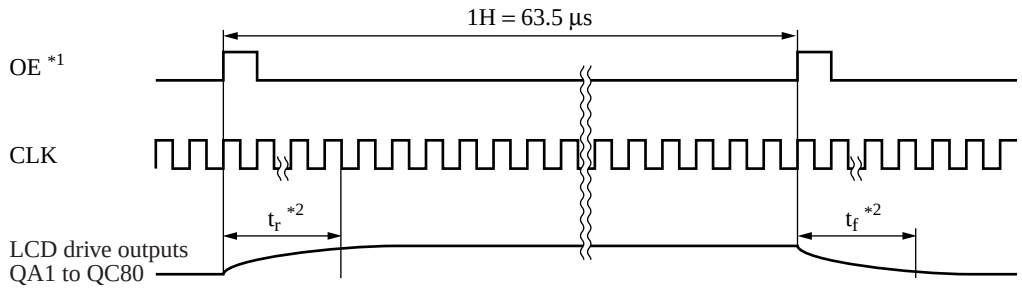
- Start of sampling

  When CLK1 rises, the start pulse (STHR = high) is acquired and sampling of the analog signal QA1 starts. The analog signal QA1 is held on the next CLK1 rising edge.

- Auto standby function

  After sampling the analog signal QC80, the IC automatically goes to the standby state, the shift register is reset, and sampling is not performed until a high level is input to STHR again.

  When multiple start pulses are input, although all the start pulses are transmitted to the shift register, the IC goes to the standby state 81 clock cycles after the first start pulse.



Note) *1: The rising edge of this signal switches between the two sample-and-hold circuit systems and starts the output of new data. When the output reaches the drive potential, the capacity is automatically lowered, and at the same time the drive potential is held steady.

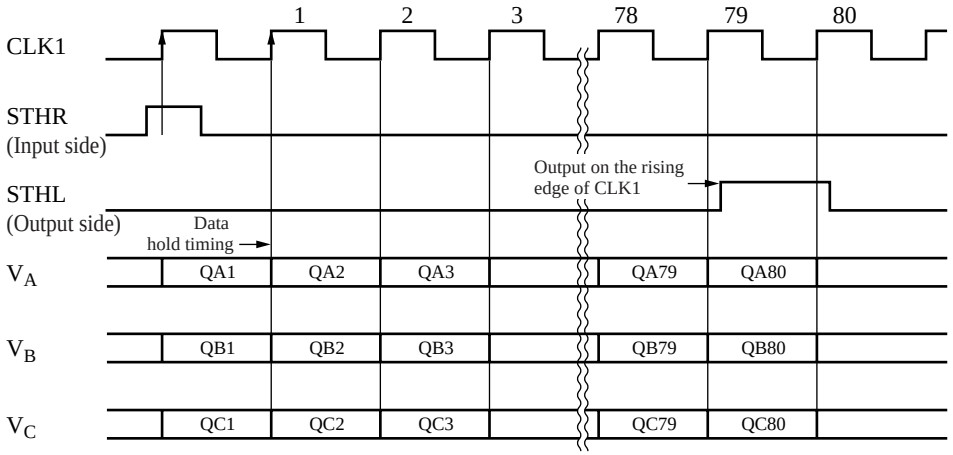
*2: The settling time is adjusted with V_{BS}.

■ Functional Description (continued)

2. Recommended operating timing diagrams (continued)

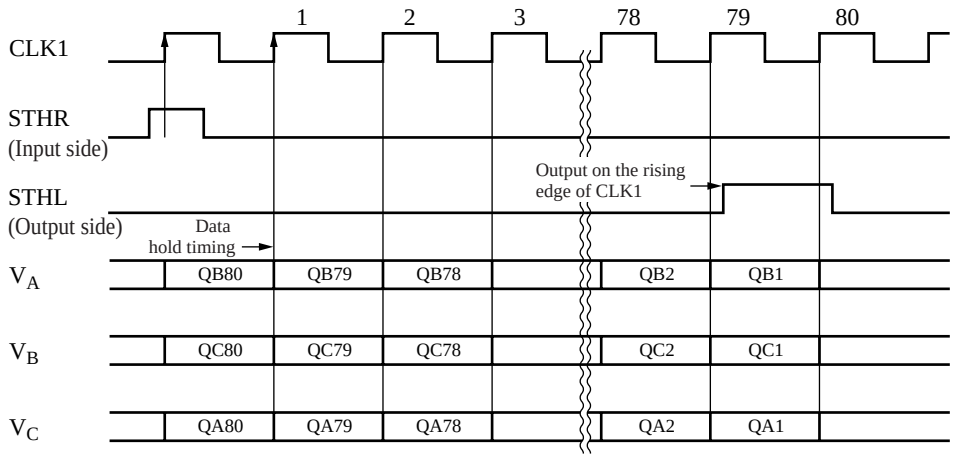
2) QA1 → QC80 transfer mode: DI = low, MOD = high

- Simultaneous sampling mode (Connect CLK2 and CLK3 to V_{DDI}.)



3) QC80 → QA1 transfer mode: DI = high, MOD = high

- Simultaneous sampling mode (Connect CLK2 and CLK3 to V_{DDI}.)



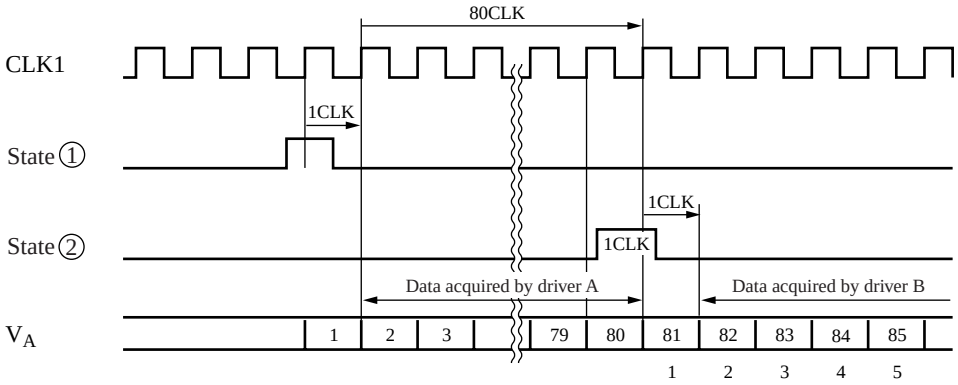
■ Functional Description (continued)

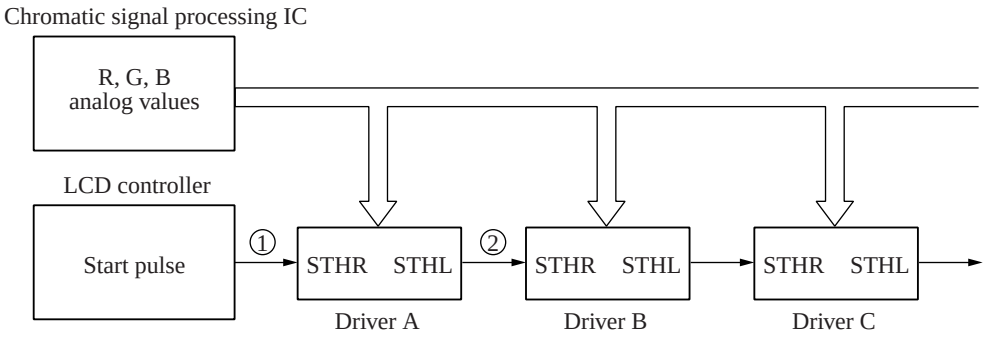
3. Operation when cascade connection is used

• When RL is high

When a start pulse is input to STHR, after one clock (CLK) cycle passes, driver A starts to acquire data. STHL (carry output) rises 80 clock cycles after the start pulse input, and one clock cycle later, data acquisition stops.

Driver B accepts the driver A STHL output as a start pulse input, and starts data acquisition one clock cycle later.





■ Electrical Characteristics

1. Absolute Maximum Ratings at V_{SS1} = 0 V, V_{SS2} = 0 V

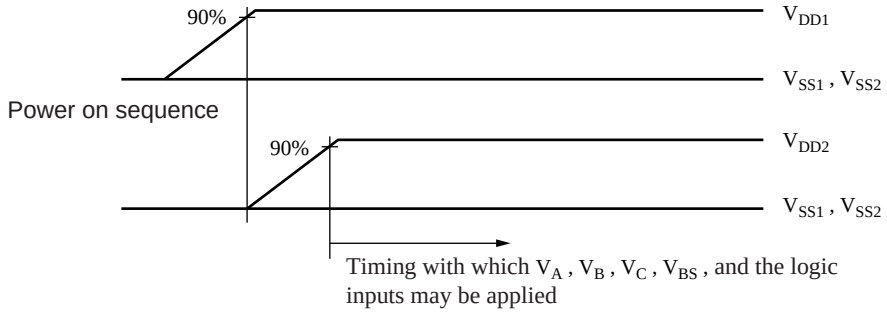
Item	Symbol	Rating	Unit
Digital system supply voltage	V_{DD1}	– 0.3 to +7.0	V
Analog system supply voltage	V_{DD2}	– 0.3 to +7.0	V
Digital input voltage	V_{I1}	– 0.3 to V_{DD1} +0.3	V
Analog input voltage	V_{I2}	– 0.3 to V_{DD2} +0.3	V
Digital output voltage	V_{O1}	– 0.3 to V_{DD1} +0.3	V
Analog output voltage	V_{O2}	– 0.3 to V_{DD2} +0.3	V
Operating and storage temperature range	T_a	–30 to +85	°C
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +110	°C

Note) 1. The absolute maximum ratings are limit values for stresses applied to the chip so that the chip will not be destroyed. Operation is not guaranteed within these ranges.
Also, the operating and storage temperature range is the temperature range over which the IC may be operated without damage to the IC. IC performance is not guaranteed within this range.
2. These ratings are guaranteed values when the standard Panasonic package is used.

2. Operating Conditions at V_{SS1} = 0 V, V_{SS2} = 0 V, T_a = -20°C to +75°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating digital system supply voltage	V_{DD1}		2.7	3.0	5.5	V
Operating analog system supply voltage	V_{DD2}		4.5	5.0	5.5	V
Analog reference voltage	V_{BS}		1.0	2.0	3.0	V
Operating frequency	f_{clk}		0.5	—	15	MHz
Analog input voltage	V_{IA} to V_{IC}		0.2	—	V_{DD2} – 0.2	V
Drive output load capacitance	C_Y		—	—	100	pF
Digital signal input pin capacitance	C_{inD}	For a 1 MHz input signal	—	8	20	pF
Analog signal input pin capacitance	C_{inA}	For a 1 MHz input signal	—	10	20	pF

Note) 1. The multiple V_{DD1} and V_{DD2} power supply pins must all be connected to the power supply level.
2. The multiple V_{SS1} and V_{SS2} ground pins must all be connected to ground.
3. When powering on this IC, first apply V_{DD1} and V_{DD2}, and only then apply V_A, V_B, V_C, V_{BS}, and the logic inputs.
When power down this IC, use the reverse sequence from the power on sequence.



4. The operating supply voltages are the voltages applied to V_{DD1} and V_{DD2}.
5. These ratings are guaranteed values when the standard Panasonic package is used.

■ Electrical Characteristics (continued)

3. DC Characteristics (continued) at V_{DD1} = 2.7 V to 5.5 V, V_{DD2} = 5.0 V, V_{SS1} = V_{SS2} = 0 V, V_{BS} = 2.5 V, f_{clk} = 15 MHz, T_a = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Operating analog system supply current 1 *1, 2, 3	I_{DD1}		—	4.5	10	mA
Operating analog system supply current 2 *3, 4	I_{DD2}	With no load	—	3.5	—	mA
Operating digital system supply current *1	I_{DD3}		—	2.3	6.5	mA
Quiescent digital system supply current	I_{DD4}	In the clock stopped state	—	—	100	µA
1) Input pins: RL, CLK1, D1						
High-level input voltage	V_{IH1}		$0.7 \times V_{DD1}$	—	V_{DD1}	V
Low-level input voltage	V_{IL1}		0	—	$0.3 \times V_{DD1}$	V
Input leakage current	V_{LI1}		–10	—	10	µA
2) Schmitt trigger input pins: OE						
High-level input voltage	V_{IH2}		$0.8 \times V_{DD1}$	—	V_{DD1}	V
Low-level input voltage	V_{IL2}		0	—	$0.2 \times V_{DD1}$	V
Schmitt voltage	ΔV_{smt}	V_{DD1} = 3.3 V	—	0.5	—	V
Input leakage current	V_{LI2}		–10	—	10	µA
3) Conditional (when MOD is high) pull-up resistor input pins: CLK2, CLK3						
High-level input voltage	V_{IH3}		$0.7 \times V_{DD1}$	—	V_{DD1}	V
Low-level input voltage	V_{IL3}		0	—	$0.3 \times V_{DD1}$	V
Pull-up resistance	R_{PU3}	V_{DD1} = 3.6 V	1.5	5	15	kΩ
4) Pull-up resistor input pins: TEST1, TEST2						
High-level input voltage	V_{IH4}		$0.7 \times V_{DD1}$	—	V_{DD1}	V
Low-level input voltage	V_{IL4}		0	—	$0.3 \times V_{DD1}$	V
Pull-up resistance	R_{PU4}	V_{DD1} = 3.6 V	1.5	5	15	kΩ
5) Pull-down resistor input pins: MOD						
High-level input voltage	V_{IH5}		$0.7 \times V_{DD1}$	—	V_{DD1}	V
Low-level input voltage	V_{IL5}		0	—	$0.3 \times V_{DD1}$	V
Pull-down resistance	R_{PU5}	V_{DD1} = 3.6 V	30	100	300	kΩ
6) I/O pins: STHR, STHL						
High-level input voltage	V_{IH6}		$0.7 \times V_{DD1}$	—	V_{DD1}	V
Low-level input voltage	V_{IL6}		0	—	$0.3 \times V_{DD1}$	V
High-level output voltage	V_{OH}	I_O = –1 mA	V_{DD1} – 0.1	—	—	V
Low-level output voltage	V_{OL}	I_O = 1 mA	—	—	0.1	V
7) Analog input pins: V_A , V_B , V_C						
Input current	I_{VA} to I_{VC}	Analog input (V_A , V_B , V_C) frequency = 0.5 MHz Analog input (V_A , V_B , V_C) amplitude = (V_{DD2} – 0.2) to 0.2 V	–150	—	150	mA

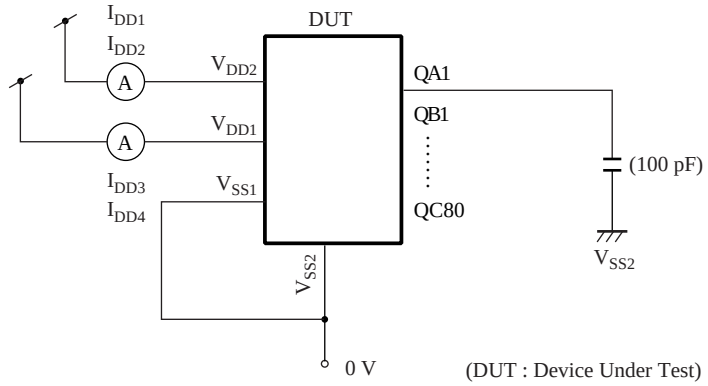
■ Electrical Characteristics (continued)

3. DC Characteristics (continued) at V_{DD1} = 2.7 V to 5.5 V, V_{DD2} = 5.0 V, V_{SS1} = V_{SS2} = 0 V, V_{BS} = 2.5 V, f_{clk} = 15 MHz, T_a = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
8) Reference voltage input pin: V_{BS}						
Input leakage current	I_{VBS}		−10	—	10	mA
9) Analog output pins: QA1 to QC80						
Output current	I_{OH}	Analog input voltage (V_A , V_B , V_C) = 4.8 V Output pin applied voltage (QA1 to QC80) = 3.8 V V_{BS} = 2.7 V	0.03	0.05	—	mA
	I_{OL}	Analog input voltage (V_A , V_B , V_C) = 0.2 V Output pin applied voltage (QA1 to QC80) = 1.2 V	0.15	2	—	
Inter-pin output voltage deviation *5	ΔV_O	Analog input voltage (V_A , V_B , V_C) = 0.2 V, 2.5 V, 4.8 V $\Delta V_O = V_{OUT} - \frac{V_{MAX} + V_{MIN}}{2}$	—	±20	—	mV

Note) 1. *1: Load conditions

Analog input signals (V_A, V_B, V_C) = 7.5 MHz, amplitude = 0.2 V to 4.8 V, OE = 100 kHz, V_{BS} = 2.5 V



(DUT : Device Under Test)

*2: The load on the analog output pins (QA1 to QC80) changes in certain cases.

*3: The formula for calculating the power consumption when a load is connected is as follows.

$I_{DD1} \times V_{DD2} + I_{DD3} \times V_{DD1}$

Use the value for I_{DD2} for I_{DD1} in the formula above to calculate the power consumption when there is no load.

*4: The no load power consumption value is provided for reference purposes only; this value is not guaranteed.

*5: V_{OUT} expresses the output voltage for each output pin, whereas V_{MAX} and V_{MIN} express the maximum and minimum values for the output voltage for the chip-internal output terminals.

2. These ratings are guaranteed values when the standard Panasonic package is used.

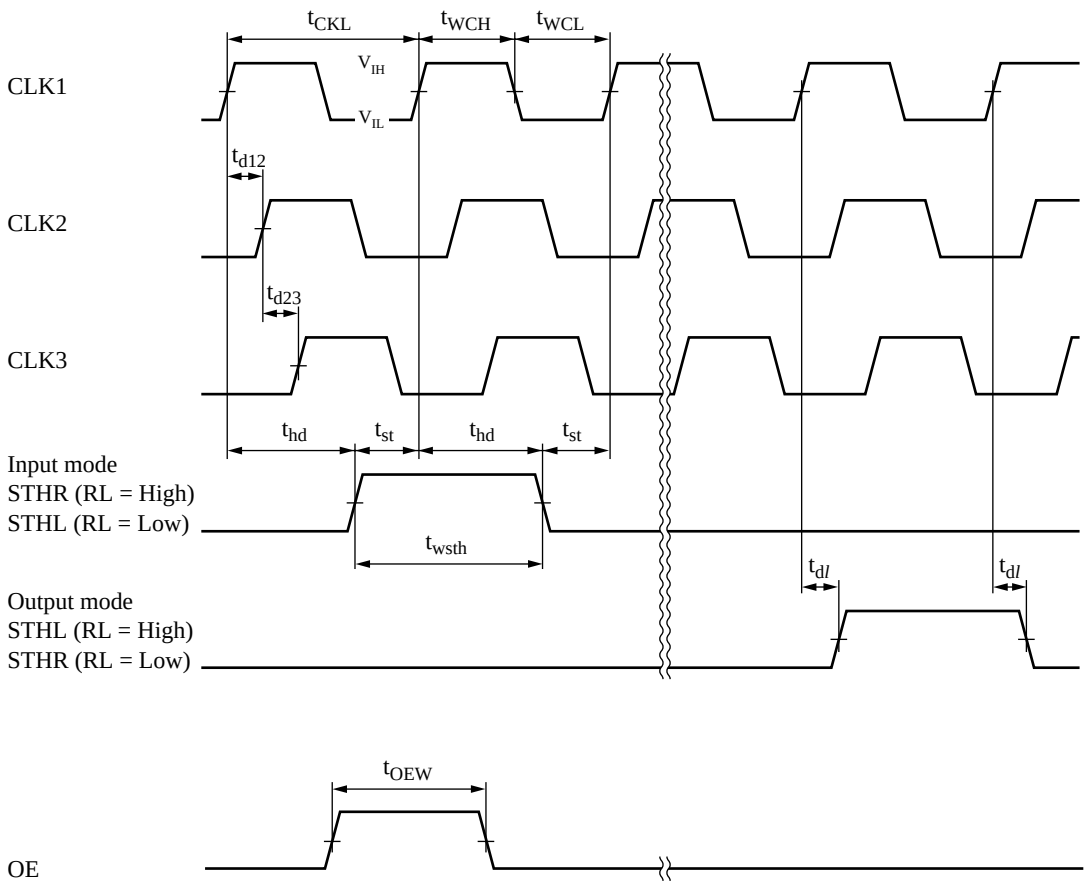
■ Electrical Characteristics (continued)

4. AC Characteristics at V_{DD1} = 2.7 V to 5.5 V, V_{DD2} = 5.0 V, V_{SS1} = V_{SS2} = 0 V, T_a = 25°C

Item	Symbol	Condition	Min	Typ	Max	Unit
Clock cycle time	t_{CLK}		66.6	—	2 000	ns
Clock high-level period	t_{WCH}		27	—	—	ns
Clock low-level period	t_{WCL}		27	—	—	ns
Clock delay time	t_{d12} , t_{d23}		16.6	—	t_{CLK} /2	ns
Start pulse setup time	t_{st}		10	—	t_{CLK} −5	ns
Start pulse hold time	t_{hd}		5	—	t_{CLK} −10	ns
Start pulse width	t_{wsth}		15	—	$2t_{CLK}$ −15	ns
Carry signal output delay time	t_{dl}	With a 25 pF load	5	—	56	ns
Output switching signal high-level period	t_{OEW}		1	—	—	µs

Note) These ratings are guaranteed values when the standard Panasonic package is used.

• Sequential sampling mode



Note) In simultaneous sampling mode, both CLK2 and CLK3 are held fixed at the high level.

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