Marconi
Electronic Devices

Frame Aligner with Optional Time Slot Zero Receiver

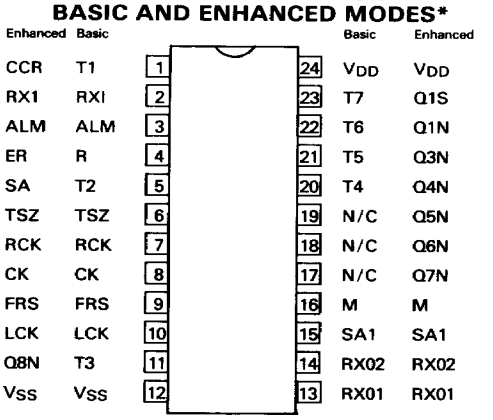
MA808

PRELIMINARY DATA

FEATURES

* Fabricated in low power CMOS
* Optional time slot zero receiver
* Detection of frame alignment signals for 30 channel PCM highways operating at 2048 kbit/s in accordance with CCITT recommendations G732
* Delay compensation and clock alignment between the transmission line system and the exchange
* Compensation of phase jitter, meeting the requirements of CCITT
* Detection and indication of loss of frame alignment
* Provision of a signal for generation of AIS
* Slip compensation
* Chip functional test facilities
* TTL compatible
* Operating power consumption 75mW max
* +5V single supply
* High latch-up immunity
* 256 kHz clock output
* Supplied in 24 Pin plastic DIL or CERDIP package

PIN ASSIGNMENT FOR BASIC AND ENHANCED MODES*



*The enhanced mode is selected by connecting Pin 16 to V_{DD}.

DESCRIPTION

The MEDL MA808 Frame Aligner chip has been primarily designed for use in equipment operating at the CCITT standard of 2048 kbit/s for 30 channel PCM data signals.

The basic function of the device is to accept a 2048 kbit/s data signal, whose frame structure conforms to CCITT recommendation G732 and frame synchronously align it to a local exchange/system clock.

The frame aligner operation is such that once a synchronisation sequence, as defined in CCITT recommendation G732, is received from a distant source synchronisation is established. Consequently the data stream is delayed such as to align it to the timing required at the local source. Once three successive sync. words are received containing errors, synchronisation is lost. The chip will remain out of sync. until the synchronising sequence is received.

The device can also, when configured in the 'enhanced mode' perform the additional function of time slot zero recovery.

A number of facilities are also provided to simplify the testing of the device and associated system.

The main applications for this device are in:

* Digital multiplex equipments.
* Interfaces between PCM line and switching systems.
* Concentrators.

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Issue 2
May 1986
C48

Integrated Circuits

OPERATION IN THE BASIC MODE

FRAME ALIGNMENT

The remote non-return-to-zero (NRZ) binary PCM data stream (RXI) required to be aligned must be applied to the frame aligner along with a synchronous clock (RCK). A time slot zero impulse (TSZ) as shown in Timing Diagram 1 is also required to define the start of the frame of input data.

A local clock (LCK) provides the timing from which the output data is clocked. Frame reset pulse (FRS) is the data output timing pulse. The MA808 aligns the 16th bit of the incoming data to this pulse, as shown in Diagram 1, and the 2 NRZ binary outputs RX01 and RX02 are produced. RX01 is purely a retimed version of the input data. RX02 has the third bit of all time slot zero locations of the input data inverted, thereby deliberately corrupting the frame sync. and the frame sync. verification words. Once synchronisation has been established FRS may be removed. If synchronisation is lost, FRS must be reapplied in order to permit resynchronisation to be established.

SLIP COMPENSATION

Small differences in frequency between the local and remote clocks (LCK and RCK) are compensated for by 'slipping in' (the repetition of) the previous frame, or 'slipping out' (the omission of) one complete frame of data.

INPUT ALARMS

Two input alarms (SA1 and ALM) are provided which will set data output(s) to an 'all ones' condition. ALM sets only RX02 and SA1 sets both RX01 and RX02 high (Timing Diagram 2).

TEST FEATURES

The operation of the internal memory of the MA808 is continuously monitored by performing a check sum comparison of the input and output data signals RXI and RX01. When an error is detected, the time slot zero words of RX01 and RX02 are set 'high'.

When a 'low' is applied to test input T3, the outputs RX01, RX02 and CK are forced into a 'three state' condition, thereby allowing associated circuitry to be tested independently of the MA808. Please note that this facility is only available in the basic mode of operation.

OPERATION IN THE ENHANCED MODE

When configured in the enhanced mode the chip performs time slot zero (TS0) recovery in addition to the frame alignment function. TS0 recovery may also be performed independently.

FRAME ALIGNMENT

The operation of frame alignment is essentially the same as the basic mode, except that the TSZ pulse is an output rather than an input, in accordance with the operation of the TS0 receiver, as shown in Timing Diagram 3. The operation of the input alarms to set the output data 'high' is the same as described in the basic mode (Timing Diagram 2).

TIME SLOT ZERO RECEIVER

Two output signals (TSZ and CCR) are provided so that the time slot zero receiver may be used independently of the frame alignment function. CCR is a channel reset pulse (as shown in Timing Diagram 3) which goes 'low' for one RCK period following a sync. word (every alternate frame) when the device is in sync. When the device is out of sync. the reset pulse occurs after each time slot zero.

The TS0 receiver accesses information contained within time slot zeros and processes it to offer the facilities of synchronisation alarm (SA), error output (ER) and time slot zero spare bits (Q1S, Q1N, Q3N-Q8N).

SYNCHRONISATION ALARM (SA)

SA indicates loss of sync. as shown in Timing Diagram 4. With the frame aligner operating in sync., SA will be 'low'. Following the receipt of 3 successive sync. words containing errors, SA will become active. SA will remain 'high' until the correct synchronising sequence as defined in CCITT recommendations G732 has been received.

ERROR OUTPUT (ER)

A logic signal, ER, indicating errors in sync. words, is provided as shown in Timing Diagram 4, from which an AIS alarm may be generated. ER is activated at the beginning of the second bit of time slot 1 two frames after the receipt of a sync. word containing errors. If successive sync. words contain errors, the signal will remain active. If synchronisation is lost, ER will remain active but will go 'low' for one period of the remote clock during the second bit of time slot 1, two frames after the receipt of a valid sync. word, as long as synchronisation is not regained at this time. If synchronisation is regained, ER will go 'low' for the two frames following the sync. word which caused synchronisation to be regained. The signal indicating an error in the sync. word two frames prior to synchronisation being regained will be delayed by one further sync. frame period. Consequently, it may be concluded that all errors in sync. words are accounted for in this signal, hence error monitoring in accordance with CCITT recommendations G7323.1.6.1 may be performed.

TIME SLOT ZERO SPARE BITS

The spare bits contained in both time slot zero words are converted from serial to parallel format (Q1N, Q3N-Q8N inc. and Q1S) are shown in Diagram 5.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
Supply voltage — operating V_{DD} - V_{SS}	−0.3	7.0	V
**Voltage on any Pin (V_{IN})	V_{SS} − 0.3V	V_{DD} + 0.3V	V
**Current through any Pin		±20	mA
Operating temperature	0	+70	°C
Storage temperature	−55	+150	°C

* Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**Guaranteed no latch up conditions.

D.C. ELECTRICAL CHARACTERISTICS at 25°C unless otherwise stated

Parameter	Min	Typ	Max	Units
Low level input voltage (V_{IL}) V_{DD} = 4.75V			0.8	V
High level input voltage (V_{IH}) V_{DD} = 5.25V	2.4			V
Low level input current (I_{IL}) V_{IN} = V_{SS}, V_{DD} = 5.25V			10.0	μA
High level input current (I_{IH}) V_{IN} = V_{DD}, V_{DD} = 5.25V			10.0	μA
Low level output voltage (V_{OL}) I_{OL} = 2mA, V_{DD} = 4.75V			0.5	V
High level output voltage (V_{OH}) I_{OH} = 0.2mA. V_{DD} = 4.75V	2.8			V
Output leakage current (I_{OL}) $V_{SS} < V_{OUT} < V_{DD}$. V_{DD} = 5.25V			±10	μA
Dynamic supply current ($I_{DD}(d)$)			15	mA
Static supply current ($I_{DD}(s)$)			1	mA

PIN DEFINITIONS

BASIC MODE

Pin	Def.	Function	Description
1	T1	Test I/P	Active high. To be tied to logic low during normal operation.
2	RXI	Data I/P	Recovered distant data input.
3	ALM	Alarm I/P	A logic high sets RX02 to an all 1s condition.
4	R	Reset I/P	'Low' resets the device tied 'high' normally.
5	T2	Test I/P	Active low. To be tied to logic high during normal operation.
6	TSZ	TS0 I/P	Remote TS0 timing signal.
7	RCK	Clock I/P	Recovered distant clock in sync. with RXI.
8	CK	256kHz O/P	256kHz square wave clock O/P synchronous with LCK.
9	FRS	Timing I/P	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock I/P	Local clock I/P.
11	T3	Test I/P	Active low. To be tied to logic high during normal operation.
12	V_{SS}	−ve I/P rail	Nominally 0v.
13	RX01	Data O/P	Retimed data output to LCK.
14	RX02	Data O/P	As per RX01 except that bit 3 of each TS0 word is inverted.
15	SA1	Set to all 1s I/P	A logic low sets RX01 and RX02 to an all 1s condition.
16	M	Mode I/P	A logic low selects basic mode operation.
17	N/C	No connection	To be left O/C during normal operation.
18	N/C	No connection	To be left O/C during normal operation.
19	N/C	No connection	To be left O/C during normal operation.
20	T4	Test I/P	Active when clocked by LCK (pin 10). To be tied to logic low during normal operation.
21	T5	Test I/P	Active when clocked by RCK (pin 7). To be tied to logic low during normal operation.
22	T6	Test O/P	To be left O/C during normal operation.
23	T7	Test O/P	To be left O/C during normal operation.
24	V_{DD}	+ve I/P rail	Nominally +5v.

ENHANCED MODE

Pin	Def.	Function	Description
1	CCR	Channel reset O/P	An output used to reset other devices within the system.
2	RXI	Data I/P	Recovered distant data input.
3	ALM	Alarm I/P	A logic high sets RX02 to an all 1s condition.
4	ER	Error O/P	A TS0 word error is signalled when ER goes to logic high.
5	SA	Sync. alarm O/P	Loss of sync. is signalled when SA goes to logic high.
6	TSZ	TS0 O/P	Remote TS0 output signal, (internally connected to the on-chip frame aligner).
7	RCK	Clock I/P	Recovered distant clock in sync. with RXI.
8	CK	256kHz O/P	256kHz square wave clock O/P synchronous with LCK.
9	FRS	Timing I/P	Data output timing pulse coincident with 16th bit of the local clock.
10	LCK	Clock I/P	Local clock I/P.
11	Q8N	O/P signal	Signal corresponding to bit 8 of the TS0 sync.
12	V_{SS}	−ve I/P rail	Nominally 0v.
13	RX01	Data O/P	Retimed data output to LCK.
14	RX02	Data O/P	As per RX01 except that bit 3 of each TS0 word is inverted.
15	SA1	Set to all 1s I/P	A logic low sets RX01 and RX02 to an all 1s state.
16	M	Mode I/P	A logic high selects enhanced mode operation.
17	Q7N	O/P signal	Signal corresponding to bit 7 of the TS0 sync. verification word.
18	Q6N	O/P signal	Signal corresponding to bit 6 of the TS0 sync. verification word.
19	Q5N	O/P signal	Signal corresponding to bit 5 of the TS0 sync. verification word.
20	Q4N	O/P signal	Signal corresponding to bit 4 of the TS0 sync. verification word.
21	Q3N	O/P signal	Signal corresponding to bit 3 of the TS0 sync. verification word.
22	Q1N	O/P signal	Signal corresponding to bit 1 of the TS0 sync. verification word.
23	Q1S	O/P signal	Signal corresponding to bit 1 of the TS0 sync. word.
24	V_{DD}	+ve I/P rail	Nominally +5v.

A.C. TIMING CHARACTERISTICS

All waveforms and timing relationships are shown in Timing Diagrams 6 and 7.

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
TSUD	Set up time of RXI to RCK (HL)		25			nS
TSUTSO	Set up time of TSZ to RCK (HL)		20			nS
TSUR	Set up time of FRS to LCK (HL)		150			nS
THDD	Hold time of Data wrt RCK (HL)		100			nS
THDTSOL	Hold time of TSZ(L) wrt RCK (HL)		50			nS
THDTSOH	Hold time of TSZ (H) wrt RCK (HL)		100			nS
THDR	Hold time of FRS wrt LCK (HL)		150			nS
f	Nominal frequency			2.048		MHz
TPD	Propagation delay of the LCK to RX01 and RX02	Outputs loaded to 10pf fclock = 2.048 MHz	30		150	nS
TPC	Propagation delay of the LCK (HL) to CK		0		175	nS
TPCCR1	Propagation delay of the RCK (HL) to CCR (HL)		0		150	nS
TPCCR2	Propagation delay of the RCK (LH) to CCR (LH)		0		150	nS
TPTSO	Propagation delay of the RCK (LH) to TSZ		20		200	nS
TPER	Propagation delay of the RCK (LH) to ER		20		200	nS
TPSA	Propagation delay of the RCK (LH) to SA		20		200	nS
TPQXY	Propagation delay of the RCK (LH) to Q8N–Q3N, Q1N and Q1S		20		200	nS

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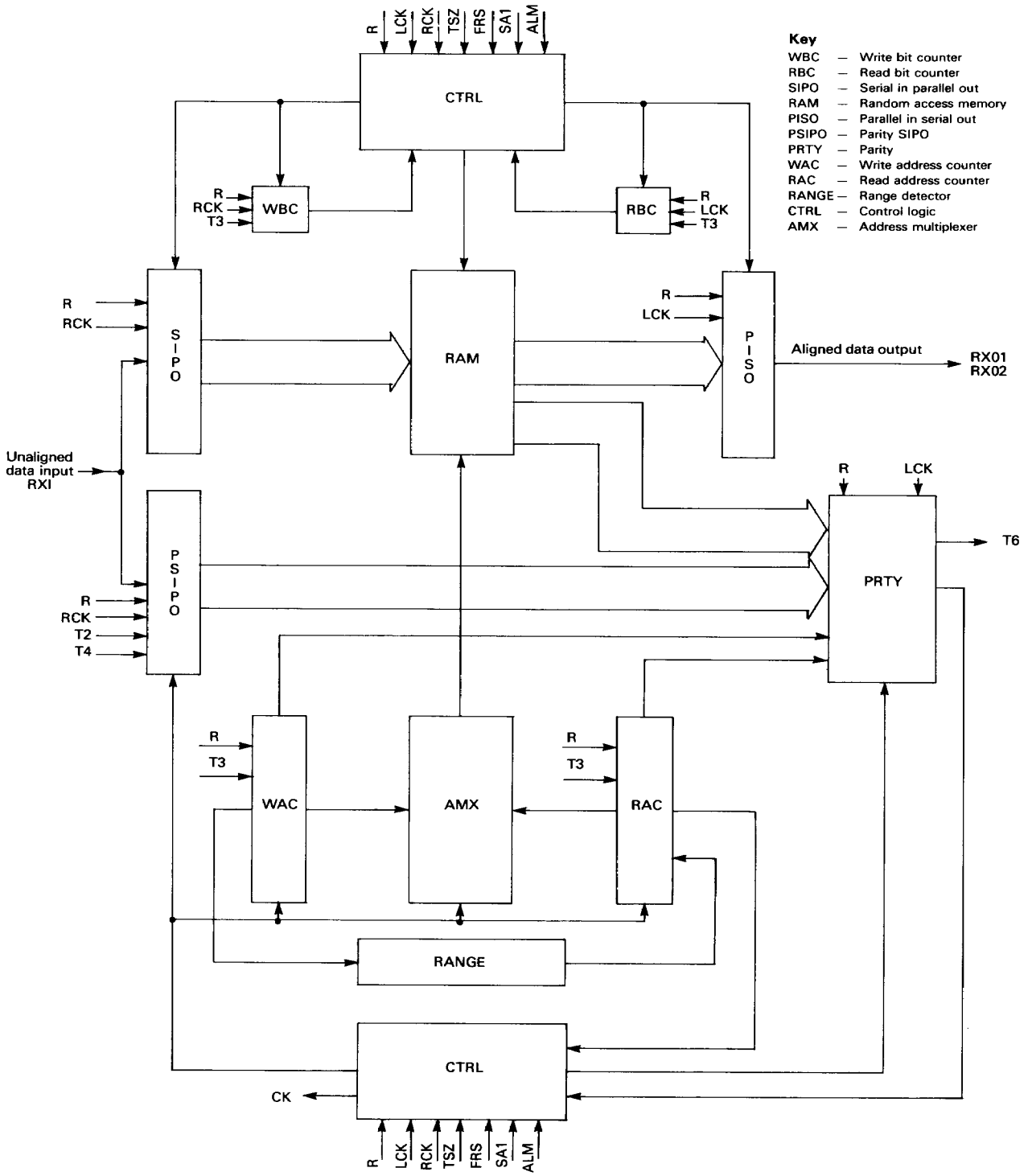
PRELIMINARY DATA

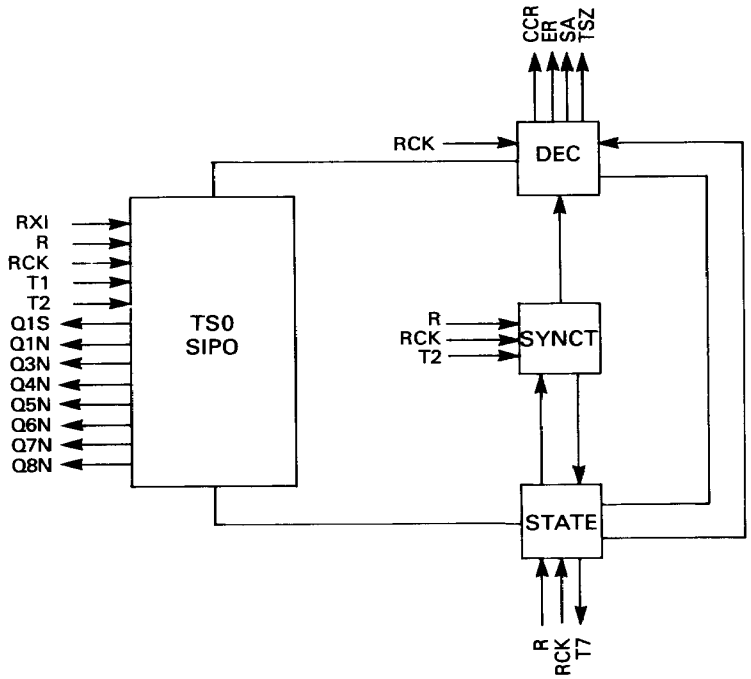
FRAME ALIGNER BLOCK DIAGRAM

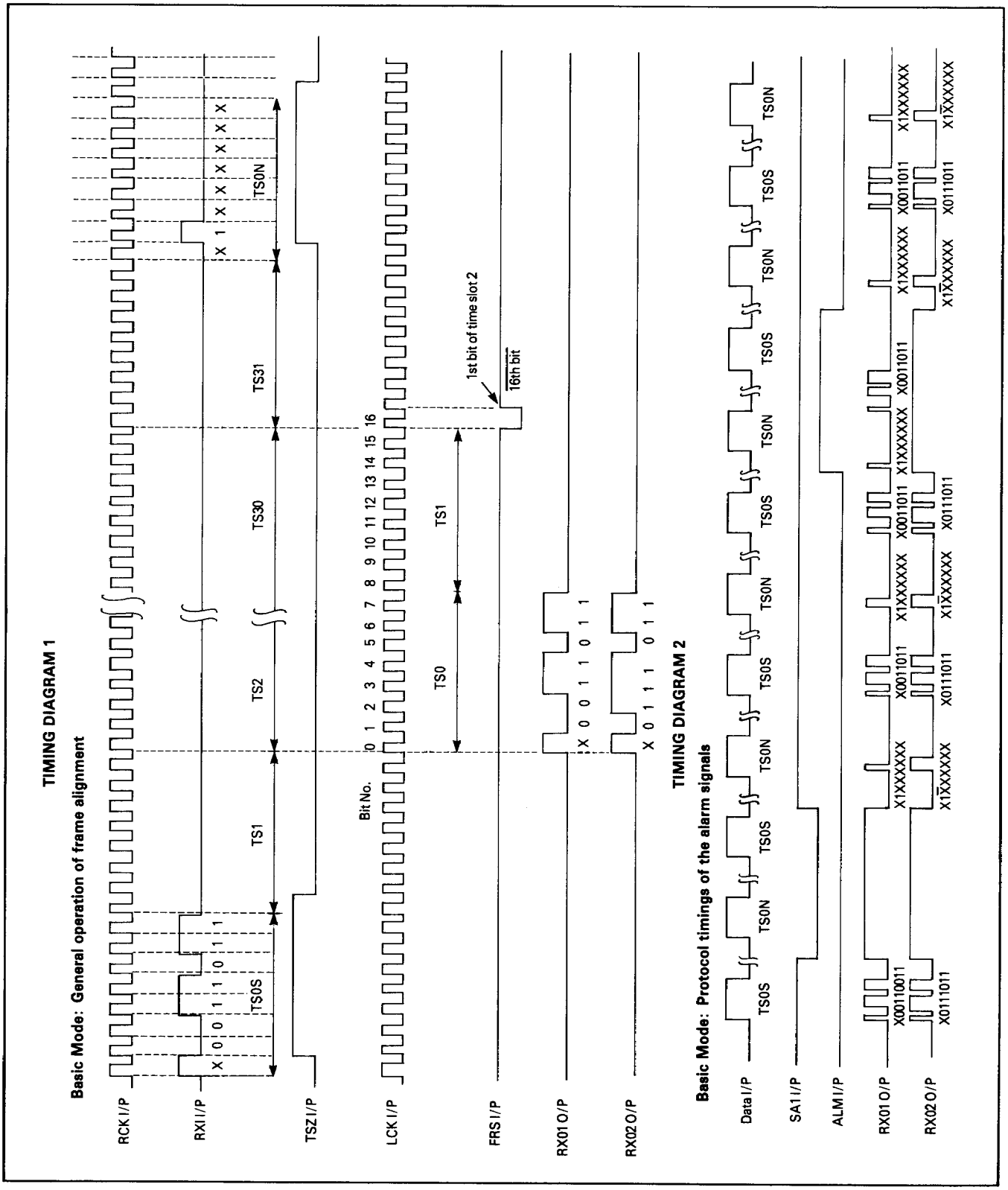


BLOCK DIAGRAM OF THE TS0 RECEIVER

Key

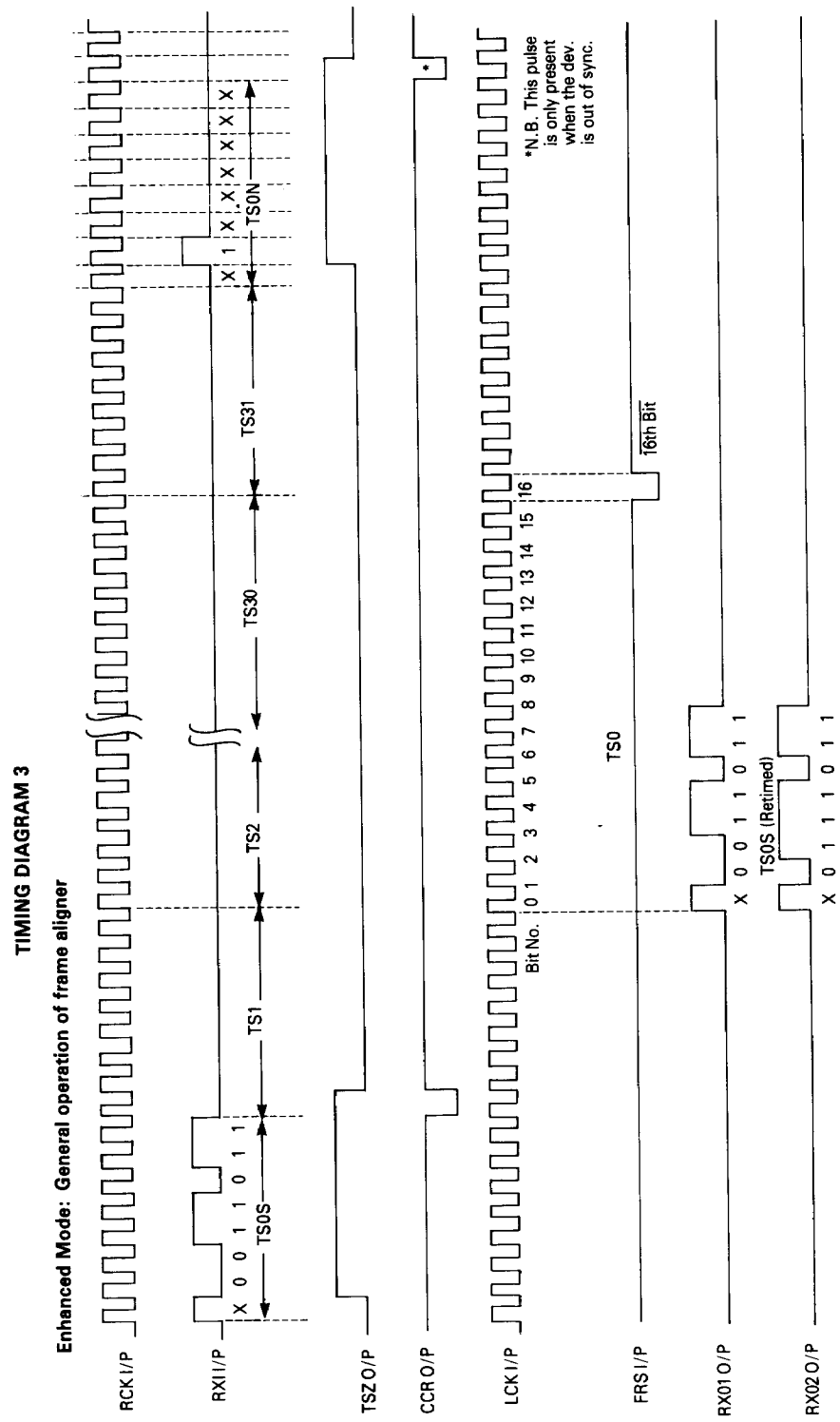
TS0 SIPO	—	Time slot zero to parallel converter
DEC	—	Decoder
SYNCT	—	Sync. counter
STATE	—	Sync. word detector and state control





TIMING DIAGRAM 3

Enhanced Mode: General operation of frame aligner



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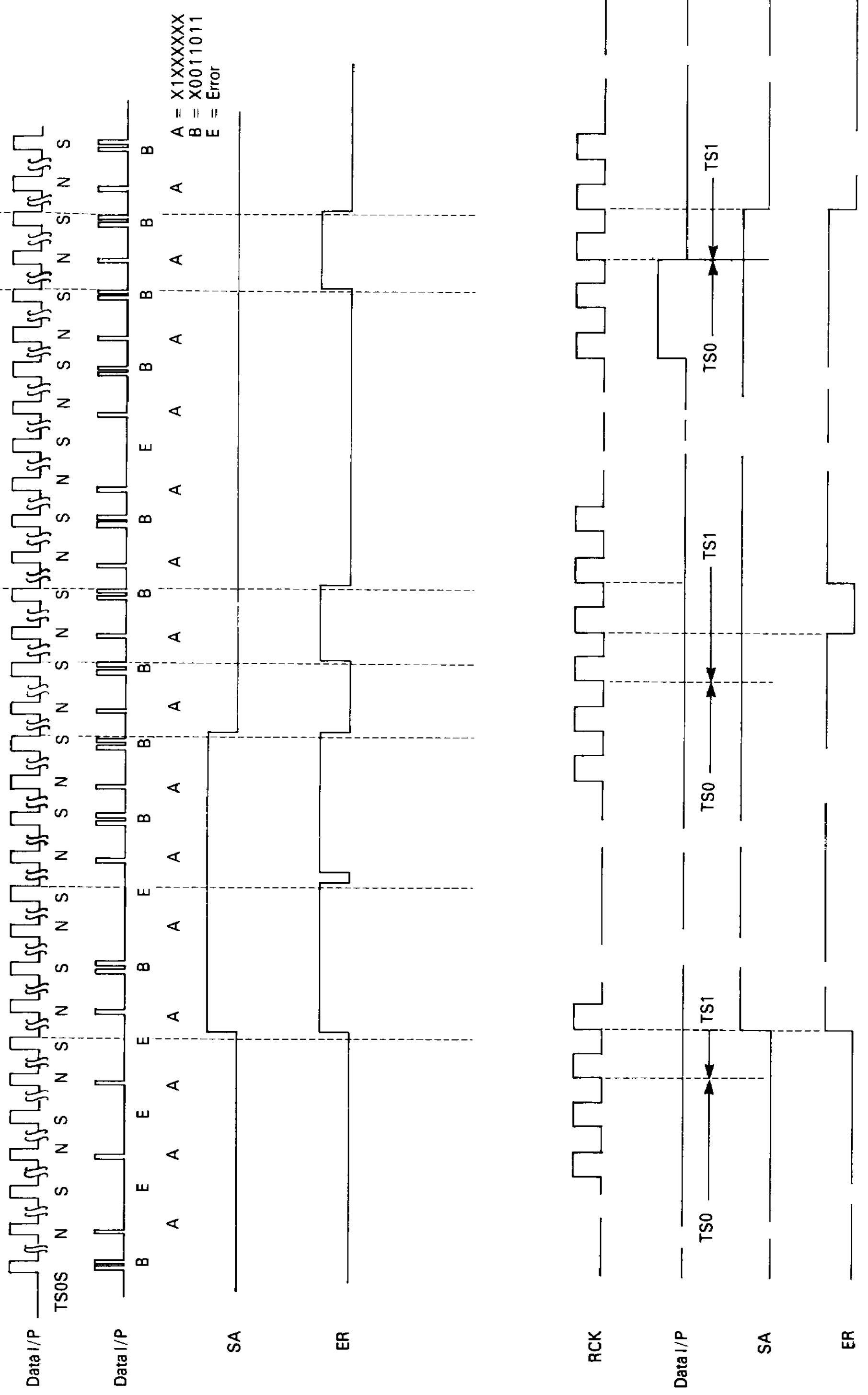
PRELIMINARY DATA

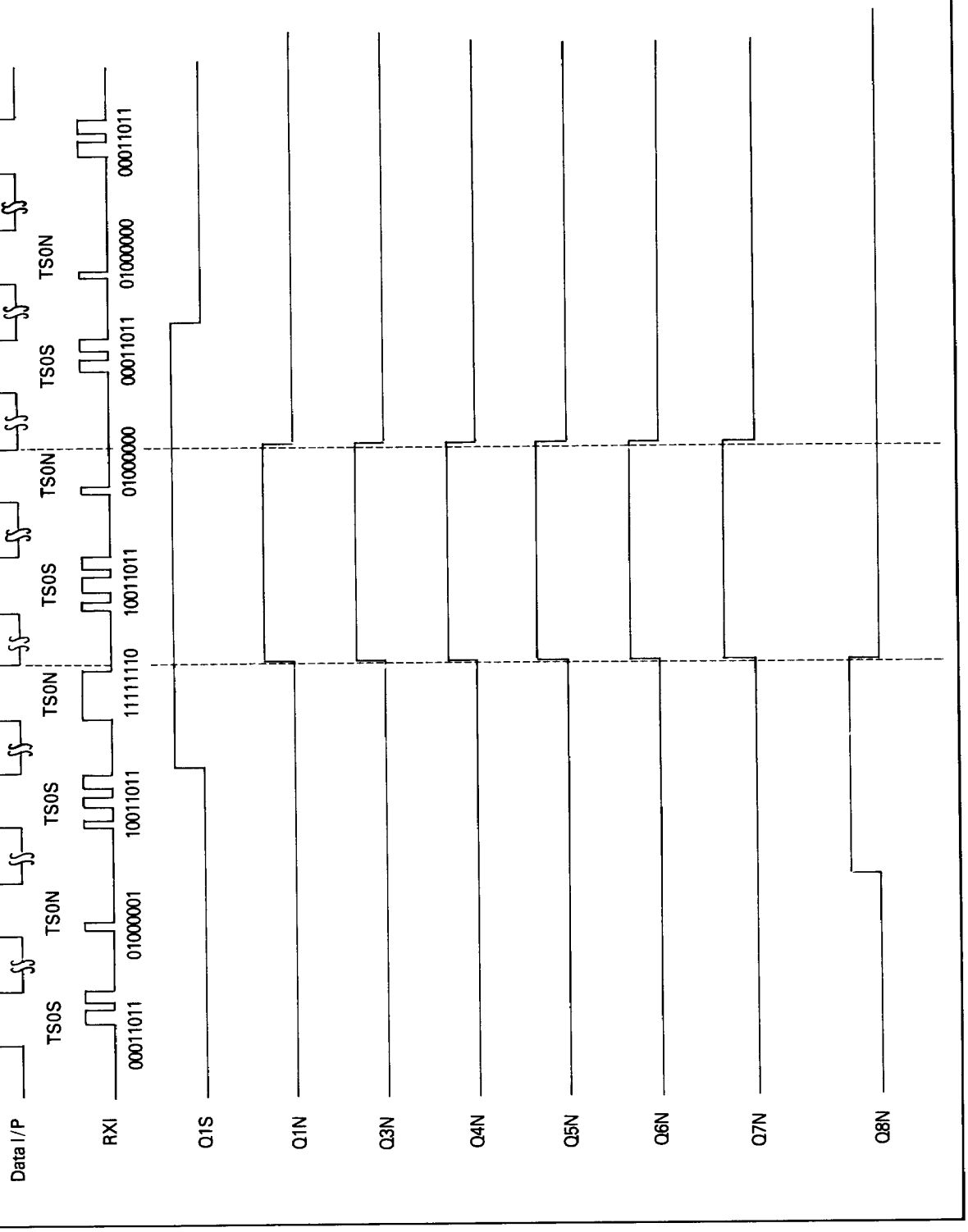


TIMING DIAGRAM 4

Enhanced Mode: Protocol timings of TS0 receiver alarms

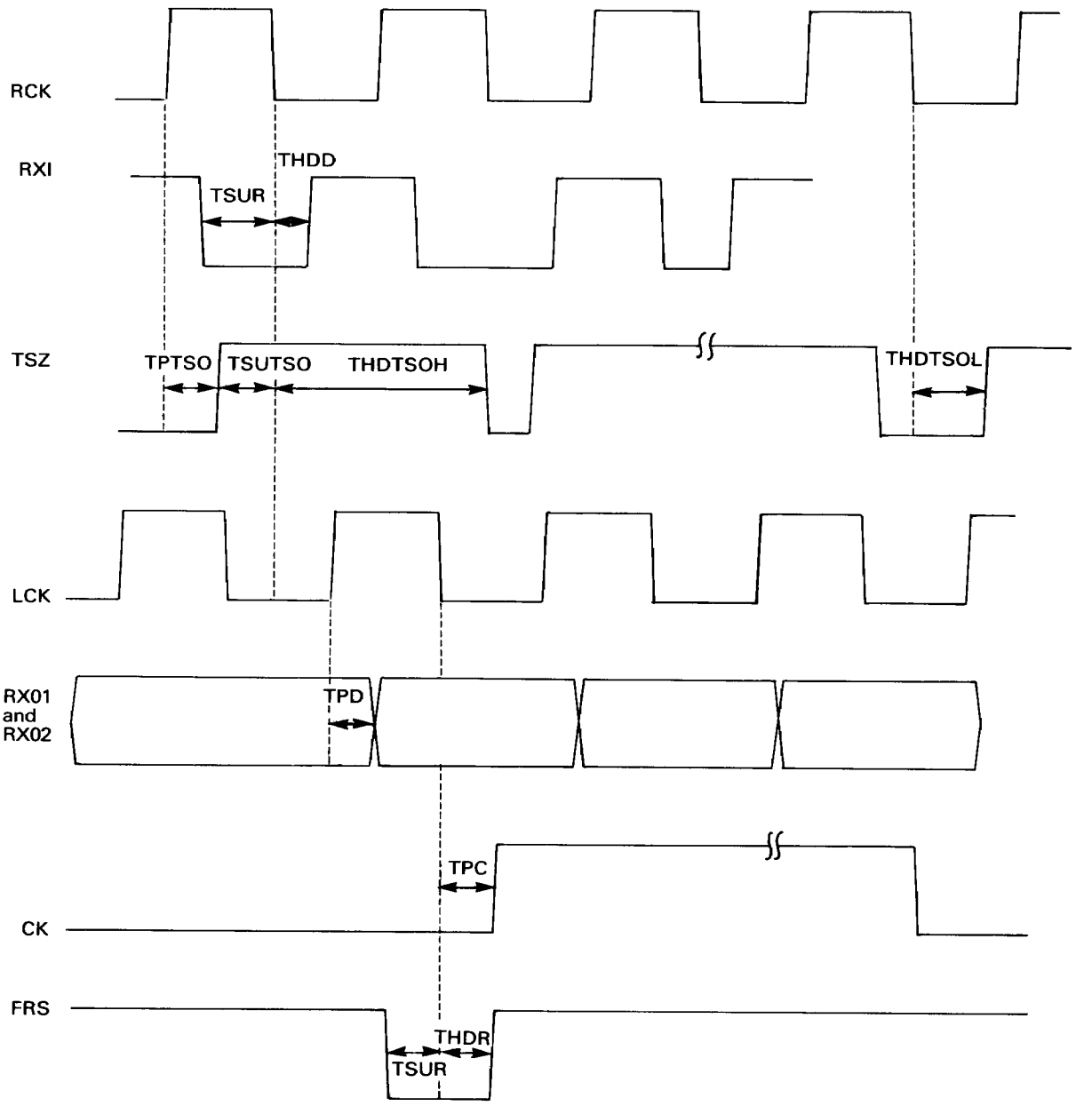
TIMING DIAGRAM 5

Enhanced Mode: Protocol timings of the signal lines

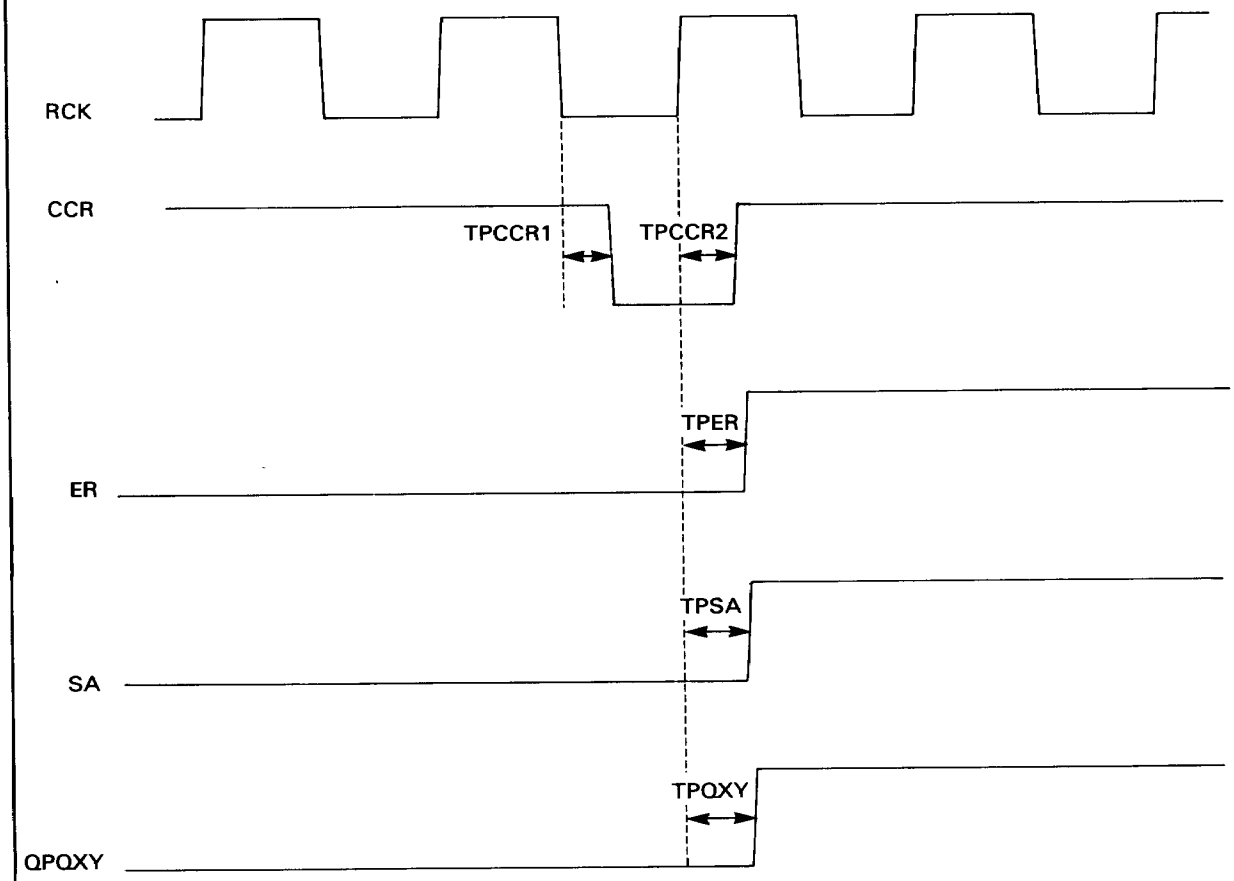


TIMING DIAGRAM 6

Basic and Enhanced Mode Timing Waveforms



TIMING DIAGRAM 7



*N.B. — All timing reference points are measured at 1.6v

Frame Aligner with Optional Time Slot Zero Receiver

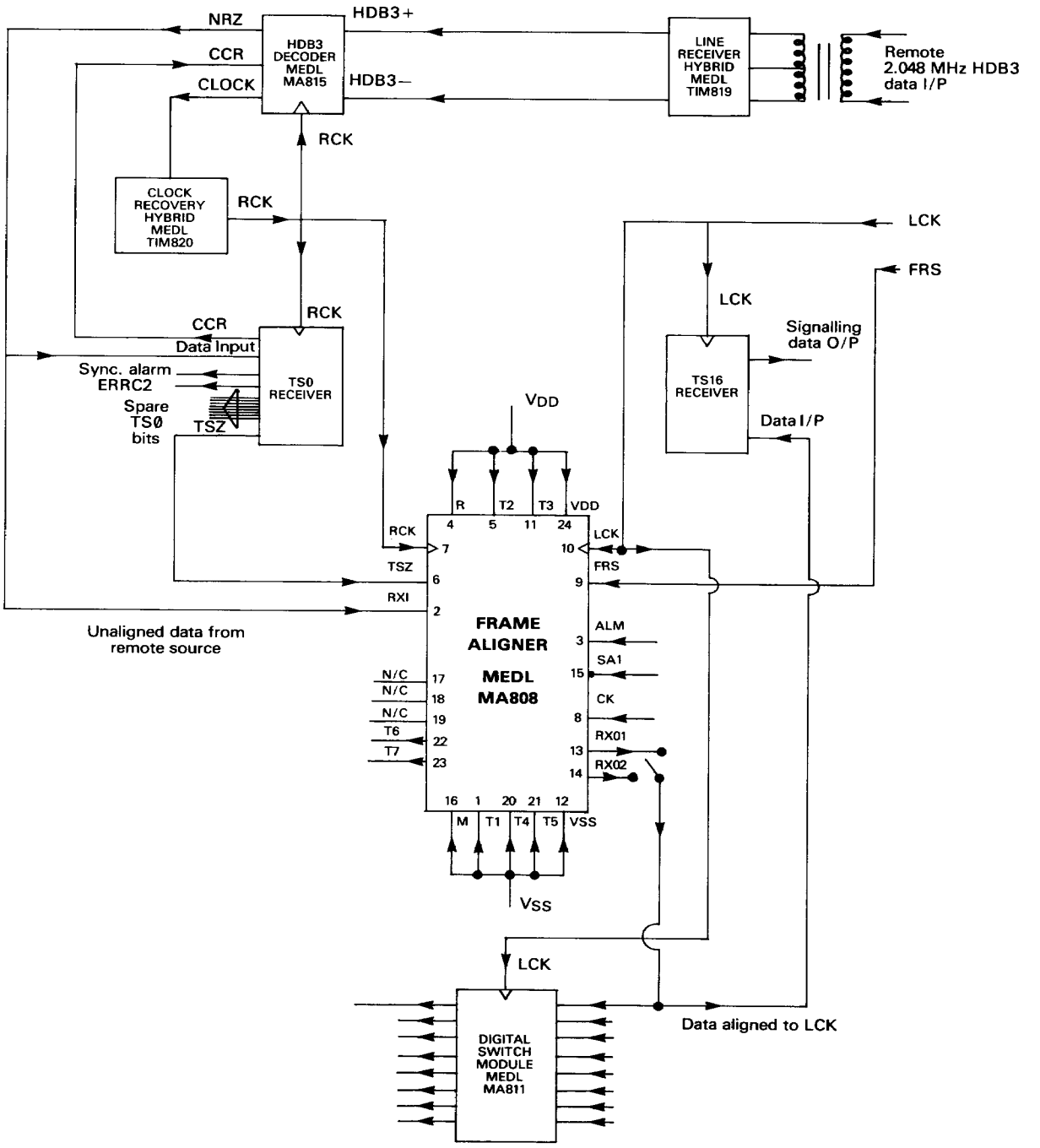
MA808

PRELIMINARY DATA

BLOCK DIAGRAM OF A DIGITAL EXCHANGE

INCORPORATING THE MA808

IN BASIC MODE



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PRELIMINARY DATA

Frame Aligner with Optional Time Slot Zero Receiver

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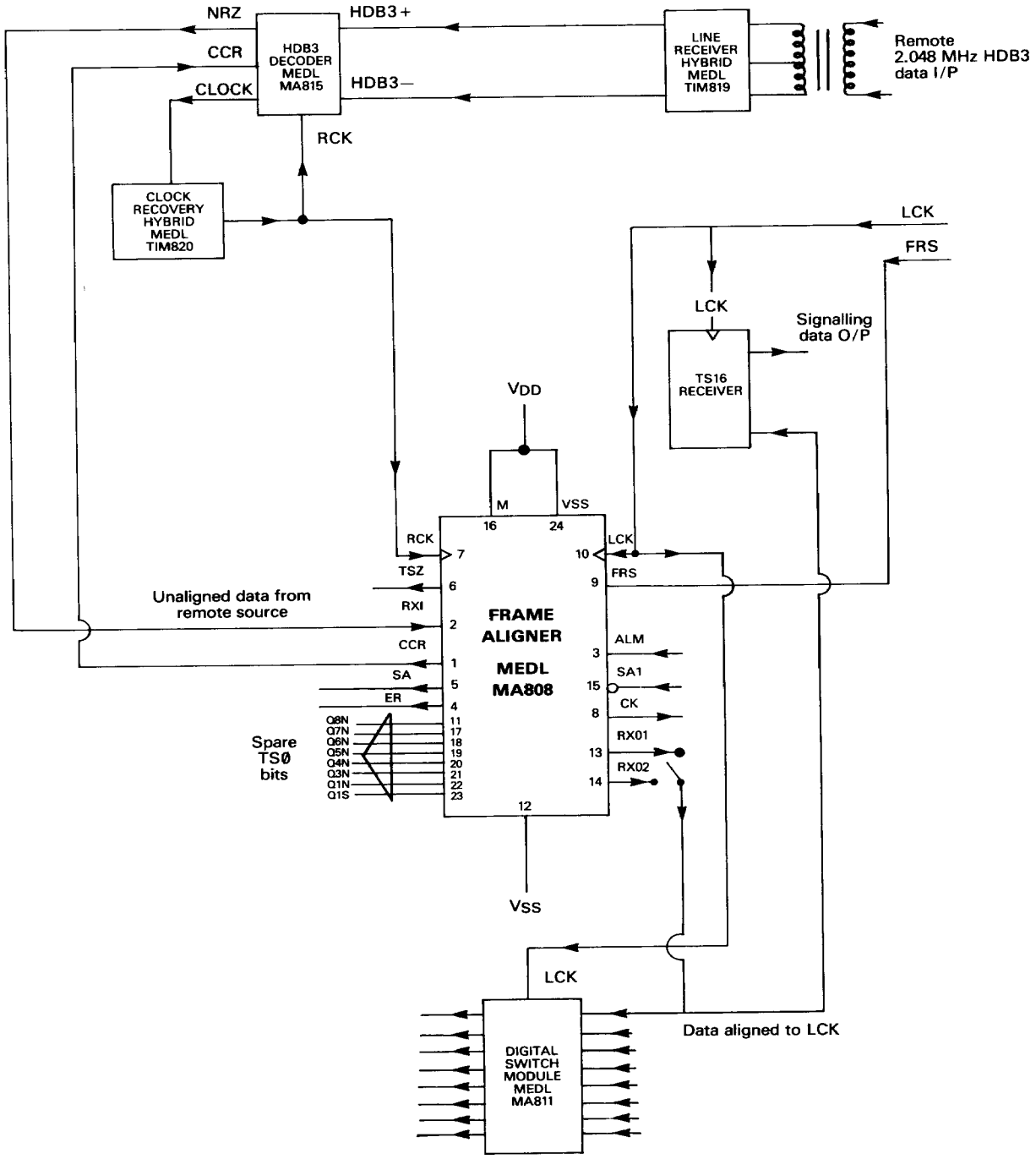
BLOCK DIAGRAM OF A DIGITAL EXCHANGE

INCORPORATING THE MA808

IN ENHANCED MODE



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