TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# JT6J15A-AS

## ROW DRIVER FOR A DOT MATRIX LCD

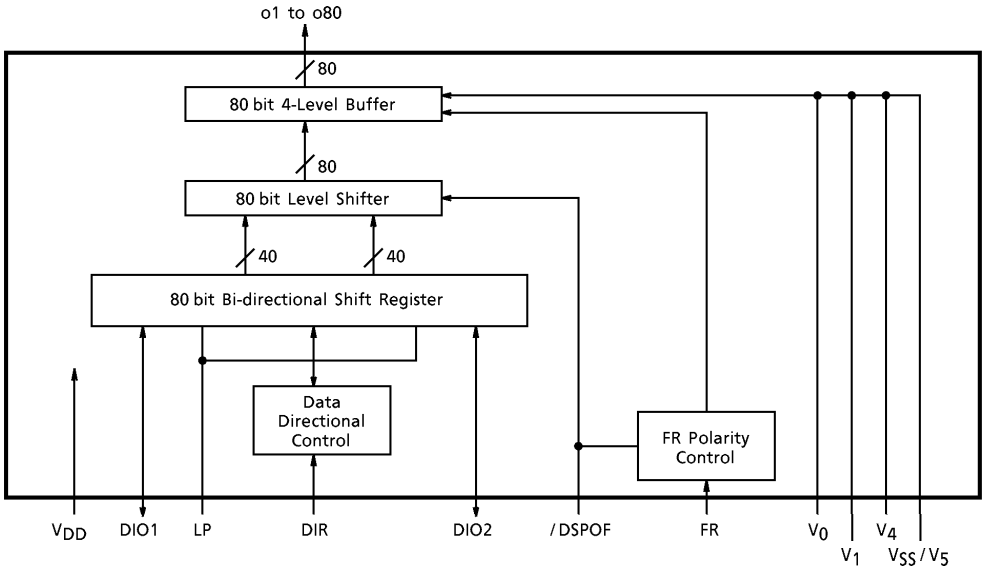
The JT6J15A-AS is a 80-channel-output row driver for a STN dot matrix LCD. The JT6J15A-AS features 28 V LCD drive voltage. The JT6J15A-AS is able to drive LCD panels with a duty ratio of up to 1 / 160.
As the JT6J15A-AS is equipped with a built-in voltage divider resistor, power supply operation amplifier, four and six-fold booster circuit, a contrast control circuit and a booster oscillator (oscillating capacitance is built in, and oscillating resistance is attached externally,) it is easy to structure a low power consumption LCD system by combining it with the JT6J14-AS column driver.

### FEATURES

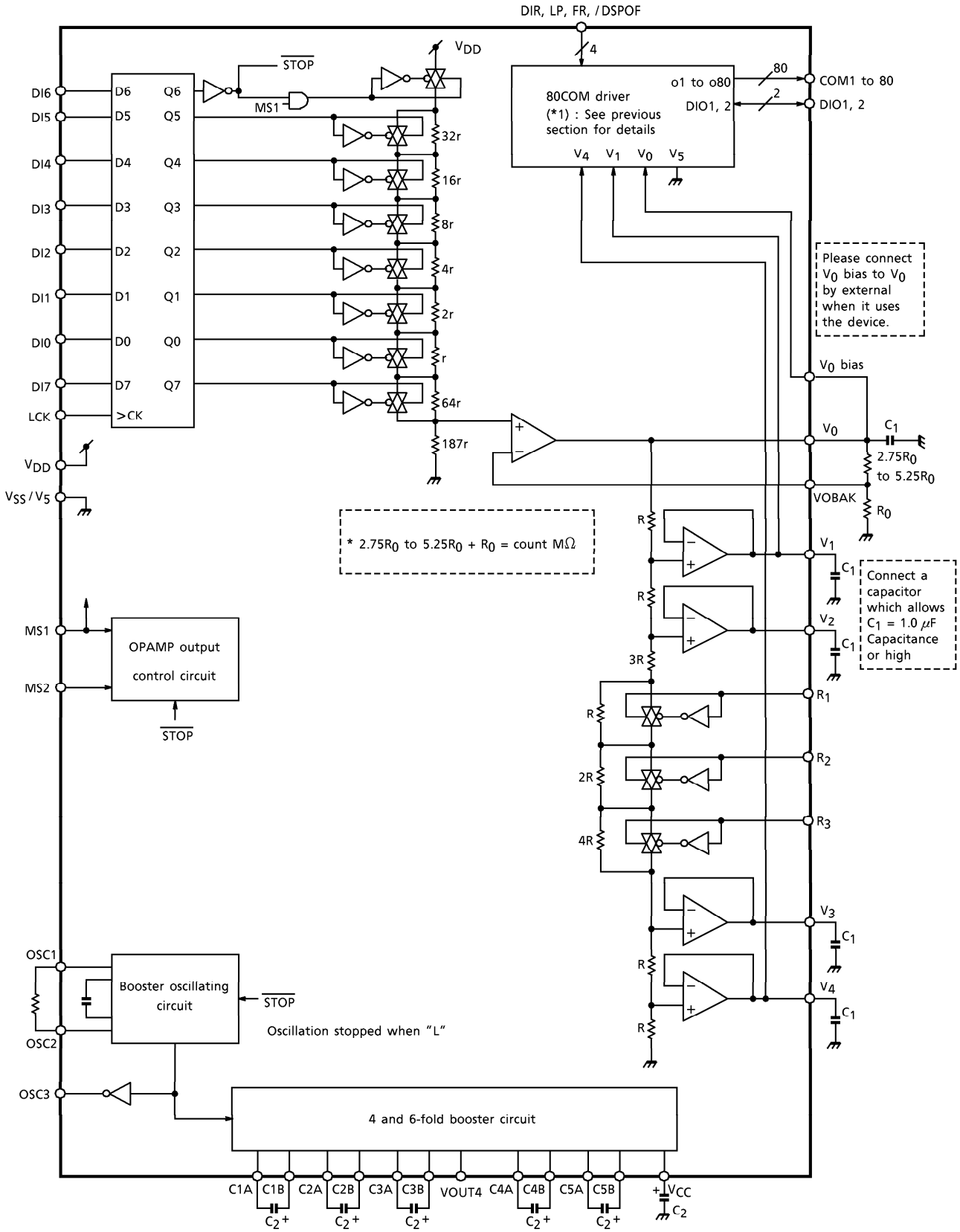
- Display duty application : to 1 / 160
- LCD drive signal : 80
- Data transfer : Two different styles of 1-bit bi-directional can be selected
  ① COM80 ← COM1
  ② COM80 → COM1
- Operating temperature : – 20 to 75°C
- LCD drive output resistance : 1.5 kΩ MAX (Vo = 12.8 V, 1 / 7 to 1 / 14 Bias)
- Display-off function : When / DSPOF is "L", all LCD drive outputs (o1 to o80) remain at the $V_{SS}$ / $V_5$ level
- LCD drive voltage : 11 to 28 V (maximum drive voltage = 30 V)
- Power supply voltage : 2.7 to 5.5 V

**BLOCK DIAGRAM 1**

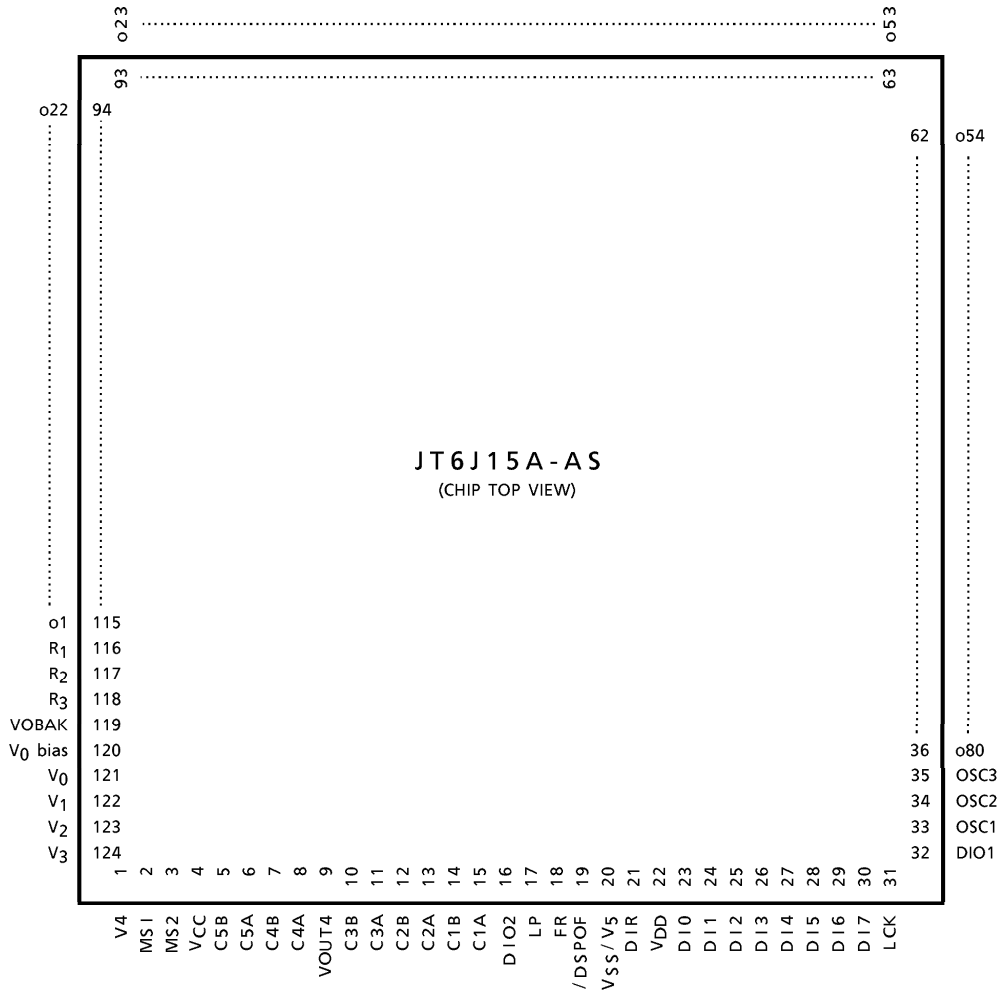
*1···80 COM driver area

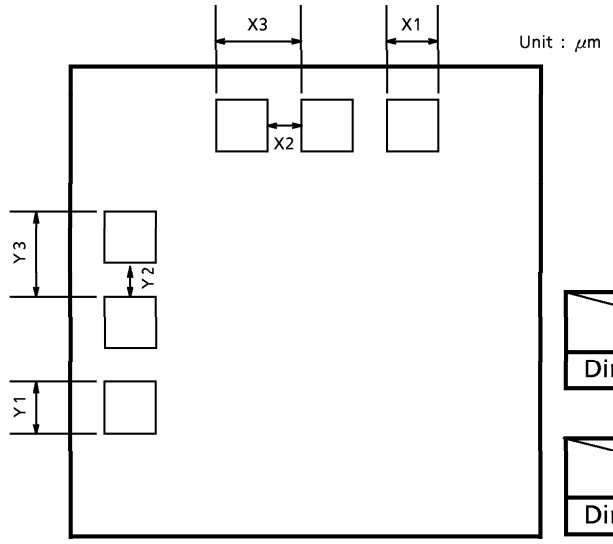


## BLOCK DIAGRAM 2



**PIN ASSIGNMENT**




Unit : $\mu$m

| | X1 | X2 | X3 |
|---|---|---|---|
| Dimensions ($\mu$m) | 100 | 30 | 130 |

| | Y1 | Y2 | Y3 |
|---|---|---|---|
| Dimensions ($\mu$m) | 100 | 30 | 130 |

**PAD COORDINATES**

Scribe width : 80 × 140 $\mu$m

Chip size : 4790 × 4850 $\mu$m (Including scribe width)

Number of PAD : 124 pcs

PAD size : 100 $\mu m^{\square}$

Palette edge coordinates 1 : −2355, −2355
2 : −2355, 2355
3 : 2355, 2355
4 : 2355, −2355

Chip edge coordinates 1 : −2395, −2425
2 : −2395, 2425
3 : 2395, 2425
4 : 2395, −2425

[Unit : $\mu$m]

| No | PAD NAME | X POINT | Y POINT |
|---|---|---|---|
| 1 | $V_4$ | −1950 | −2139 |
| 2 | MS1 | −1820 | −2139 |
| 3 | MS2 | −1690 | −2139 |
| 4 | $V_{CC}$ | −1560 | −2139 |
| 5 | C5B | −1430 | −2139 |
| 6 | C5A | −1300 | −2139 |
| 7 | C4B | −1170 | −2139 |
| 8 | C4A | −1040 | −2139 |
| 9 | VOUT4 | −910 | −2139 |
| 10 | C3B | −780 | −2139 |
| 11 | C3A | −650 | −2139 |
| 12 | C2B | −520 | −2139 |
| 13 | C2A | −390 | −2139 |
| 14 | C1B | −260 | −2139 |
| 15 | C1A | −130 | −2139 |
| 16 | DIO2 | 0 | −2139 |
| 17 | LP | 130 | −2139 |
| 18 | FR | 260 | −2139 |
| 19 | /DSPOF | 390 | −2139 |
| 20 | $V_{SS}$ / $V_5$ | 520 | −2139 |
| 21 | DIR | 650 | −2139 |
| 22 | $V_{DD}$ | 780 | −2139 |
| 23 | DI0 | 910 | −2139 |
| 24 | DI1 | 1040 | −2139 |
| 25 | DI2 | 1170 | −2139 |
| 26 | DI3 | 1300 | −2139 |
| 27 | DI4 | 1430 | −2139 |
| 28 | DI5 | 1560 | −2139 |
| 29 | DI6 | 1690 | −2139 |
| 30 | DI7 | 1820 | −2139 |
| 31 | LCK | 1950 | −2139 |
| 32 | DIO1 | 2139 | −1950 |
| 33 | OSC1 | 2139 | −1820 |

| No | PAD NAME | X POINT | Y POINT |
|---|---|---|---|
| 34 | OSC2 | 2139 | −1690 |
| 35 | OSC3 | 2139 | −1560 |
| 36 | o80 | 2139 | −1430 |
| 37 | o79 | 2139 | −1300 |
| 38 | o78 | 2139 | −1170 |
| 39 | o77 | 2139 | −1040 |
| 40 | o76 | 2139 | −910 |
| 41 | o75 | 2139 | −780 |
| 42 | o74 | 2139 | −650 |
| 43 | o73 | 2139 | −520 |
| 44 | o72 | 2139 | −390 |
| 45 | o71 | 2139 | −260 |
| 46 | o70 | 2139 | −130 |
| 47 | o69 | 2139 | 0 |
| 48 | o68 | 2139 | 130 |
| 49 | o67 | 2139 | 260 |
| 50 | o66 | 2139 | 390 |
| 51 | o65 | 2139 | 520 |
| 52 | o64 | 2139 | 650 |
| 53 | o63 | 2139 | 780 |
| 54 | o62 | 2139 | 910 |
| 55 | o61 | 2139 | 1040 |
| 56 | o60 | 2139 | 1170 |
| 57 | o59 | 2139 | 1300 |
| 58 | o58 | 2139 | 1430 |
| 59 | o57 | 2139 | 1560 |
| 60 | o56 | 2139 | 1690 |
| 61 | o55 | 2139 | 1820 |
| 62 | o54 | 2139 | 1950 |
| 63 | o53 | 1950 | 2139 |
| 64 | o52 | 1820 | 2139 |
| 65 | o51 | 1690 | 2139 |
| 66 | o50 | 1560 | 2139 |

| No | PAD NAME | X POINT | Y POINT |
|---|---|---|---|
| 67 | o49 | 1430 | 2139 |
| 68 | o48 | 1300 | 2139 |
| 69 | o47 | 1170 | 2139 |
| 70 | o46 | 1040 | 2139 |
| 71 | o45 | 910 | 2139 |
| 72 | o44 | 780 | 2139 |
| 73 | o43 | 650 | 2139 |
| 74 | o42 | 520 | 2139 |
| 75 | o41 | 390 | 2139 |
| 76 | o40 | 260 | 2139 |
| 77 | o39 | 130 | 2139 |
| 78 | o38 | 0 | 2139 |
| 79 | o37 | – 130 | 2139 |
| 80 | o36 | – 260 | 2139 |
| 81 | o35 | – 390 | 2139 |
| 82 | o34 | – 520 | 2139 |
| 83 | o33 | – 650 | 2139 |
| 84 | o32 | – 780 | 2139 |
| 85 | o31 | – 910 | 2139 |
| 86 | o30 | – 1040 | 2139 |
| 87 | o29 | – 1170 | 2139 |
| 88 | o28 | – 1300 | 2139 |
| 89 | o27 | – 1430 | 2139 |
| 90 | o26 | – 1560 | 2139 |
| 91 | o25 | – 1690 | 2139 |
| 92 | o24 | – 1820 | 2139 |
| 93 | o23 | – 1950 | 2139 |
| 94 | o22 | – 2139 | 1950 |
| 95 | o21 | – 2139 | 1820 |

| No | PAD NAME | X POINT | Y POINT |
|---|---|---|---|
| 96 | o20 | – 2139 | 1690 |
| 97 | o19 | – 2139 | 1560 |
| 98 | o18 | – 2139 | 1430 |
| 99 | o17 | – 2139 | 1300 |
| 100 | o16 | – 2139 | 1170 |
| 101 | o15 | – 2139 | 1040 |
| 102 | o14 | – 2139 | 910 |
| 103 | o13 | – 2139 | 780 |
| 104 | o12 | – 2139 | 650 |
| 105 | o11 | – 2139 | 520 |
| 106 | o10 | – 2139 | 390 |
| 107 | o9 | – 2139 | 260 |
| 108 | o8 | – 2139 | 130 |
| 109 | o7 | – 2139 | 0 |
| 110 | o6 | – 2139 | – 130 |
| 111 | o5 | – 2139 | – 260 |
| 112 | o4 | – 2139 | – 390 |
| 113 | o3 | – 2139 | – 520 |
| 114 | o2 | – 2139 | – 650 |
| 115 | o1 | – 2139 | – 780 |
| 116 | $R_1$ | – 2139 | – 910 |
| 117 | $R_2$ | – 2139 | – 1040 |
| 118 | $R_3$ | – 2139 | – 1170 |
| 119 | VOBAK | – 2139 | – 1300 |
| 120 | $V_0$ bias | – 2139 | – 1430 |
| 121 | $V_0$ | – 2139 | – 1560 |
| 122 | $V_1$ | – 2139 | – 1690 |
| 123 | $V_2$ | – 2139 | – 1820 |
| 124 | $V_3$ | – 2139 | – 1950 |

**PIN FUNCTIONS**

| PIN NAME | I/O | FUNCTIONS | LEVEL |
|---|---|---|---|
| o1 to o80 | Output | Output for LCD drive signal | $V_0$ to $V_{SS}$/$V_5$ |
| DIO1, DIO2 | I/O | Input/Output for shift data | $V_{DD}$ to $V_{SS}$/$V_5$ |
| LP | Input | (Shift Clock Pulse)<br>Input for shift clock pulse | |
| FR | Input | (Frame)<br>Input for frame signal | |
| DIR | Input | (Direction)<br>Input for data flow direction select | |
| /DSPOF | Input | (Display Off)<br>Display off pin<br>"L" : Display-off mode, (o1 to o80) remain at the $V_{SS}$/$V_5$ level.<br>"H" : Display-on mode, (o1 to o80) are operational. | |
| DI0 to DI7 | Input | Data bus : For contrast control usage<br>Contrast adjustments are variable between 128 stages with the DI0 to DI5 and D17 data.<br>DI6 : When "H": Stops the booster's oscillation frequency and turns the power supply ($V_{DD}$) to the contrast controller off<br>When "L": Operates the booster circuit and contrast controller circuit | |
| LCK | Input | Data bus loading clock<br>Synchronized during rising and loaded internally. | |
| R1 to R3 | Input | Bias set-up pin (bias settings possible between 1/7 and 1/14) | |
| OSC1/OSC2 | Input | Booster oscillation pin<br>Resistors connected to these pins when the internal clock is operating (100 kΩ between OSC1 and OSC2).<br>The clock is input to OSC1 when the external clock is operating. | |
| OSC3 | Output | Booster oscillating output pin<br>The OCS3 pin is connected to another IC's OCS1 when the booster's oscillating frequency is shared with multiple connections. | |
| MS1/MS2 | Input | Master/slave switching pin | |
| CnA to CnB | — | Terminal for connecting external condensers (n = 1 to 5)<br>Connect a booster capacitor which allows about $C_2$ = 3.3 μF capacitance between CnA and CnB. | — |
| VOUT4 | — | Booster voltage output pin (4-fold booster)<br>Connect VOUT4 and $V_{CC}$ when use of 4-fold booster. | |
| $V_{CC}$ | — | LCD drive voltage pin<br>(operation amplifier drive voltage, 6-fold booster terminal) | |
| $V_{DD}$ | — | Power supply for internal logic | |
| $V_{SS}$/$V_5$ | — | Power supply for internal logic | |
| VOBAK | — | Voltage amplifier circuit | |
| $V_0$, $V_1$, $V_2$, $V_3$, $V_4$, $V_0$ bias | — | Power supply for LCD drive circuit<br>Connect an external capacitor which allows $C_1$ = 1.0 μF capacitance or high to AMP output. | |

**RELATIONSHIP BETWEEN FR, DATA INPUT AND OUTPUT LEVELS**

| FR | INPUT DATA (DIO1, DIO2) | / DSPOF | OUTPUT LEVEL |
|---|---|---|---|
| H | L | H | $V_4$ |
| H | H | H | $V_0$ bias |
| L | L | H | $V_1$ |
| L | H | H | $V_{SS}$ / $V_5$ |
| (*) | (*) | L | $V_{SS}$ / $V_5$ |

(*) : Don't Care

**DATA INPUT FORMAT**

| DIR | DATA TRANSFER DIRECTION | DATA INPUT TERMINALS | |
|---|---|---|---|
| | | DIO1 | DIO2 |
| H | o1 → o80 | Input | Output |
| L | o80 → o1 | Output | Input |

**OPERATION AMPLIFIER OUTPUT CONTROL CIRCUIT**

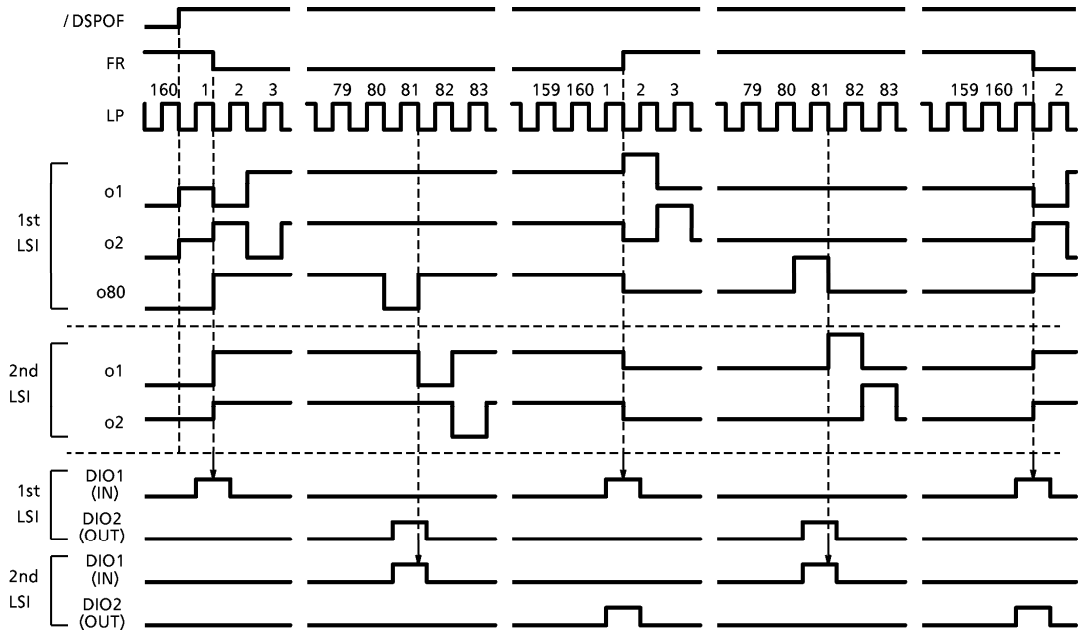
| MS1 | MS2 | / STOP | MODE | BOOSTER OSCILLATIONS | BOOSTER | $V_0$ OUTPUT | $V_1$, $V_4$ OUTPUT | $V_2$, $V_3$ OUTPUT |
|---|---|---|---|---|---|---|---|---|
| L | *1 | L | Slave mode (The booster circuit is driven and $V_{CC}$ voltage generated. $V_0$, $V_1$, $V_2$, $V_3$ and $V_4$ are supplied from an external source) | — | Booster stopped | Output CUT, PD Tr ON | | Output CUT, PD Tr ON |
| | | H | | External clock | Booster operating | Output CUT, PD Tr OFF (supplied from external source) | | Output CUT, PD Tr ON |
| H | L | L | Master mode 1 ($V_0$ is output from the $V_{CC}$ voltage generating through driving the booster circuit. $V_1$, $V_2$, $V_3$ and $V_4$ are supplied from an external source) | Oscillations stopped | Booster stopped | Output CUT, PD Tr ON | Output CUT, PD Tr ON | Output CUT, PD Tr ON |
| | | H | | Oscillations operating | Booster operating | Output ON, PD Tr OFF (supplied to internal / external sources) | Output cut, PD Tr OFF (supplied from external source) | Output CUT, PD Tr ON |
| H | H | L | Master mode 2 $V_0$, $V_1$, $V_2$, $V_3$ and $V_4$ are output from the $V_{CC}$ voltage generating through driving the booster circuit.) | Oscillations stopped | Booster stopped | Output CUT, PD Tr ON | | Output CUT, PD Tr ON |
| | | H | | Oscillations operating | Booster operating | Output ON, PD Tr OFF (supplied to internal / external sources) | | Output ON, PD Tr OFF (supplied to external source) |

PD : Pull Down

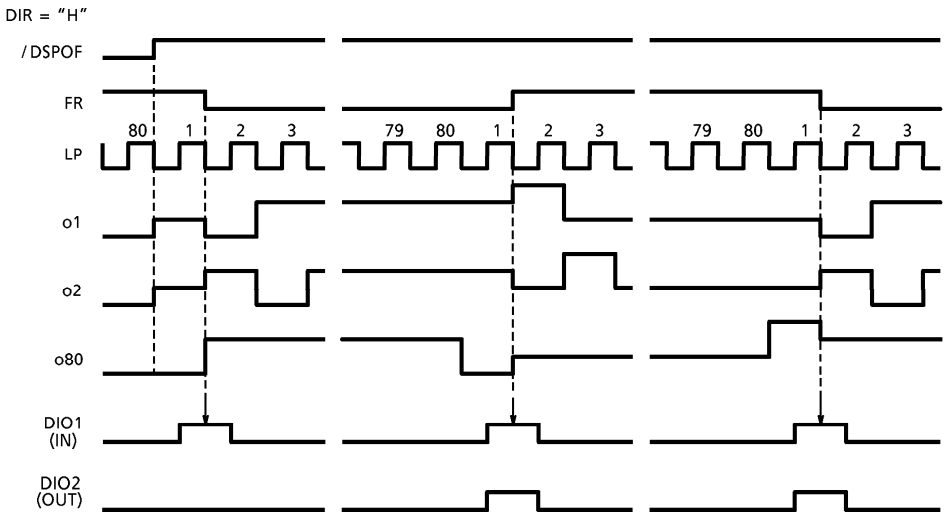
(*1) : Connect to $V_{DD}$ or $V_{SS}$ / $V_5$

**TIMING DIAGRAM**

- Use of JT6J15A-AS 2 pcs (DIR = "H")




- Use of JT6J15A-AS 1 pc (DIR = "H")




**ABSOLUTE MAXIMUM RATINGS**

(Ensure that the following conditions are maintained, $V_0 \geqq V_1 \geqq V_2 \geqq V_3 \geqq V_4 \geqq V_{SS} / V_5 = 0\,V$)

| CHARACTERISTIC | SYMBOL | RATING | UNIT | PIN NAME |
|---|---|---|---|---|
| Power Supply Voltage (1) | $V_{DD}$ | −0.3 to 6.0 | V | $V_{DD}$ |
| Power Supply Voltage (2) | $V_{CC}$ | $V_{DD}$ to 30.0 | V | $V_{CC}$ |
| Input Voltage | $V_{in}$ | −0.3 to $V_{DD}$ + 0.3 | V | (*2) |
| Operating Temperature | $T_{opr}$ | −20 to 75 | °C | — |
| Storage Temperature | $T_{stg}$ | −40 to 125 | °C | — |

(*2) : FR, LP, DIR, DIO1, DIO2, DI0 to DI7, LCK, R1 to R3, /DSPOF

**ELECTRICAL CHARACTERISTICS**

DC CHARACTERISTICS 1

(Unless otherwise noted, $V_{SS}$ = 0 V, $V_{DD}$ = 2.7 to 5.5 V, $V_0$ = 11 to 28 V, Ta = −20 to 75°C)

| ITEM | | SYMBOL | TEST CONDITION | | MIN | TYP. | MAX | UNIT | PIN NAME |
|---|---|---|---|---|---|---|---|---|---|
| Supply Voltage (1) | | $V_{DD}$ | | | 2.7 | 5.0 | 5.5 | V | $V_{DD}$ |
| Supply Voltage (2) | | $V_0$ | $V_{CC} \geqq V0$ | | 11 | — | 28 | V | $V_0$ |
| Supply Voltage (3) | | $V_{CC}$ | $V_{CC} \geqq V0$ | | 11 | — | 28 | V | $V_{CC}$ |
| Input Voltage | "H" Level | $V_{IH}$ | | | 0.8 $V_{DD}$ | — | $V_{DD}$ | V | (*3) |
| | "L" Level | $V_{IL}$ | | | 0 | — | 0.2 $V_{DD}$ | | |
| Output Voltage | "H" Level | $V_{OH}$ | $I_{OH}$ = −0.5 mA | | $V_{DD}$ − 0.5 | — | $V_{DD}$ | V | DIO1, DIO2 |
| | "L" Level | $V_{OL}$ | $I_{OL}$ = 0.5 mA | | 0 | — | 0.5 | | |
| Output Resistance | "H" Level | $R_{OH}$ | $V_{OUT} = V_0$ − 0.5 V (*4) | | — | — | 1.5 | kΩ | o1 to o80 |
| | "M" Level | $R_{OM}$ | $V_{OUT} = V_1 \pm 0.5$ V (*4) | | — | — | 1.5 | | |
| | | $R_{OM}$ | $V_{OUT} = V_4 \pm 0.5$ V (*4) | | — | — | 1.5 | | |
| | "L" Level | $R_{OL}$ | $V_{OUT} = V_{SS} / V_5$ + 0.5 V (*4) | | — | — | 1.5 | | |
| Input Current | | IIL1 | $V_{IN}$ = 0 to $V_{DD}$ | | −1.0 | — | 1.0 | μA | (*3) |
| Output Voltage (with a 4-fold booster) | | $V_{O1}$ | $V_{DD}$ = 5.0 V (*5) | | 17.64 | | | V | $V_{CC}$ |
| Output Voltage (with a 6-fold booster) | | $V_{O2}$ | $V_{DD}$ = 3.0 V (*5) | | 14.0 | | | | |
| Current Consumption | | $I_{DD}$ OPE | VDD = 5.0 V | When operating (*6) | | 1.1 | 1.5 | mA | $V_{DD}$ |
| | | | $V_{DD}$ = 3.0 V | When operating (*7) | | 1.2 | 1.8 | | |
| | | $I_{DD}$ LEAK | $V_{DD}$ = 5.5 V | When no operating | | | 1.0 | μA | |
| | | $I_0$ bias OPE | $V_0$ = 15.0 V | When operating (*8) | | 10 | 25 | | $V_0$ bias |
| | | $I_{CC}$ LEAK | | When no operating (*9) | | | 1.0 | | $V_{CC}$ |

(*3) : FR, LP, DIR, DIO1, DIO2, DI0 to DI7, LCK, R1 to R3, /DSPOF

(*4) : $V_0$ = 12.8 V, 1/7 to 1/14 bias

(*5) : ILoad = 450 μA, external $C_2$ = 3.3 μF, when using COM 1 pc Ta = 25°C, OP-AMP ON

(*6) : Oscillation resistance = 100 kΩ, DC/DC ON, OP-AMP ON, 1/10 bias, contrast MAX
fLP = 11.2 kHz, fFR = 35 Hz, fFP = 70 Hz, $V_{DD}$ = 5.0 V, 4 booster, no load

(*7) : Oscillation resistance = 100 kΩ, DC/DC ON, OP-AMP ON, 1/10 bias, contrast MAX
fLP = 11.2 kHz, fFR = 35 Hz, fFP = 70 Hz, $V_{DD}$ = 3.0 V, 6 booster, no load

(*8) : LCD drive current : fFR = 35 Hz, fLP = 11.2 kHz, fFP = 70 Hz, 1/10 bias, no load,
MS1 = "L", /STOP = "L"

(*9) : MS1 = "L", /STOP = "L"
$f_{FP}$ : Screen switching frequency

DC CHARACTERISTICS 2

LOAD REGULATIONS CHARACTERISTICS 1 ··· no load / MAX load Offset

TEST CONDITIONS : $V_{CC}$ = 18 V (Outside applied voltage), Contrast = 62 (DI1 to DI5 = "H", DI0, DI7 = "L"), External capacitor for AMP : $C_1$ = 1.0 $\mu$F
Gain Resistance = 4 times ($3R_0$, $R_0$), 1 / 10 bias, $V_{DD}$ = 5.0 V, Ta = – 20 to 75 °C,
The $V_1$ to $V_4$ OFFSET spec is defined toward the ideal voltage calculated from the $V_0$ voltage.

OFFSET SPECIFIED VALUE

| | NO LOAD | | MAX LOAD | | MAX LOAD (REVERSE ELECTRIC CURRENT) | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_0$ | 14.6 | 15.6 | 14.50 | 15.50 | — | — | V |
| $V_1$ | – 100 | 90 | – 110 | 75 | – 110 | 110 | mV |
| $V_2$ | – 65 | 65 | – 50 | 75 | – 110 | 110 | mV |
| $V_3$ | – 70 | 70 | – 85 | 50 | – 110 | 110 | mV |
| $V_4$ | – 55 | 50 | – 45 | 65 | – 110 | 110 | mV |
| X | – 220 | 190 | – 255 | 145 | — | — | mV |
| Y | – 120 | 130 | – 170 | 85 | — | — | mV |
| $\Delta V$ | – 210 | 190 | – 300 | 120 | — | — | mV |

LOAD CONDITIONS

| | NO LOAD | MAX LOAD | MAX LOAD (REVERSE ELECTRIC CURRENT) | UNIT |
|---|---|---|---|---|
| $I_0$ | 0 | – 300 | — | $\mu$A |
| $I_1$ | 0 | – 50 | 50 | $\mu$A |
| $I_2$ | 0 | 200 | – 100 | $\mu$A |
| $I_3$ | 0 | – 200 | 100 | $\mu$A |
| $I_4$ | 0 | 50 | – 50 | $\mu$A |

Non-lighting BIAS

$X = (V_1 - V_2) - (V_0 - V_1)$

$Y = (V_3 - V_4) - (V_4 - V_{SS})$

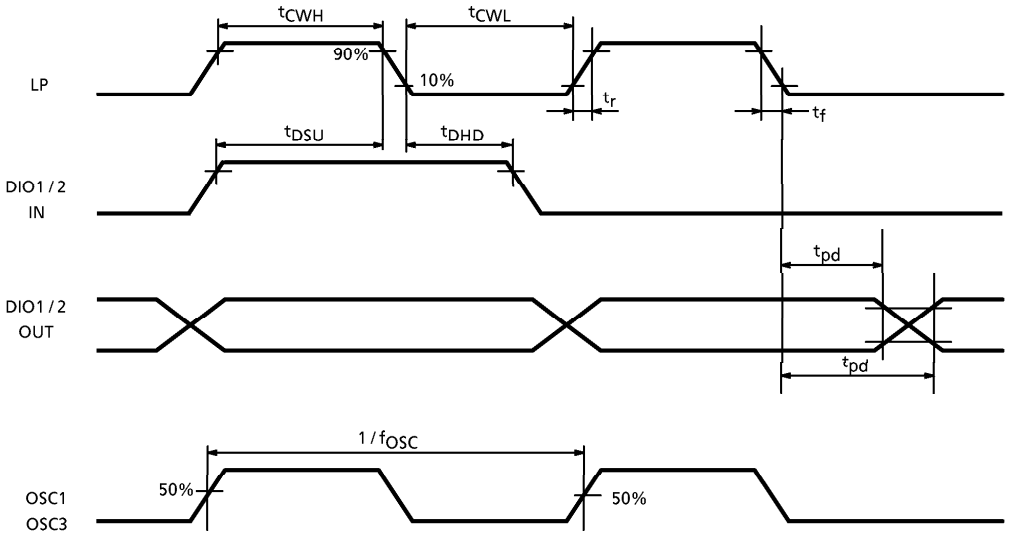
VOM balance

$\Delta V = X + Y$

$V_0$ to $V_4$ are specified as follows
When the $V_0$ voltage is set to the maximum voltage for the contrast with the DI0 to DI7 data bus set to "H".

| BIAS SET-UP VALUE | $R_1$ | $R_2$ | $R_3$ | $V_1$ | $V_2$ | $V_3$ | $V_4$ |
|---|---|---|---|---|---|---|---|
| 1 / 7 | H | H | H | 6 / 7V0 | 5 / 7V0 | 2 / 7V0 | 1 / 7V0 |
| 1 / 8 | L | H | H | 7 / 8V0 | 6 / 8V0 | 2 / 8V0 | 1 / 8V0 |
| 1 / 9 | H | L | H | 8 / 9V0 | 7 / 9V0 | 2 / 9V0 | 1 / 9V0 |
| 1 / 10 | L | L | H | 9 / 10V0 | 8 / 10V0 | 2 / 10V0 | 1 / 10V0 |
| 1 / 11 | H | H | L | 10 / 11V0 | 9 / 11V0 | 2 / 11V0 | 1 / 11V0 |
| 1 / 12 | L | H | L | 11 / 12V0 | 10 / 12V0 | 2 / 12V0 | 1 / 12V0 |
| 1 / 13 | H | L | L | 12 / 13V0 | 11 / 13V0 | 2 / 13V0 | 1 / 13V0 |
| 1 / 14 | L | L | L | 13 / 14V0 | 12 / 14V0 | 2 / 14V0 | 1 / 14V0 |

**AC CHARACTERISTICS 1**

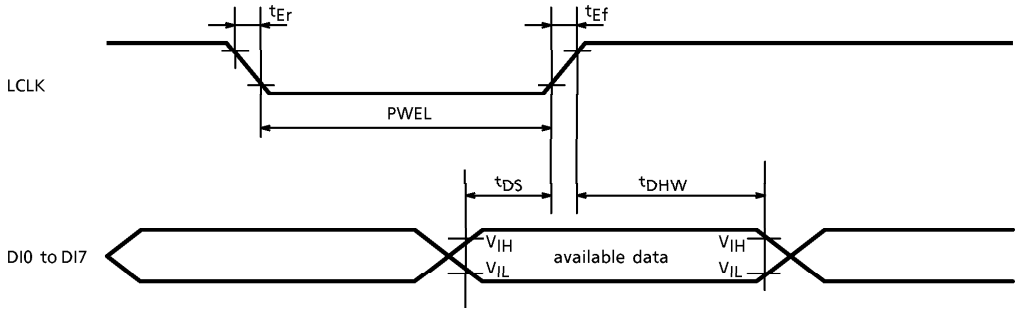



TEST CONDITIONS : $t_C$ (one LP signal cycle) = $t_{CWH} + t_{CWL} + t_r + t_f$
(Unless otherwise noted, $V_{SS}$ = 0 V, $V_{DD}$ = 2.7 to 5.5 V, $V_{CC}$ = 11 to 28 V, Ta = −20 to 75°C)

| ITEM | SYMBOL | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|
| LP Pulse Width | $t_{CWH}$ | LP | 30 | — | — | ns |
| | $t_{CWL}$ | LP | 1 | — | — | μs |
| Data Set-up Time | $t_{DSU}$ | DIO1, DIO2 | 30 | — | — | ns |
| Data Hold Time | $t_{DHD}$ | DIO1, DIO2 | 5 | — | — | |
| LP Rise / Fall Time | $t_r$, $t_f$ | LP, FR, DIO1, DIO2 | — | — | 50 | |
| Output Delay Time (*11) | tpd | DIO1, DIO2 | 20 | — | 500 | |
| Oscillating Frequency | $f_{OSC}$ | OSC1 (*12) | 25.5 | — | 42.5 | kHz |
| External Clock Frequency | | OSC3 | 25.5 | — | 42.5 | |

(*11) : $C_L$ = 10 pF
(*12) : External resistance = 100 kΩ (between OSC1 and OSC2)

**AC CHARACTERISTICS 2**

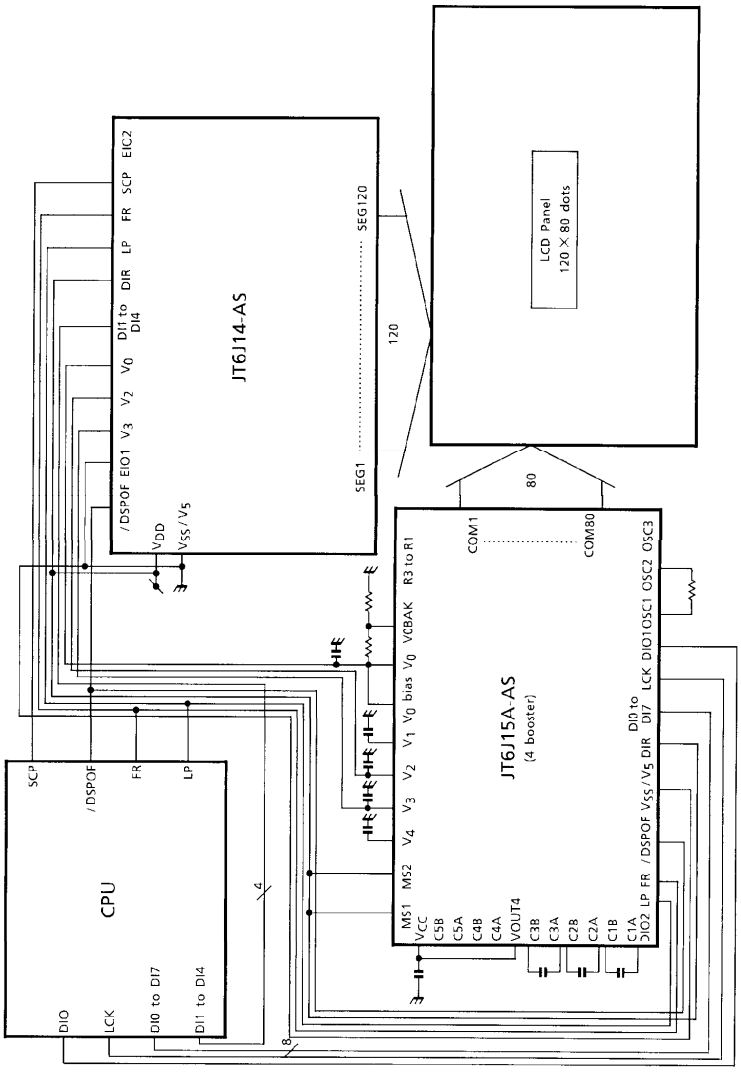



TEST CONDITIONS 1
(Unless otherwise noted, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 V ± 10%, $V_{CC}$ = 11 to 28 V, Ta = −20 to 75°C)

| ITEM | SYMBOL | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|
| Enable Rise / Fall Time | $t_{Er}$ / $t_{Ef}$ | | | | 25 | ns |
| Enable Pulse Width | PWEL | | 60 | | | ns |
| Data Set-up Time | $t_{DS}$ | | 60 | | | ns |
| Data Hold Time | $t_{DHW}$ | | 10 | | | ns |

TEST CONDITIONS 2
(Unless otherwise noted, $V_{SS}$ = 0 V, $V_{DD}$ = 5.0 V ± 10%, $V_{CC}$ = 11 to 28 V, Ta = −20 to 75°C)

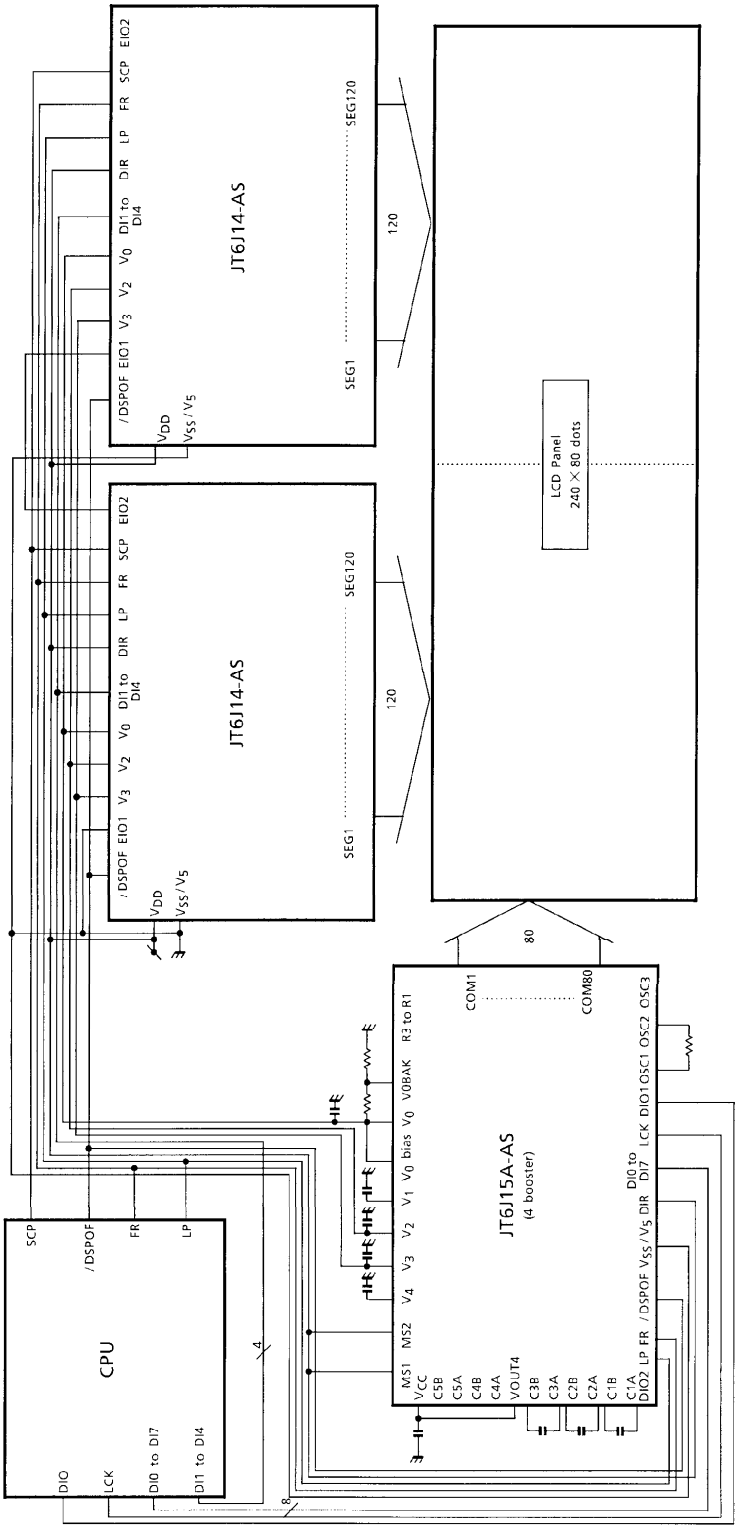
| ITEM | SYMBOL | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|
| Enable Rise / Fall Time | $t_{Er}$ / $t_{Ef}$ | | | | 20 | ns |
| Enable Pulse Width | PWEL | | 60 | | | ns |
| Data Set-up Time | $t_{DS}$ | | 60 | | | ns |
| Data Hold Time | $t_{DHW}$ | | 10 | | | ns |



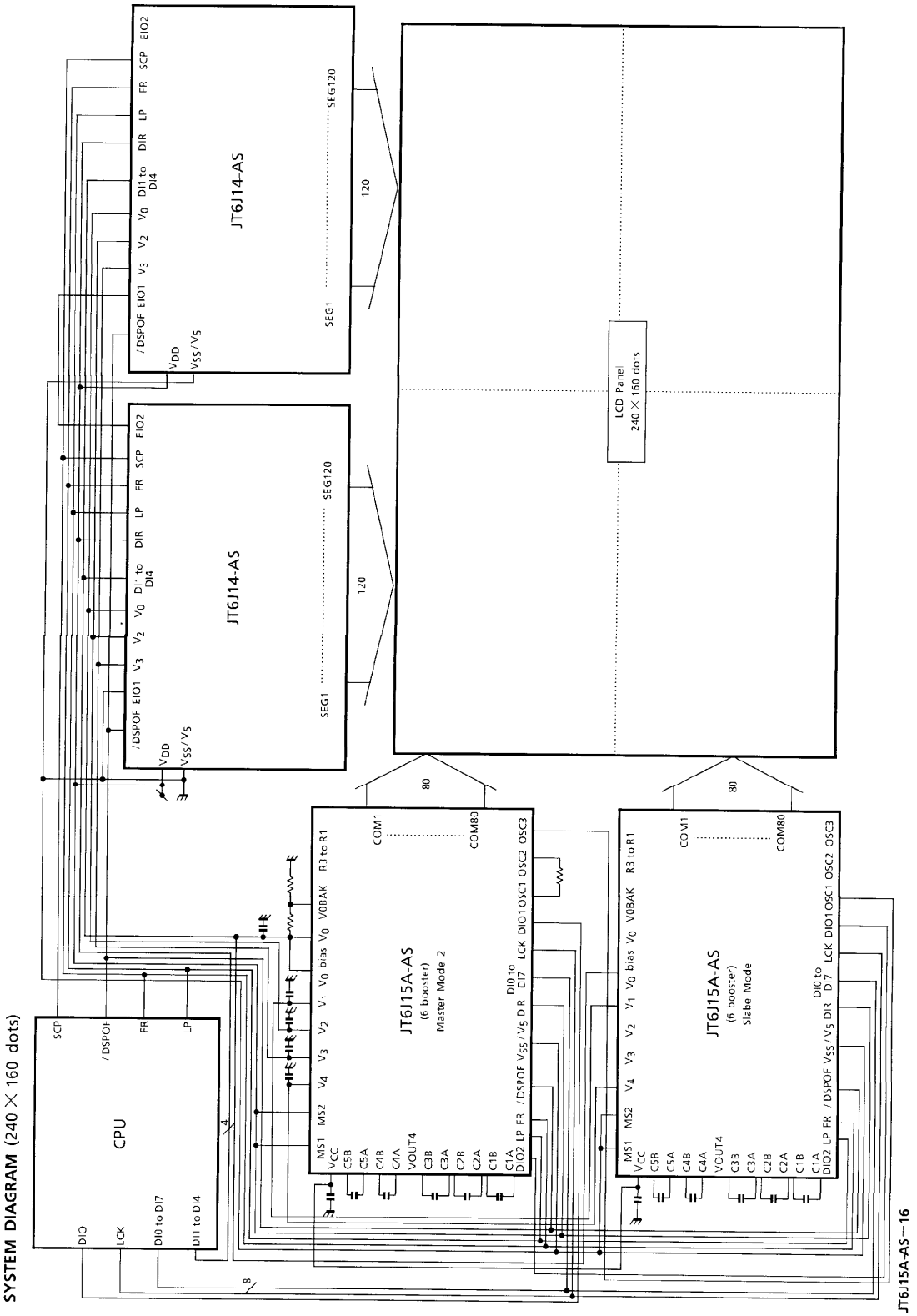

SYSTEM DIAGRAM (120 × 80 dots)

JT6J15A-AS-14

SYSTEM DIAGRAM (240 × 80 dots)




JT6J15A-AS—15


SYSTEM DIAGRAM (240 × 160 dots)
CPU
SCP
/DSPOF
FR
LP
DIO
LCK
DI0 to DI7
DI1 to DI4
JT6J14-AS
/DSPOF EIO1 V3 V2 V0 DI1 to DI4 DIR LP FR SCP EIO2
VDD
VSS/V5
SEG1
SEG120
120
JT6J15A-AS
(6 booster)
Master Mode 2
Slabe Mode
MS1 MS2 V4 V3 V2 V1 V0 bias V0 V0BAK R3 to R1
VCC C5R C5A C4B C4A VOUT4 C3B C3A C2B C2A C1B C1A
DIO2 LP FR /DSPOF VSS/V5 DR DI0 to DI7 LCK DIO1 OSC1 OSC2 OSC3
COM1
COM80
80
LCD Panel
240 × 160 dots
4
8
JT6J15A-AS-16