Semiconductors for TV Tuners
–
The New EasyLink Concept

Issue: 12. 95

Table of Contents

Introduction

This application note describes semiconductor components TEMIC produces for TV- and VCR tuners.

The various product groups are presented in the following three chapters.

- The new MOSMIC families replacing the MOSFET prestages
- The TV mixer families
- The PLL families

The term FAMILY is used for a group of components with similar pinning or functional content.

Each of the main chapters mentioned above contains a short overview, followed by information not given by the data sheet, hints how to simplify the development of a TV tuner and references to known weak points of applications. The chapters may be read separately. They contain all necessary information. References to other chapters are marked by notes (see „Appendix“).

The chapter „The New EasyLink Concept“ introduces a new concept of controlling the tuner by the PLL, the so-called EasyLink Concept.

The appendix contains a description of measurement and design procedures. The respective results are used and given below.

Basic literature, CAD tools and a list of the abbreviations used are given at the end.

The MOSMIC Preamplifier

Overview

The first generation of TEMIC MOSMICs[1] (MOS Monolithic Integrated Circuits) with a transconductance of 24 mS can be thought of as a BF998 MOSFET surrounded by some special components. These fulfill the following tasks:

- Biasing the MOSMIC
- Shifting the pinch-off voltage
- Keeping the drain current to a nearly constant level when reducing the gain

Though this new device is an IC, its handling and features are comparable to the BF998. Exceptions are:

- It is not allowed to change the biasing
- Gate 2 is used only for AGC purposes
- The maximum G2 voltage is lower compared to a MOSFET.

Table 1. The MOSMIC families

Type	V_S	F/ dB @ 800 MHz	Y/ mS @ 200 MHz
S849T	12 V	1.3	24
S913T	9 V	1.3	24
S594T	5 V	1.3	24
S886T	12 V	1.4	30
S949T	9 V	1.4	30
S595T	5 V	1.4	30
S918T	12 V	1.5	40
S593T	5 V	1.5	40

Table 1 lists the families available at the moment. As the biasing is fixed by the internal circuit, adapted types are necessary for different supply voltages.

More families, e.g., with a different transconductance or for higher frequencies, are under development.

Advantages of a MOSMIC Preamplifier

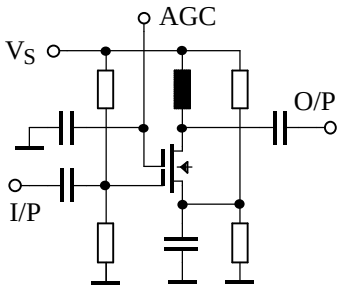

Figure 1. MOSFET preamplifier

Figure 1 shows the circuitry of a conventional preamplifier using a MOSFET. The four resistors are necessary for biasing the circuit. As the MOSFET is of the depletion-type, the source resistor is used to limit the current. The capacitor in parallel to it acts as a RF ground to keep the gain high.

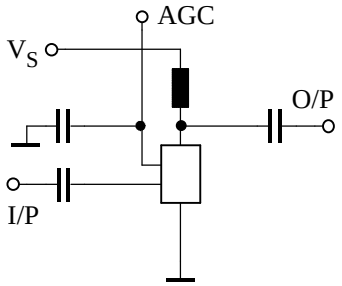

Figure 2. MOSMIC preamplifier

Figure 2 shows a preamplifier using a MOSMIC. A comparison with the old concept shows that all five external components mentioned above have been eliminated. This offers an advantage in cost and PCB space (which is doubled or tripled for a tuner with separate RF branches for VHF and UHF).

The second advantage is the different way to activate a preamplifier stage. Part of the MOSMIC device is a power-down circuit. The MOSMIC is switched off, if the G1 voltage is changed to a level below 1 V, by connecting a resistor to ground. Compared to the standard method with a MOSFET (switching off the drain voltage), the isolation between input and output is improved significantly. This feature reduces antenna radiation and increases the decoupling from the antenna to the IF part. A more detailed description of the switching method is given in the chapter „The New EasyLink Concept“.

The internal control circuit of the MOSMIC keeps the drain current on a nearly constant level when reducing the gain by means of the G2 voltage. This new feature improves the large-signal behavior (intermodulation and cross modulation). Figure 3 shows the difference between a conventional MOSFET preamplifier and the MOSMIC. The measurements were performed in the test fixture with 50- Ω impedance.

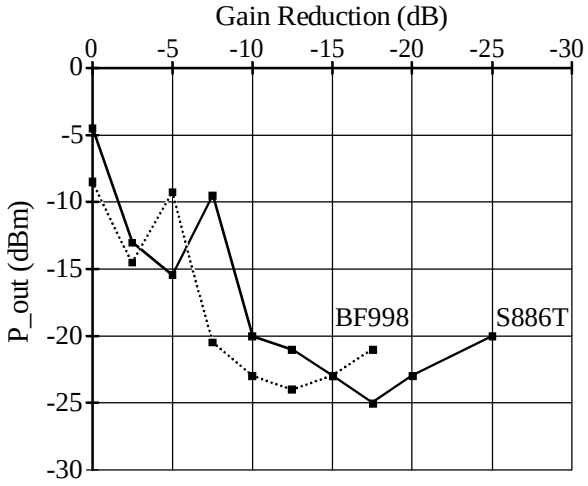

Figure 3. Intermodulation versus gain reduction

Reference for both is an ideal gain-controlled amplifier. It can be intended as a constant gain amplifier with an attenuator in front of the input. Thus, the possible output voltage for a certain intermodulation distortion is constant for all gain values. Figure 3 shows this output voltage versus the gain reduction for an IM3 distortion of -50 dBc. The curve for the "reference" amplifier would be a horizontal line. Neither amplifier achieves the ideal curve of the reference amplifier. The MOSMIC, however, delivers about 3 dB more output power for a given IM3. For a comparable output, this gives a performance increase of 6 dB for IM3 distortions.

Differences between MOSMICs and MOSFETs

If a MOSFET (e.g., the BF998) is replaced by a MOSMIC, the proceeding is easy. Dependent on the supply voltage, the appropriate type is chosen. The parts mentioned above (four resistors and one capacitor) have to be removed. The source resistor must be replaced by a short circuit.

Now two differences have to be considered:

- The maximum allowed G2 voltage is lower. This problem may be solved by a voltage divider near the MOSMIC. As the AGC voltage of most of the TV tuners is delivered by the IF circuit, we recommend the adjustment of a few corresponding resistors in the IF part.

- The slope of the AGC curve is higher. Figure 4 shows a comparison. This is an inherent feature of the MOSMIC, which might influence the stability of the AGC loop in a negative way, depending on the prior layout with the MOSFET. Only slight changes in the IF part have to be made in order to solve potential problems.

TEMIC is prepared to give direct support for these modifications. The new generation of IF amplifiers, for example, allows a negative dynamic feedback. In practice, these problems can be observed only in the case of receiving standard L/ L' signals.

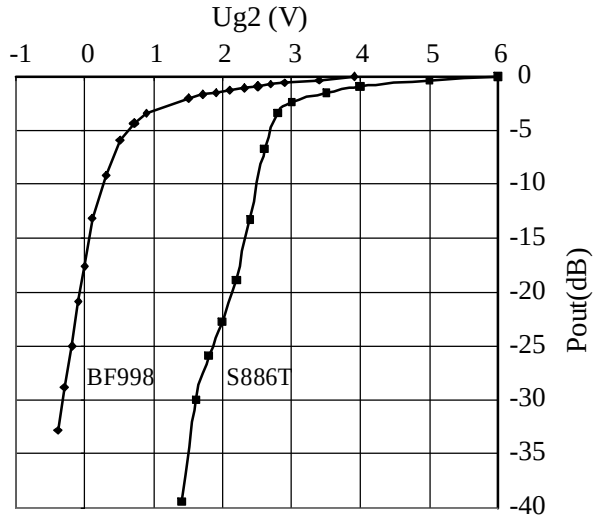

Figure 4. Comparison of gain control

Replacing MOSFETs by MOSMICs offers the following advantages:

- Fewer external components
- Less space required on the PCB
- Better intermodulation performance
- Low power band switching
- Higher reverse isolation when turned off

The TV Mixer Families

Overview

TEMIC actually produces two families of TV mixers, the U2300B and the U2321B. Their main 12-V types are listed in table 2. New types and families, e.g., mixers in SSO packages, are still under development. The column "Remarks" refers to other types.

- 'M' indicates a pin-mirrored type
- '9' indicates a version with 9-V supply voltage

Table 2. TV mixers

Type	Package	No. of Mixers	SAW Driver	LO-O/P	Remarks
U2300B	SO28	3	Yes	Yes	9
U2320B	SO20	2	Yes	No	M, 9
U2321B	SO16	2	No	Yes	9

The main differences between the two families:

- Pinning
- Input impedance of the mixers

Mixer IC Selection Guide

It is often necessary to replace a mixer in a finished design. Package dimensions and pinning of the U2300B mixer family are nearly the same or even compatible with various IC types from other suppliers. The following sections explain technical upgrades of TEMIC products.

The Different Mixer Circuitries

All TEMIC TV mixer ICs have implemented Gilbert mixer cells. The input may be either a common-emitter or a common-base amplifier.

The common-emitter input shown in figure 5 has a high input impedance. It is resistive at low frequencies, but behaves as a capacitive half-plane for higher frequencies. This configuration has the advantage that the input may be driven asymmetrically. By designing it to the necessary tight coupling, the bandpass filter in front of the mixer input is de-tuned. Therefore, its tuning range is reduced considerably. The VHF mixer cell of the U2300B family is of this type.

The common-base input shown in figure 6 has a low input impedance which is resistive at low frequencies and turns into the inductive half-plane for higher frequencies. This input must be driven symmetrically. By this load, the bandpass filter in front of the mixer input is neither de-tuned nor is its tuning-range reduced. The signal voltage across the tuning diodes of the bandpass filter is also reduced by the low-resistive load, thus minimizing intermodulation distortion. As mentioned earlier, all mixer cells are of this type, despite the VHF part of the U2300B family.

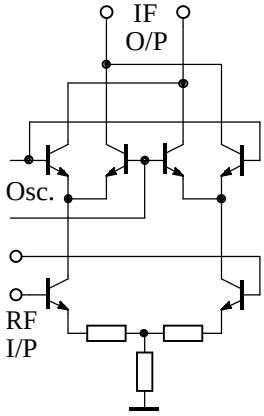

Figure 5. Common-emitter mixer

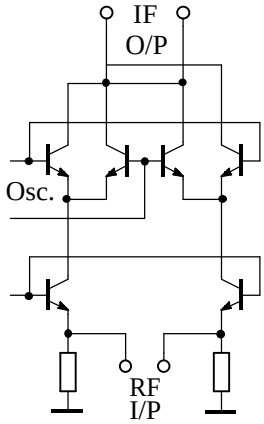

Figure 6. Common-base mixer

The SAW Driver

The SAW driver contained in the mixers of the U2300B family is suited to drive directly a symmetrical SAW filter. The high losses of the filter of up to 30 dB (related to the picture carrier) are compensated. The very low output impedance of the driver suppresses the so-called triple-transient response. Some tuner applications, however, need a different IF output connector, e.g., an asymmetrical one with an impedance of 75 Ω. In this case, a discrete transistor stage should be taken into consideration.

The LO Output

For a PLL-controlled tuner, the simplest method is to use a mixer with a local oscillator (LO) output. If the interface between mixer and PLL is well defined, there will be no problems with poor sensitivity of the PLL or a weak output signal of the oscillator. Some mixer-ICs have no LO output[2]. They were designed mainly for voltage synthesis tuners. Of course it is possible to apply these kinds of components. The chapter „No LO Output“ will show how to connect these ICs to PLL circuits.

Frequency Tuning Range

TV tuners differ in the required oscillator tuning range. Problems may arise if the tuning range of an oscillator is too wide. Therefore, some ICs have three mixers and three oscillators. As a result, better performance is possible compared to the 2-oscillator types, but costs for the periphery are higher.

Influence of the Supply Voltage

Most TEMIC TV mixers are now available with two different supply voltages (12 V and 9 V). This possibility simplifies the production of tuner types for two supply voltages and makes customer demands easier to fulfill. Some differences, however, have to be kept in mind:

- The higher supply voltage gives a better large-signal performance
- The coupling capacitors at the oscillators have to be adjusted slightly
- The lower power dissipation of 9-V types allows smaller IC packages

Examples of Mixer Applications

The following sub-chapters contain only some of the important topics. For the overall circuitries of the specific mixers, see the appropriate IC- or tuner data sheets.

Connection to the Bandpass Filter

As explained in the chapter „The Different Mixer Circuitries“, there are two different types of mixer inputs.

The common-emitter type is very easy to handle because usually only one input is connected to the bandpass filter via a fixed capacitor. The other input pin of the mixer is RF-grounded by means of a second capacitor. So there is no need for a symmetrical input configuration. To improve the tracking and the shape of the bandpass filter, tuned coupling is also possible by adding one varicap diode and resistors.

The common-base mixer is the better solution with regard to RF aspects. However, there is also the stringent necessity for a symmetrical input. There are two ways to connect an asymmetrical bandpass filter to a symmetrical mixer input:

- Simple mutual coupling
- A more sophisticated circuit including coils for impedance transformation

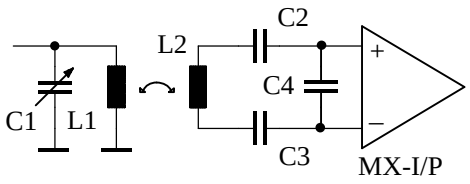

Figure 7. Mutual coupling

Figure 7 shows the first method. The mixer input is coupled to the bandpass filter by means of coil L2, which is located near coil L1 of the secondary part of the filter. In reality, the bandpass filter looks more complex. The load of the filter is adjusted by the ratio of the windings and the distance between the coils. C2 and C3 serve for DC blocking. The transformer may be extended to a resonant type by adding a suited capacitor C4.

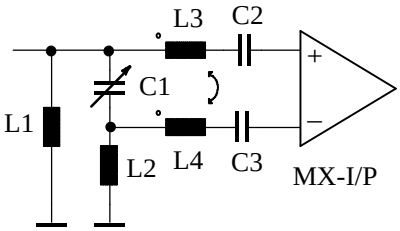

Figure 8. Inductive transformation

Figure 8 shows the more complex method. Again, L1 and C1 represent the secondary part of the bandpass filter. C1 is connected to ground by L2. L3 and L4 perform the transformation of the mixer's low input impedance to the resonant circuit. At the same time, they are mutually coupled to achieve a symmetrical signal at the mixer input. The orientation of the coils is indicated by points.

The Different Oscillator Circuits

Several types of oscillators are used for the different applications. All TEMIC mixers have an asymmetrical 2-pin oscillator for the lowband- and symmetrical 4-pin

oscillators for the higher frequencies. Four types of external circuits are recommended, depending on the count of mixers plus oscillators and on the frequency band. The frequency span of each one is mainly limited by the external components as all oscillators include broadband amplifiers.

The following figures show extracts from the data sheets of the examples mentioned. Please refer to these for complete information about the recommended circuitry.

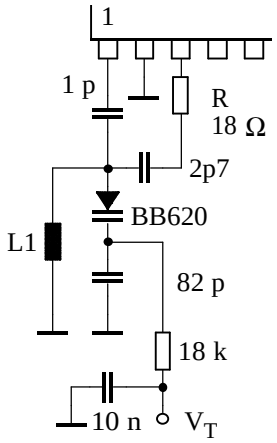

Figure 9. Simple 2-pin oscillator

Figure 9 shows the circuitry for the first oscillator type, e.g., band A of the U2300B. As this IC contains three mixers plus oscillators, the frequency range is limited to about 80 - 230 MHz. Pin 1 is the input and pin 3 the output of an IC-internal amplifier. Output and input are in phase. The resistor R with a value of 18 Ω serves to avoid possible parasitic oscillations at frequencies around 1 GHz.

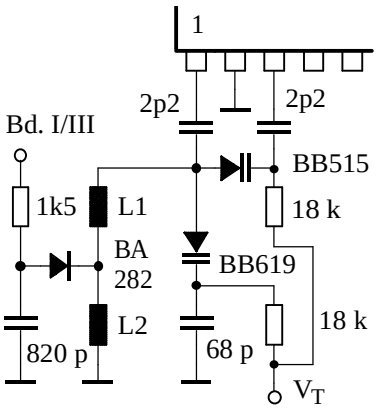

Figure 10. 2-pin oscillator with tuned feedback

The circuitry shown in figure 10 is recommended for VHF oscillators with switching diodes like the BA282. An example is the U2320B, where one oscillator covers the ranges of about 80 - 230 MHz plus 230 - 500 MHz. This is the whole VHF range including the Hyperband. Three problems arise with this concept:

- The switching diode adds losses to the resonant circuit
- The padding capacitor in series with the varicap has to be very large, and thus the varicap adds losses to the resonant circuit
- In an oscillator with fixed feedback, there is only one frequency with an optimum feedback condition.

The internal circuit of the IC is the same as in the example above. The above mentioned problems can be minimized by adding a tuned feedback (BB515 plus 18-k resistor) to the circuit. Moreover, the tuning span is increased significantly.

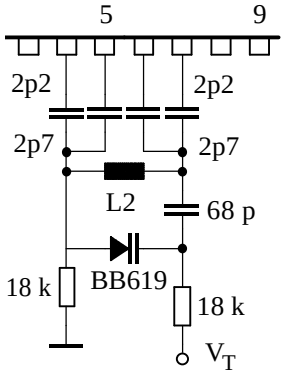

Figure 11. Simple 4-pin oscillator

Figure 11 shows the external circuitry for the Hyperband oscillator, e.g., that of the U2300B. Pins 4 plus 7 are the inputs and pins 5 plus 6 the outputs of the internal symmetrical amplifier. Pin 4 is in phase with pin 5. The range is about 230 - 500 MHz. A symmetrical oscillator improves the performance of the mixer and reduces radiation problems. If the tuning span is limited to a factor of around 2 and the maximum frequency is below 700 MHz, there is no need for additional components to extend the range.

The circuit shown in figure 12 is used for all UHF oscillators. Again, the example is the U2300B. Compared to figure 11, three components were added. L4 and the 100-pF capacitor increase the possible tuning range significantly. The 2k2-resistor suppresses possible subharmonic oscillations of the extended circuitry. The proper value of the resistor has to be fixed for a certain design. If the value is too small, losses are again added to the circuit.

At frequencies above 700 MHz, the transit time through the oscillator amplifier can not be neglected. From outside the IC this seems to be a capacitive load which increases with the frequency. One way to decrease this

effect is to reduce the size of the coupling capacitors between the IC and external circuit. This, however, leads to problems at the low end of the oscillator. The extension described above is the best compromise to solve the problem mentioned.

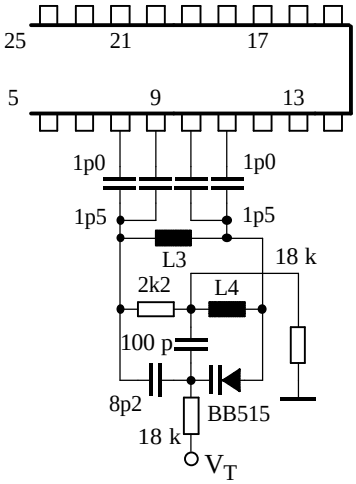

Figure 12. 4-pin oscillator with extended range

Some typical data of the varicaps used above can be found in table 3.

Table 3. Typical data of the varicaps

Type	C @ 1 V	C1 / C28	R_s / Ω
BB620	70 pF	22	1.3
BB619	39 pF	15	0.6
BB515	19 pF	9	0.5

No LO Output

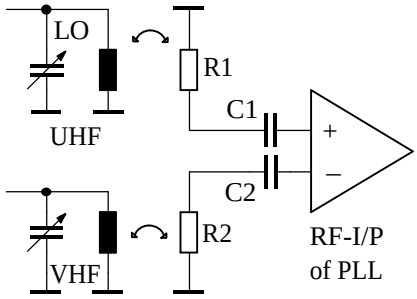

Figure 13. Mixer without LO-O/P plus PLL

Some types of mixer ICs have no direct LO output to connect a PLL. This is not, however, a major problem if a corresponding PLL circuit is applied. TEMIC PLLs are very sensitive and can therefore be used easily.

Figure 13 shows the principle circuitry. At the sides of the oscillator's resonant circuits there is enough electro-magnetic field strength to induce a sufficient voltage in a short wire or resistor. So the PLL gets its inputs from two different sources (VHF and UHF). While only one input is active, the other is decoupled to ground by the capacitor and the resistor. The value of the resistors is about 50 Ω. The capacitors should be around 10 pF to form a high-pass filter together with the input impedance of the PLL. This prevents IF signals from disturbing the input. The overall sensitivity of the PLL is not reduced significantly.

PLLs for a TV Tuner

Overview

Phase-Locked Loop (PLL) circuits are the best choice to stabilize an oscillator on different frequencies with a certain step size. TEMIC produces a large variety of these types of circuits. They differ in the following features:

- Application in TV, satellite TV, telecom
- Similarity to European and Japanese competitors
- Frequency range up to 1 GHz, 2.9 GHz and more
- Pin count from 14 to 20
- Packages DIP, SDIP, SO, and SSO
- Bus is I²C, 3-wire or UNIVERSAL bus
- PLL self-oscillating[3] or not

The UNIVERSAL bus is a new development by TEMIC. 'Universal' means that the circuit automatically detects whether it is connected to an I²C- or a 3-wire bus. This feature simplifies the production of tuners for both bus systems.

Table 4 gives an overview of the PLL families used in TV tuners for analog transmission systems and SAT TV.

Table 4. Recommended PLLs

Type	U63xxB	U620xB	U621xB	U622xB
Package(s)	(S)DIP20 SO20L	SO14 SO16	SO16	SO16
Bus	3-wire	I²C	UNIV.	UNIV.
Self-osc.	Yes	Yes/ no	Yes/ no	Yes
V_S	5 V	5 V	5 V	5 V
I_S	65 mA	55 mA	35 mA	25 mA
Application	TV	TV	TV	SAT TV

Digital transmission systems were introduced in the USA in 1994 (DSS via satellite) and will be introduced in Europe in 1995 (DVB). The demands concerning phase noise of the oscillators used in such systems are higher than in analog systems. Other types of PLLs are therefore necessary for digital application. Some telecom types by TEMIC are well-suited for digital systems. Special concepts for DSS / DVB are under development.

The following chapters will not give an introduction to the PLL principle. The necessary literature is given in the appendix.

Controlling the PLL

As mentioned before, there are mainly two types of bus systems. Independent from the PLL used, the development engineer needs a flexible tool to program the PLL. The best choice is a PC with a small interface connected to a parallel port. A suitable program[4] can control all necessary features of the PLL. These are not only the divider ratios, band switches and different currents of the phase detector, but also the test mode of the PLL.

This test mode is described in the individual data sheets. The following actions can be started by setting certain bits in the control words:

- Connecting the output of the main divider to a band switch
- Connecting the output of the reference divider to a band switch
- Inhibiting the output of the amplifier (OS bit)

With full control over the PLL IC, possible problems can easily be detected.

To check the connection between the PC program and the PLL, a band switch can be activated and switched off again. Some band switch outputs are of the open-collector type and a resistor should therefore be connected to the supply voltage.

To check the correct function of the reference divider, look at the appropriate band switch. The desired reference frequency should be measured.

The main divider function is checked at another band switch output. It must be kept in mind that the waveform is not symmetrical.

To check the programming at a certain frequency, connect an external signal source to the input instead of the LO output. If the frequency of that source is lower than the programmed frequency, the tuning voltage quickly changes to its highest value (e.g. about 30 V) and vice versa.

Application Hints

The Loop Filter

Most of the necessary parts forming the frequency control loop are implemented in the PLL IC. The only additional external components are an NPN transistor to handle the 33-V tuning voltage source and a filter consisting of one resistor, R1, and two capacitors, C1/ C2 (see figure 14). Together with the VCO, a "type 2 third-order loop" is formed[5].

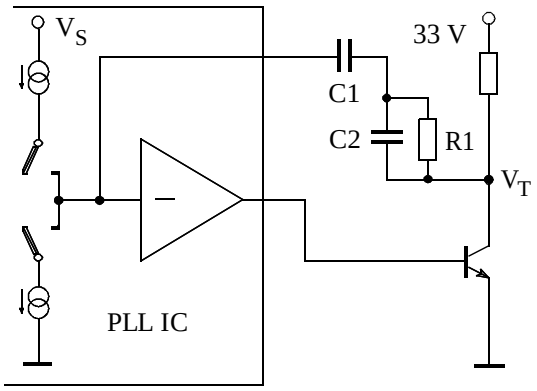

Figure 14. A typical loop filter

This consists of two integrators, one being the VCO and the second the filter with the three time constants

$$\tau_1 = R2 \times C1 \qquad \text{(pole)}$$

$$\tau_2 = R1 \times (C1 + C2) \qquad \text{(zero)}$$

$$\tau_3 = R1 \times C2, \qquad \text{(pole)}$$

where $\omega = 1 / \tau$ and $\omega_3 > \omega_2 > \omega_1$.

R2[6] is not included in figure 14, it can be calculated from the data sheet. The current I_{CP} of the pump has to be translated to its equivalent voltage source. Therefore, an approximation is

$$R2 = (V_S / 2) / I_{CP}$$

For a current of 180 µA, for example, R2 can be calculated as ≈ 13.9 kΩ.

As a result, the designer has some independence to influence the loop performance which can be described by the open loop gain. Unfortunately, this gain can not be measured because of the integrating amplifier. Other methods to characterize the loop have to be utilized, e.g. the step response[7]. There are some programs for the CAD[8] of a PLL loop.

An easy way to develop a PLL-controlled tuner is to take the necessary component values from the appropriate data sheet. This is, however, only a proposal. The result may be influenced by quite a different tuning steepness[9] of the oscillator or by additional low-pass filters, placed between PLL and the varicap diode of the VCO.

The following is necessary to check and optimize a system:

- Measurement of the performance
- Knowledge of what to change

As mentioned above, the open loop gain, which is a complex function, describes the performance of the loop. One part of it is the gain constant K. The VCO tuning steepness and the current of the phase detector contribute to it. The low-pass frequency, ω_1, is part of the overall low-pass characteristic of the loop, while the high-pass frequency, ω_2, mainly serves for the stability of the loop (the so-called phase margin). The second low-pass, ω_3, improves suppression of the reference frequency.

Damping Factor and Loop Frequency

One way to describe the control loop is by using a function which includes the poles and zeros mentioned above. Another way is by using a function which has been normalized to a form that includes two terms

- Natural frequency, ω_n
- Damping factor, D, or the phase margin

The damping factor is used and can be calculated up to functions of the second order. For higher orders like the example above, the term „phase margin“ is common, but the damping factor is easier to comprehend.

The damping factor describes how the loop will reach its final value. A value of 1 means an exponential approach without ringing. A value < 0.7 means faster lock-in, but ringing with a frequency of about ω_n and an exponential decreasing amplitude.

Therefore, ω_n describes the speed of the phase lock loop plus the ability of the loop to suppress interference and disturbances. For this effect, the loop can be seen as a high-pass filter with a cut-off frequency of ω_n. On the other side there has to be a low-pass filter in the loop to suppress or smooth the pulses of the phase detector (e.g. 7.8125 kHz). As a compromise, ω_n should be around 300 Hz for the example above.

All variable parameters of the loop influence both the damping factor and the natural frequency. An exception is the cut-off frequency, ω_3, which mainly influences the suppression of the reference frequency.

Dependent on the possibilities given by the software to control the PLL, the large variation of the VCO's tuning steepness has to be kept in mind when optimizing or testing the performance[10] of the PLL tuner. A damping factor from 0.3 to 0.6 seems to be the optimum.

A rough formula is given in the literature[11] for a second-order loop:

$$\omega_n = \sqrt{\frac{K_{VCO} \times I_{CP}}{N \times C1}}$$

$$D = 0.5 \times \omega_n \times R1 \times C1$$

where C2 of the loop filter is neglected, N is the overall division ratio, K_{VCO} (in MHz/V) is the tuning steepness of the LO and I_{CP} is the current of the phase detector pump.

Avoiding Disturbances

Bus systems in general have more or less problems with crosstalk caused by the activity on the bus with its very fast digital signals of 5 V amplitude. TEMIC PLLs have been developed to minimize noise from within the IC. So the main problem is the layout of the customer application. The following points should be observed:

- Shortest possible connection between the interface and the programming pins of the IC
- Good ground connection for the IC
- For I²C, a series resistor of about 270 Ω should be used at SDA and SCL. Better performance is achieved by a T type filter with 2 × 150 Ω plus a capacitor of 100 pF from center to ground. Using higher values for the resistors, problems will arise with regard to the acknowledged feature of the bus.
- Unused band switches may be connected together with a pull-up resistor to V_S and a blocking capacitor to ground. They should be programmed to the high impedance state.
- The programming wires may influence the VCO and harmonics of the crystal oscillator may disturb the IF part of the tuner. So keep them at a distance.
- Hold the bus in an active mode only when a change is necessary. PLLs are often programmed at very short intervals.

The New EasyLink Concept

Definition

EasyLink is a new concept for TEMIC PLLs. Customer-specific modified standard PLLs support the tuner developer and manufacturer by the following features:

- Easy connection between PLL, MOSMIC pre-amplifier and mixer
- Full support of the MOSMIC benefits including G1 switch-off
- Correct band switching of the mixer used by the customer
- Full software compatibility
- Minimizing possible problems

Examples

The following examples show the principle of EasyLink. Solutions generally have to be found in co-operation with the customer to meet his demands.

3-Mixer IC and MOSMICs

This example shows the full benefit of EasyLink. A PLL shall control:

- A mixer IC with three mixers and oscillators (e.g., U2300B)
- Three MOSMIC preamplifiers

First, a short overview is given about a special feature of today's PLLs. There are two types of band switches, one with NPN- and one with PNP transistors. The traditional method for band switching is switching off the supply voltage. Therefore, external PNP transistors have to be added to the PLL type with NPN switches. This need for external components led to the development of PLL circuits with PNPs.

Using internal PNPs for the band switch, however, has several disadvantages:

- The necessity for an additional pin in the PLL for the supply voltage, e.g., of 12 V
- Integrated PNPs need a lot of space on the chip, thus increasing the price of the component
- They need a lot of current, because their DC current gain factor is very low
- They have to be protected against short circuits (All leads of the tuner that carry the supply voltage are exposed to the danger of being shorted during measurements and alignment)
- In addition to the problems mentioned above, PNPs are not only unnecessary but also inconvenient for a tuner with MOSMICs

To obtain the best performance, MOSMIC preamplifiers should be switched off[12] at Gate 1. The mixer has a tri-state band switch input and needs three different voltages. So the simplified circuitry in figure 15 shows the "EasyLink" of all components. Compared to the traditional approach, only few external components are necessary.

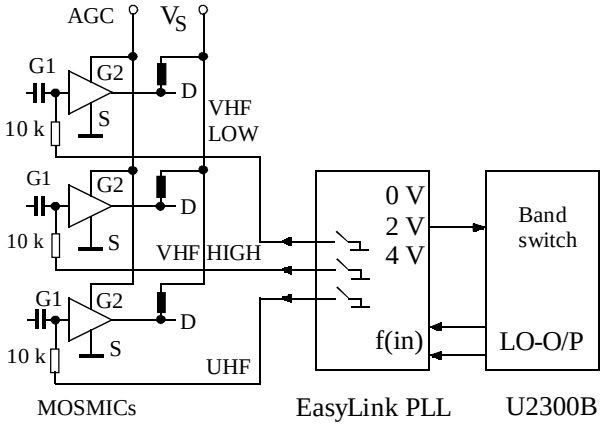

Figure 15. Example for an EasyLink

There is an obvious problem in this case, however. In a conventional concept, an active band switch activates the appropriate preamplifier. The mixer is switched by means of a small network consisting of diodes and resistors. The MOSMIC preamplifier is switched off via G1 by an active band switch. The concept of figure 15, together with a standard PLL, would no longer be software-compatible to prior tuners. There is no solution as to how the MOSMICs and the mixer can be switched off by a simple external logic. Therefore, the easiest way to solve this problem is to use the EasyLink. TEMIC can make the minor modifications in the PLL's logic on a customer-specific basis. The software remains un-changed.

Non-Self-Oscillating PLL

This is an example for reducing possible problems in the tuner. One weak point of the oscillators is their behavior[13] at low tuning voltages, where the quality factor of the external resonant circuit is low. There are two possibilities:

- The oscillation stops
- A parasitic oscillation starts at a very high frequency

The oscillators of TEMIC mixers are developed to avoid parasitic oscillation.

Most PLLs and prescalers are self-oscillating if the input amplitude is too low. This is an inherent feature of this type of circuits. It is not possible to decide whether there is a valid input signal or not. The virtual input frequency seems to be in the upper part of the normal operating range.

TEMIC has long experience in producing prescalers with a modified circuitry. These devices don not self-oscillate in the absence of an input signal. This principle can be transferred to PLL circuits.

There are therefore two possibilities if an oscillator has stopped at a low tuning voltage, depending on the associated PLL type:

- If the PLL is of the self-oscillating type, it is „fooled“ by this effect. The input frequency seems to be too high, and the tuning voltage decreases to its minimum value and will remain there. Changing the channel without an additional band change will have no effect; the tuner is blocked.
- If the PLL is of the non-self-oscillating type, the input frequency seems to be too low (i.e., zero). The tuning voltage therefore rises to a higher value and the oscillation will start again. The voltage may decrease again and the oscillation may stop. The cycle mentioned above restarts – changing the channel will nevertheless be possible.

As the improved non-self-oscillating PLL has the same features as the oscillating PLL, it can easily replace the standard type if useful.

Appendix

This appendix contains a description of measurement procedures to assist application designers. The measurement results have been used in previous chapters which include references to topics in this chapter. Wherever possible, a simple gear was used for the measurements.

Measurement of Tuner Parameters

Quality Factor of Resonant Circuits

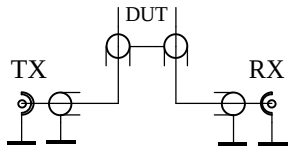

Figure 16. Cable for Q measurement

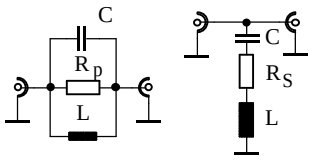

Figure 17 Measuring Q factors

The necessary equipment includes a swept signal generator and a receiver which may include a broadband detector (e.g. the Polyskop by ROHDE & SCHWARZ). A specially assembled temperature-resistant coax cable of the same impedance as the generator source is very useful. Figure 16 shows how the cable is assembled. The measurement system is calibrated by connecting the two inner conductors. This is equivalent to an R_p of zero Ω or an R_s of infinity (see figure 17 and table 5). The DUT is then connected to the cable as shown in figure 17, depending on whether it is a parallel or series resonant circuit. At the resonant frequency, the reactance of C and L realizes compensation and the voltage at the receiver is at a minimum referred to the calibration performed earlier. The remaining circuit consists of a voltage divider with three resistors. Table 5[14] shows which equivalent parallel resistor R_p or series resistor R_s causes the measured voltage gain (attenuation), if the system impedance is 50 Ω.

With a known capacitance or inductance value, the quality factor can now be calculated.

Table 5. Calculation of the equivalent resistor

V_G	R_p	R_s	V_G	R_p	R_s
/ dB	/ Ω	/ Ω	/ dB	/ Ω	/ Ω
0	0	Infinity	-11	254.8	9.8
-1	12.2	204.9	-12	298.1	8.4
-2	25.9	96.6	-13	346.7	7.2
-3	41.3	60.6	-14	401.2	6.2
-4	58.5	42.7	-15	462.3	5.4
-5	77.8	32.1	-16	531.0	4.7
-6	99.5	25.1	-17	607.9	4.1
-7	123.9	20.2	-18	694.3	3.6
-8	151.2	16.5	-19	791.3	3.2
-9	181.8	13.7	-20	900.0	2.8
-10	216.2	11.6	-21	1022.0	2.4

This calculation is not necessary for some applications. Here, only the value of the equivalent resistor is important and not the quality factor of the resonant circuit.

In many cases, the values of C and L are also unknown. Determining the C value by a short experiment is easy. A small capacitor C_x (of a known value) is simply connected in parallel with the unknown C and the change of the resonant frequency from f_1 to f_2. is controlled. C can now be calculated as:

$$C = \frac{C_x}{\left(\frac{f_1}{f_2}\right)^2 - 1}$$

It can be seen from table 5 that the described method is very sensitive for a small R_s and a large R_p. The series resistance of tuning diodes can thus be measured by adding a high Q inductor and using the series resonant method.

For more complex circuits such as crystals, the use of a CAD tool[15] is recommended to compare the measurement with the simulated equivalent circuit.

Voltage Levels and Load Impedance

Measurements of the **V**oltage **G**ain (VG) of different tuner stages are required to verify figures in the data sheet or to collect data for a level diagram[16]. The load

impedance must also be known for the calculation of **P**ower **G**ain (PG) .

The VG cannot be determined very exactly as the RF probe tip used may influence the result by loading and/ or de-tuning the test point. This possible failure can be reduced by using the following method: The gain is measured by means of a tuned receiver (e.g., spectrum analyzer). A second receiver (e.g., broadband) is connected to the IF output of the tuner and monitors the change of amplitude when the probe tip is connected to the test point. This difference is subtracted from the result of the tuned receiver.

The data sheets of the semiconductors used can be consulted to obtain the load impedance, R_p, at a certain point of the tuner. The most practical method again uses the receiver at the IF output. An additional resistive load, R_x, is connected in parallel with the point of interest. The value of this load is changed until the measured output voltage is one half of the voltage without load . R_x is then equal to R_p, the resistive part of the unknown impedance. WARNING: this method is valid only, if the resistance of the load is smaller than the output resistance[17] of the preceding stage.

Cascaded Noise and Intermodulation

When a tuner design is complete, it is necessary to determine the weak points concerning noise and intermodulation distortions. From the antenna to the IF output, there are several stages which contribute to these unwanted effects. Formulas describe the behavior of cascaded stages with regard to noise[18] and **I**nter**M**odulation (IM). As some passive components produce IM also, a measurement is suited to support and improve the design.

The test set-up for noise figures or IM[19] of the third (IM3) or second (IM2) order is used for the measurement. It is also possible to use a selective receiver (e.g., spectrum analyzer) for both measurements, thus replacing the noise figure meter. It will be necessary to connect the measurement equipment to multiple points in the tuner.

By connecting a resistive load of an appropriate value in parallel with the output of a certain stage, the overall gain is reduced by several dB. If noise figure or IM remains at the same level, the following stages up to the test point do not contribute to it significantly. By repeating this method with the outputs of every stage, those parts of the tuner can be determined where an improvement is most effective. The results of the noise measurement can also be compared to the level diagram to verify its input data.

Level Diagram of a Tuner

The level diagram is a powerful tool for tuner development. If computer programs like Microsoft Excel are used, it is possible to simulate a kind of virtual tuner in order to show the influence of the different stages and how they contribute to noise and other effects. The spreadsheets shown in table 6and table 7 are limited to noise examination. In table 6, the columns and rows are labeled to simplify the following explanation.

First of all, an explanation is needed for the data which has to be entered into the level diagram: Row 1 shows the bandwidth used (5 MHz). The different stages are marked and named; for example, the preamplifier is column C. The voltage gains (row 7) and noise figures (row 9) of the different stages can be measured or taken from the data sheets. The impedance (row 3) between the stages is also required. The voltage in field B4 (voltage at the antenna jacket, e.g., 2.5 mV/ rms) is set to that value, as from which the IF circuit shall start reducing the gain of the preamplifier.

The rest of the data is calculated by means of fundamental equations. These are:

- The power at the inputs of all stages (row 5)
- The power gain of all stages (row 8)
- The cascaded power gain (row 11)
- Several noise parameters (rows 12, 14, 15)
- The noise figure from the antenna to this point (row 16)
- A so-called quality factor (row 17)

The meaning of the quality factor is explained by an example. The value of 0.44 dB per dB in field D17 means that the cascaded noise figure increases by 0.44 dB in the following stage (F16) if:

- The power gain of the preceding stage (C8) is reduced by 1 dB

or

- The noise figure of the following stage (E9) is increased by 1 dB

Interfaces with high values for the quality factor (e.g., columns D and J) indicate that their two associated stages (preceding and following) are sensitive related to noise.

The IF circuit is partly included because it may also increase the noise figure or **S**ignal-to-**N**oise ratio (S/N). Its noise figure is calculated from data included in the data sheet.

Table 6. Level diagram U2300B VHF-I/P

	A	B	C	D	E	F	G	H	I	J	K	L
1	System settings:	Bandwidth = 5 E + 06										
2			Preamplifier		U2300B +		SAW driver		SAW filter		IF circuit	
3	Impedance/Ω	75		500		500		1000		1000		1000
4	Signal voltage/ mV (rms)	2.5		22.3		62.8		995.3		31.5		31.5
5	Signal power/ dBm	-40.8		-30.0		-21.0		0.0		-30.0		-30.0
7	Voltage gain/ dB		19.0		9.0		24.0		-30.0		0.0	
8	Power gain/ dB		10.8		9.0		21.0		-30.0		0.0	
9	Noise figure/ dB		3.0		12.0		10.0		30.0		14.0	
11	Cascaded power gain/ dB			10.8		19.8		40.8		10.8		10.8
12	Noise level/ dBm (1 Hz)	-174.0		-160.2		-149.1		-128.0		-157.9		-155.9
14	Noise level/ dBm	-107.0		-93.2		-82.1		-61.0		-90.9		-88.9
15	S/N/ dB	66.2		63.2		61.1		61.0		60.9		58.9
16	Cascaded noise figure/ dB			3.00		5.11		5.23		5.34		7.36
17	Quality factor dB/ dB			0.44		0.44		0.33		0.42		

Table 7. Level diagram U2300B Hyperband I/P

	A	B	C	D	E	F	G	H	I	J	K	L
1	System settings:	Bandwidth = 5 E + 06										
2			Preamplifier		U2300B +		SAW driver		SAW filter		IF circuit	
3	Impedance/Ω	75		30		500		1000		1000		1000
4	Signal voltage/ mV (rms)	2.5		5.6		62.8		995.3		31.5		31.5
5	Signal power/dBm	-40.8		-29.8		-21.0		0.0		-30.0		-30.0
7	Voltage gain/ dB		7.0		21.0		24.0		-30.0		0.0	
8	Power gain/ dB		11.0		8.8		21.0		-30.0		0.0	
9	Noise figure/ dB		3.0		12.0		10.0		30.0		14.0	
11	Cascaded power gain/ dB			11.0		19.8		40.8		10.8		10.8
12	Noise level/ dBm (1 Hz)	-174.0		-160.0		-149.2		-128.1		-157.9		-155.9
14	Noise level/ dBm	-107.0		-93.0		-82.2		-61.1		-90.9		-88.9
15	S/N/ dB	66.2		63.2		61.2		61.1		60.9		58.9
16	Cascaded noise figure/ dB			3.00		5.02		5.15		5.34		7.36
17	Quality factor dB/ dB			0.43		0.04		0.03		0.42		

Table 6 shows the level diagram for the VHF part of the U2300B with an asymmetrical common-emitter input. Table 6 shows the level diagram for the Hyperband part with a symmetrical common-base input. The differences between the input characteristics are explained in the chapter „The Different Mixer Circuitries“.

Both tuner branches have the same overall power gain of 10.8 dB (from the input to the SAW-filter output J11). Everything seems to be very similar. But there is a big difference at the interface between the preamplifier and the mixer. The input impedance (D3) of the Hyperband mixer is much lower. The voltage across the tuning diodes in the band-pass filter, which connects the mixer to the preamplifier, is therefore about 12 dB lower. Varicap diodes produce intermodulation because of their non-linear behavior. This negative effect is significantly reduced by the solution described in table 7.

The level diagram is a powerful tool for development. Several virtual tuners may be compared. The optimum gain values for the single stages can be optimized for

- Best performance concerning noise and intermodulation
- Reduced sensitivity to tolerances in production

Measurement of Mixer Parameters

Tuning Steepness of the VCO

The tuning steepness is an essential factor in tuner development. It can be defined as the change of the oscillator frequency in relation to a change of the tuning voltage. The values are given in kHz/ mV or MHz/ V.

Only the curve is of interest for a voltage-synthesized or simply voltage-controlled tuner. Larger non-steady changes or negative values indicate problems with the oscillator :

- Frequency drift versus temperature
- AFC operation

For a PLL-controlled tuner, the absolute values are also of interest because they determine the stability and the lock-in time of the loop. The results of the measurement method described are also used in the chapter „Loop Constants and Settling Time“.

Measurement should be performed under computer control. Up to 301 points are required for each frequency band, e.g. points at intervals of 100 mV in the tuning-voltage range from 0 V to 30 V. Therefore, the necessary equipment consists of

- A computer with a suitable program
- A programmable voltage source
- A programmable frequency counter

If the mixer/ oscillator used has an LO output, the counter can be connected to it. If this possibility is not given, a small probe should be placed near the oscillator under test. This probe may be realized in the form of a short piece of wire or a 50-Ω resistor at the end of a coax cable. To increase the sensitivity of the counter or to extent its frequency range, an additional frequency divider (prescaler) connected at the counter input is very useful.

The first step is to check the DUT. It must be ensured that harmonics or weak signals from the oscillator do not influence the test. If the tuner is PLL-controlled, the amplifier of the PLL circuit should be disabled[20] by the appropriate bus command in order to avoid conflicts with the external tuning voltage.

Measurement now takes place. For all frequency bands, the tuning voltage is increased from the minimum value (e.g., 0 V) stepwise to the maximum value (e.g., 30 V), the oscillator frequency is measured and stored in the memory of the computer at each step.

All stored values are plotted to display the results. Although the tuning voltage was the independent variable, it is better to plot the tuning voltage versus the oscillator frequency. A sample plot (dotted line) is shown in figure 18 in which the left vertical axis is the tuning voltage in volts.

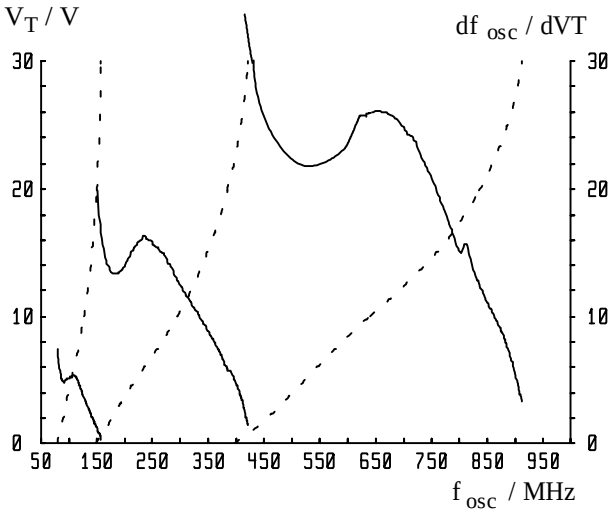

Figure 18. Tuning steepness

To calculate the tuning steepness from the stored values, a difference quotient of neighboring points is plotted against their associated frequency. The steady line shows the result with the right vertical axis being assigned unit kHz/ mV or MHz/ V. The large variation

of the steepness, ranging from about 1 kHz/ mV to about 40 kHz/ mV at the lower end of the UHF is remarkable.

The example above shows the tuning parameters of a DUT equipped with a U2321B. The full frequency range from 48 to 860 MHz is covered in three bands but with only two oscillators. The VHF branch is switched to the second range by means of switching diodes (see also the chapter „Quality Factor of Oscillator Circuits“).

It is worth mentioning the large variation of the tuning steepness, especially at the edge of the bands. Problems may arise concerning the stability of a PLL (see the chapter „Loop Constants and Settling Time“) or AFC performance.

Quality Factor of Oscillator Circuits

This chapter describes a method on how to qualify the whole oscillator circuit in the active state. In the chapter „Quality Factor of Resonant Circuits“, only the quality factor of a single resonant circuit was estimated. This method, however, is not suited for measurement in an active circuit.

The quality of an oscillator includes the Q of the resonant circuit as well as the stability of the oscillation. This stability is mainly influenced by losses in the peripheral components which reduce the gain.

Besides other effects (like lossy coils) in nearly all components, there are two main factors which contribute to the losses:

- Tuning diodes
- Switching diodes

The equivalent circuit of a varicap mainly consists of a voltage-variable capacitor in series with a small resistor R_s of less than 1 Ω. This resistor is changed from the series type to a parallel-connected resistor to achieve an equivalent circuit of the parallel resonant type. The appropriate R_p depends on the value of the effective capacitance, C_s, in series with R_s, which consists of the voltage-dependent part of the varicap and a commonly used padding capacitor. The value of R_p decreases when C_s increases, i.e. at low tuning voltages. The weak point of an oscillator is therefore its behavior at low VT, especially around 0 V.

A switching diode also contributes to losses because parts of the coils are imperfectly shorted.

To realize an in-circuit method to qualify a stable oscillation, it is only necessary to add losses to the resonant circuit in a controlled manner. This can be done by applying a small negative voltage across the tuning diodes. The diodes thus start conducting while the current is limited by the resistors which decouple the diodes. The negative voltage is increased until the oscillation stops or its amplitude falls below a certain level. The value at this point is the quality figure of the oscillator.

The ambient temperature also influences the stability of the oscillation. Instead of heating up the tuner, a correlated measurement can be performed with the method described above.

Measurement of PLL Parameters

It is not possible to determine all parameters for optimization of the PLL from the data sheets or CAD simulations. Thus, the only solution is a measurement.

Loop Constants and Settling Time

A loop has to be fast but stable. The best way to check a design is to measure the overall parameters of the loop. This is best done by controlling the step response[21] of the loop. The PLL is therefore programmed to hop between two frequencies, perhaps including a band change.

A simple method is to measure the tuning-voltage response directly with an oscilloscope. As the tuning steepness[22] of the VCO is very high (up to 40 kHz/ mV), the resolution will be poor. Moreover, there is no direct readout for the frequency offset.

A better way is to use a spectrum analyzer. This instrument is very versatile. It can measure:

- The spectrum of a signal in its standard mode
- Pulses, when switched to a large bandwidth
- Amplitude modulation, when switched to a large bandwidth and the zero-scan mode, tuned to the peak and thus suppressing frequency modulation
- Frequency modulation in the absence of amplitude modulation when switched to a suited bandwidth in the zero-span mode and tuned to the slope of the filter

In the zero-span mode, the spectrum analyzer acts as a receiver at a fixed frequency. Along the slope of the IF filter, a frequency deviation or modulation is converted to a change of amplitude. The filter used needs to be calibrated only once.

If the PLL is hopping between the frequencies f_1/ f_2, where $f_2 > f_1$, the spectrum analyzer should be tuned to $> f_2$ or $< f_1$. This ensures that the analyzer is not influ-

enced by the VCO frequency crossing the top of its IF filter.

If the controller for programming the PLL is able to produce a trigger signal after transmission of the last byte, the spectrum analyzer can be triggered at that time and an exact measurement of the overall settling time is possible.

Figure 19 shows an example for the measurement described. It is performed without a trigger and thus the settling time cannot be determined. The LO hops between 600 and 601 MHz. Calibration of the vertical axis is therefore very easy. It is 1000 kHz/ 4.5 divisions, i.e. 222 kHz per division. The center frequency of the spectrum analyzer is tuned to around 596 MHz. Thus, the higher amplitude is caused "by the 600MHz".

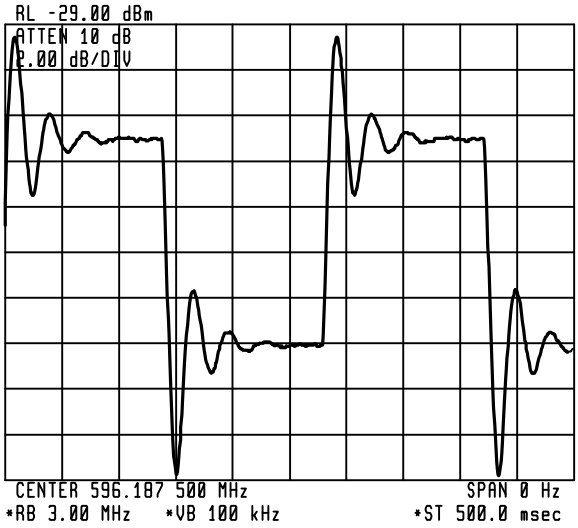

Figure 19. Measurement of the step response

Six msec. after the start of the jump, the frequency crosses the final frequency for the first time. Three overshoots follow, the first having an offset of 600 kHz. The fourth peak is less than 50 kHz of the final value. The loop needs 56 msec. up to this point The frequency of the oscillation is about 32 Hz or 201 rad/sec. The calculation formulas[23] give the results below:

- Damping factor D = 0.33
- Natural frequency, ω_n, = 213 rad/sec

This example is therefore good with regard to the damping factor[24], but too slow in the case of ω_n.

Sensitivity

Some problems seem to stem from insufficient sensitivity of the PLL.

Measurement of the input sensitivity versus the input frequency should be performed in a special test fixture. The main divider of the PLL is programmed to a suitable value Thus, it is able to count its output in the test mode. Typical curves and the guaranteed limits are included in the data sheets. The following has to be kept in mind:

- The input voltage should always lie between the guaranteed minimum and maximum values
- When comparing the curves of an oscillating and a non-oscillating PLL, there is distinct sensitivity around the resonant frequency. Nevertheless, these devices are not sensitive to harmonics of input signals on subharmonic frequencies. Both PLL types behave similar. In order to avoid problems, the first harmonic of the input signal should be below -10 dBc for low input frequencies. A higher harmonic content is possible even for higher frequencies.

To perform a quick check of the tuner, the PLL is programmed to a suitable main counter value N with the OS bit activated, thus disabling the amplifier output. The appropriate band switch has to be activated for each band to be checked, The VCO is tuned by means of the voltage at the 33-V pin which now is directly applied to the varicaps. It is convenient to use a spectrum analyzer with an RF probe connected to the special band switch to which the main counter output is sent in the test mode. Setting the sweep of the spectrum analyzer from 0 to 1000 MHz divided by N gives a quasi-direct readout possibility. As the output of the main counter is a square wave (duty cycle <> 50%), many harmonics appear on the spectrum analyzer screen.

The best criterion for checking a PLL circuit having a sufficient input signal is displaying the output signal on a spectrum analyzer with a small frequency span. The PLL will add noise sidebands to the signal if the input voltage is just above the limit of operation. As the frequency remains the same, a counter cannot check this limit.

Utilities

Literature

Books about PLLs:

Best, Roland E.:	Phase-locked loops. Theory, design and applications. 2nd ed., McGraw-Hill, 1993.	[1]
Rohde, Ulrich L.:	Digital PLL frequency synthesizers. Theory and Design. Prentice-Hall, Englewood Cliffs, N.J., 1983.	[2]
Gardner, Floyd M.:	Phaselock Techniques. 2nd ed., John Wiley & Sons, New York, 1979.	

Application notes by TEMIC:

Measurement of non-linear distortions with the spectrum analyzer, using the example of cross-modulation and intermodulation in television tuners (ANT004)

TV tuner basics (In preparation)

Satellite tuner basics (In preparation)

CAD Tools for PCs

Programs for designing and evaluating PLLs:

SIMUL.	Contained on a disk in [1]. Program for designing PLLs.	(DOS)
R_PLL	Listing contained in [2] on page 453. Designing a 5th-order PLL.	(DOS)
PLLSYN	From the RF Design magazine, Software Service (Disk RFD-0793).	(DOS)
Several programs by TEMIC for controlling a PLL (LPT1 of the PC).		(DOS / Windows)

General simulation tools:

PSpice	By MicroSim. Demo versions are available for DOS and Windows. They can handle only small circuits. However, this is sufficient for some purposes.
Mathcad	By MathSoft. Program for solving mathematical problems.
Excel	By Microsoft. Spreadsheet program for handling formulas. Several spreadsheets, including the described level diagram, are available from TEMIC.

All programs and spreadsheets by TEMIC are available on request.

List of Abbreviations and Expressions Used

AFC	**A**utomatic **F**requency **C**ontrol
AGC	**A**utomatic **G**ain **C**ontrol
D	**D**amping factor of a control loop (in the literature, ζ = zeta)
dBc	**dB** related to a (reference) **c**arrier
DIP	**D**ual **I**n-line **P**ackage (package for ICs)
DUT	**D**evice **U**nder **T**est
EasyLink	New concept by TEMIC
G1	**G**ate **1** of a MOSFET or a MOSMIC
I_{CP}	Current of the phase detector's pump
IF	**I**ntermediate **F**requency
IM2	**I**nter**M**odulation of the **2**nd order
IM3	**I**nter**M**odulation of the **3**rd order (two-tone method)
IS	Supply current
K	Gain constant of a filter, phase detector or VCO
LO	**L**ocal **O**scillator
MOSMIC™	**MOS M**onolithic **I**ntegrated **C**ircuit
N	Divider ratio of a counter
OS	Special control bit for the PLL which inhibits amplifier output
PC	**P**ersonal **C**omputer with an x86-compatible processor
PG	**P**ower **G**ain
Q	**Q**uality factor of a resonant circuit
R_p	Equivalent **R**esistor in a **P**arallel resonant circuit
R_s	Equivalent **R**esistor in a **S**eries resonant circuit
RX	**R**eceiver
S/N	**S**ignal-to-**N**oise ratio
SAT	Satellite
SAW	**S**urface **A**coustic **W**ave
SDIP	**S**hrinked **DIP**
SO	**S**mall **O**utline (package for ICs)
SSO	**S**hrinked **SO**
τ	Time constant of a filter pole or zero
TX	Signal source (**T**ransmitter)
U2300B	Mixer IC by TEMIC
U2321B	Mixer IC by TEMIC
UNIVERSAL	New bus for I^2C and 3-wire
VCO	**V**oltage-**C**ontrolled **O**scillator
V_G	**V**oltage **G**ain
V_S	**S**upply **V**oltage
V_T	**T**uning **V**oltage
ω	Natural (angular) frequency in rad / sec ($2\pi \times f$)
ω_n	Natural (angular) frequency of the PLL in rad / sec

Notes

1 MOSMIC is a registered trademark by TEMIC
2 See table 2 in chapter „Overview“, page 8
3 See chapter „Non-Self-Oscillating PLL“
4 See chapter „CAD Tools for PCs“
5 See Rohde [2], page 31
6 See Rohde [2], page 31
7 See chapter „Loop Constants and Settling Time“
8 See chapter „CAD Tools for PCs“
9 See chapter „Tuning Steepness of the VCO“
10 See chapter „Loop Constants and Settling Time“
11 See Best [1], page 58
12 See chapter „Advantages of a MOSMIC Preamplifier“
13 See also chapter „The Different Oscillator Circuits“
14 EXCEL spreadsheet
15 See chapter „Utilities“
16 See chapter „Level Diagram of a Tuner“
17 See chapter „The SAW Driver“ for an exception
18 Implemented in chapter „Level Diagram of a Tuner“
19 See chapter „Utilities“
20 See chapter „Controlling the PLL“
21 See also chapter „ The Loop Filter“
22 See chapter „Tuning Steepness of the VCO“
23 See Best [1], page 282
24 See chapter „Damping Factor and Loop Frequency“