8-Bit, 250 MSPS 3.3V A/D Converter

Preliminary Technical Data

AD9480

FEATURES

- DNL = ± 0.25 LSB
- INL = ± 0.5 LSB
- Single +3.3 V supply operation (3.0 to 3.6 V)
- Power dissipation of 450 mW at 250 MSPS
- 1 Vp-p analog input range
- Internal 1.0 V reference
- Single-ended or differential analog inputs
- LVDS or single-ended TTL/CMOS outputs
- Power down mode
- Clock duty cycle stabilizer
- Pin-similar to AD9054A

APPLICATIONS

- Digital oscilloscopes
- Instrumentation and measurement
- Communications (modems)

PRODUCT DESCRIPTION

The AD9480 is an 8-bit monolithic analog-to-digital converter optimized for high speed, low power, small size, and ease of use. The product operates at a 250 MSPS conversion rate, with excellent linearity and dynamic performance over its full operating range.

To minimize system cost and power dissipation, the AD9480 includes an internal reference and track-and-hold circuit. The user only provides a +3.3 V power supply and a differential encode clock. No external reference or driver components are required for many applications.

A data sync input is supported for proper output data port alignment, and a data clock output is available for proper output data timing. The digital outputs are TTL/CMOS or LVDS (ANSI 644) compatible with an option of two's complement or binary output format. The CMOS dual (demultiplexed) mode pipes ADC data through two 8-bit channels at one-half the clock rate in either interleaved or parallel mode. LVDS mode provides the best output performance with all data piped at the full clock rate through a single output channel.

Fabricated on an advanced BiCMOS process, the AD9480 is available in a 44-pin surface mount package (44-TQFP) specified over the industrial temperature range (-40°C to +85°C).

FUNCTIONAL BLOCK DIAGRAM

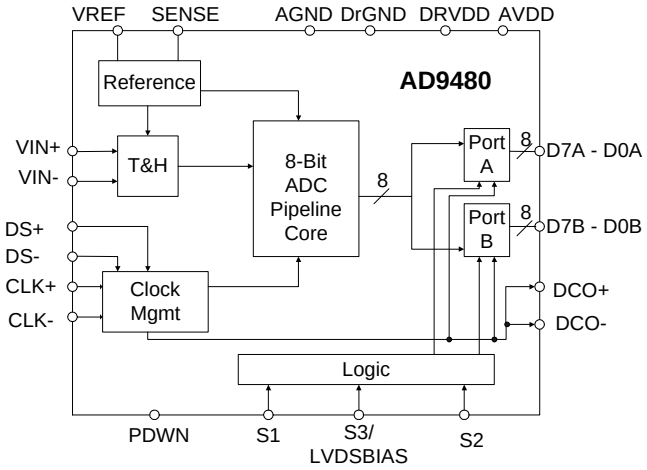

Figure 1. Functional Block Diagram

PRODUCT HIGHLIGHTS

Power down mode – A power-down function may be exercised to bring total consumption down to 13mW

Superior linearity – A DNL of +/- 0.25 makes the AD9480 suitable for instrumentation and measurement applications.

Pin-similar to the AD9054A – Allows easy upgrades for improved linearity and ac performance

LVDS outputs (ANSI-644) – simplifies timing and improves noise performance

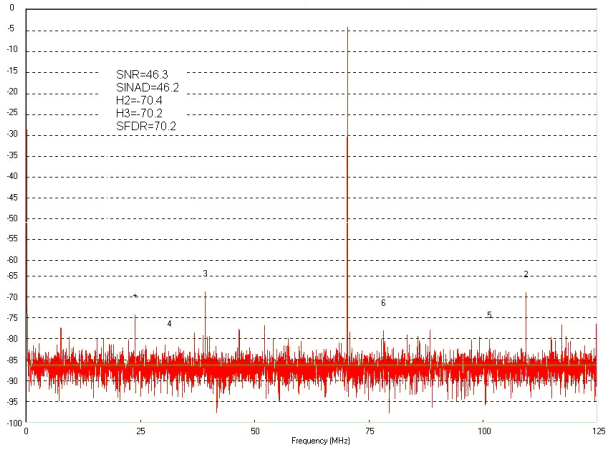

Figure 2 FFT 70MHz Analog Input at 250MSPS

Rev. PrH_ 3/5/2004

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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REVISION HISTORY

Revision PrA: Initial Version

Revision PrB: Added timing diagram

Revision PrC: Updated specifications

Revision PrD: Updated pin names, pin functions, and timing diagram; added application section; formatted to new data sheet template; updated power dissipation and analog bandwidth

Revision PrE: Updated timing diagram, latency numbers, PDWN labeling, Power ---> 470mW

Revision PrF: Added reference, equivalent circuits, package info, DS section

Revision PrG: Added Output Coding section, SFDR spec, SFDR plot, FFT plot, Timing specs, $Theta_{ja}$, Power-Down Dissipation, Vcm for analog, Updated Analog Rin, T_{HDS}, Tj max , AC specs, Power specs, Corrected VREF typo

Revision PrH: added Power Down Timing, Tovr placeholders, corrected ext. VREF typo (p3,10), updated power down description

AD9480—DC SPECIFICATIONS[1]

AVDD = 3.3V, DRVDD = 3.3V; EXT REF; DIFFERENTIAL ANALOG AND CLOCK INPUTS, LVDS OUTPUT MODE, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION					8		Bits
ACCURACY	No Missing Codes	Full	VI		Guaranteed		
	Offset Error	Full	VI				mV
	Gain Error[2]	25°C	I				% FS
	Differential Nonlinearity (DNL)	25°C	I		± 0.25		LSB
		Full	VI		± 0.35		LSB
	Integral Nonlinearity (INL)	25°C	I		± 0.5		LSB
		Full	VI	- 1.0	± 0.7	+ 1.0	LSB
TEMPERATURE DRIFT	Offset Error	Full	V				ppm/°C
	Gain Error	Full	V		110		ppm/°C
	Reference	Full	V		1200		ppm/°C
REFERENCE	Internal Reference Voltage	25°C	I		1.0		V
	Output Current	Full	V				uA
	Input Current	Full	V				uA
	Input Resistance	Full	V				kΩ
ANALOG INPUTS	Differential Input Voltage Range				±0.5		Vpp
	Common Mode Voltage	Full	V		2		V
	Input Resistance	Full	V		10		kΩ
	Input Capacitance	Full	V		4		pF
	Analog Bandwidth, Full Power	Full	V		750		MHz
POWER SUPPLY (LVDS Mode)	AVDD	Full	IV	3.0	3.3	3.6	V
	DRVDD	Full	IV				V
	Power Dissipation[3]	Full	VI		574		mW
	Power Down Dissipation	Full	VI		16		mW
	Power Supply Rejection Ratio (PSRR)	25°C	I				mV/V
	I_{AVDD}[4]	Full	VI		148		mA
	I_{DRVDD}[4]	Full	VI		34		mA
POWER SUPPLY (CMOS Mode)	AVDD	Full	IV	3.0	3.3	3.6	V
	DRVDD	Full	IV				V
	Power Dissipation[3]	Full	VI		452		mW
	Power Down Dissipation	Full	VI		13		mW
	Power Supply Rejection Ratio (PSRR)	25°C	I				mV/V
	I_{AVDD}[4]	Full	VI		146		mA
	I_{DRVDD}[4]	Full	VI		39		mA

Table 1

[1] Specifications subject to change without notice
[2] Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.0 V external reference and a 1 V p-p differential analog input).
[3] Power dissipation measured with rated encode and a dc analog input (Outputs Static).
[4] I_{AVDD} and I_{DRVDD} measured with 19.7 MHz analog input @ 0.5dBFS at 250MSPS.

DIGITAL SPECIFICATIONS

AVDD = 3.3V, DRVDD = 3.3V

Parameter		Temp	Test Level	Min	Typ	Max	Unit
DIGITAL INPUTS (CLK+, CLK-, DS+, DS-)	Differential Input	Full	IV				mV
	V_{IH}	Full	IV				V
	V_{IL}	Full	IV				V
	Input Resistance	Full	IV				kΩ
	Input Capacitance	25°C	IV				pF
LOGIC INPUTS	Logic '1' Voltage	Full	IV				V
	Logic '0' Voltage	Full	IV				V
	Input Resistance	Full	IV				kΩ
	Input Capacitance	Full	IV				PF
DIGITAL OUTPUTS (CMOS Mode)	Logic '1' Voltage	Full	IV	DRVDD – 0.05			V
	Logic '0' Voltage	Full	IV			0.05	V
DIGITAL OUTPUTS (LVDS Mode)	Differential Output Voltage (V_{OD})	Full	IV	247		454	mV
	Output Offset Voltage (V_{OS})	Full	IV	1.125		1.375	V
	Output Coding	Full	IV	Twos Complement or Binary			

Table 2: Digital Specifications

AC SPECIFICATIONS[1]

AVDD = 3.3 V, DRVDD = 3.3 V; INTERNAL REF; DIFFERENTIAL ANALOG AND CLOCK INPUT, LVDS OUTPUT MODE, UNLESS OTHERWISE NOTED

Parameter		Temp	Test Level	Min	Typ	Max	Unit
SIGNAL TO NOISE RATIO (SNR) – Without Harmonics	f_{IN}= 19.7 MHz	25°C	I		46		dB
	f_{IN}= 49.7 MHz	25°C	I		46		dB
	f_{IN}= 70.1 MHz	25°C	I		46		dB
	f_{IN}= 100 MHz	25°C	V		46		dB
	f_{IN}=170 MHz	25°C	V		45.5		dB
SIGNAL TO NOISE RATIO (SINAD) – With Harmonics	f_{IN}= 19.7 MHz	25°C	I		46		dB
	f_{IN}= 49.7 MHz	25°C	I		46		dB
	f_{IN}= 70.1 MHz	25°C	I		46		dB
	f_{IN}= 100 MHz	25°C	V		46		dB
	f_{IN}=170 MHz	25°C	V		45.5		dB
EFFECTIVE NUMBER OF BITS (ENOB)	f_{IN}= 19.7 MHz	25°C	I				Bits
	f_{IN}= 49.7 MHz	25°C	I				Bits
	f_{IN}= 70.1 MHz	25°C	I				Bits
	f_{IN}= 100 MHz	25°C	V				Bits
	f_{IN}=170 MHz	25°C	V				Bits
SECOND AND THIRD HARMONIC DISTORTION	f_{IN}= 19.7 MHz	25°C	I		-60		dBc
	f_{IN}= 49.7 MHz	25°C	I		-60		dBc
	f_{IN}= 70.1 MHz	25°C	I		-60		dBc
	f_{IN}= 100 MHz	25°C	V		-60		dBc
	f_{IN}=170 MHz	25°C	V		-60		dBc
Spurious Free Dynamic Range (SFDR)	f_{IN}= 19.7 MHz	25°C	I		65		dBc
	f_{IN}= 49.7 MHz	25°C	I		65		dBc
	f_{IN}= 70.1 MHz	25°C	I		65		dBc
	f_{IN}= 100 MHz	25°C	V		64		dBc

[1] SNR/harmonics based on an analog input voltage of –0.5 dBFS referenced to a 1 Vpp full-scale input range.

Parameter		Temp	Test Level	Min	Typ	Max	Unit
	f_{IN}=170 MHz	25°C	V				dBc
TWO TONE INTERMOD DISTORTION (IMD)	f_{IN1}= 19 MHz, f_{IN2}= 20 MHz	25°C	V		-65		dBc
	f_{IN1}= 70 MHz, f_{IN2}= 71 MHz	25°C	V		-55		dBc

Table 3: AC Specifications

SWITCHING SPECIFICATIONS

AVDD = 3.3 V, DRVDD = 3.3 V; DIFFERENTIAL ENCODE INPUT, UNLESS OTHERWISE NOTED

Parameter		Temp	Test Level	Min	Typ	Max	Unit
CLOCK	Clock Rate	Full	VI	250			MSPS
	Clock Pulse Width High (t_{EH})	Full	IV	1.2	2		nS
	Clock Pulse Width Low (t_{EL})	Full	IV	1.2	2		nS
OUTPUT PARAMETERS IN CMOS MODE	Valid Time (t_V)[1]	Full	VI	2			nS
	Propagation Delay (t_{PDR})[1]	Full	VI		3.7		nS
	Propagation Delay (t_{PDF})[1]	Full	VI		3.4		nS
	Rise Time (t_R)	Full	V		1.6		nS
	Fall Time (t_F)	Full	V		1.3		nS
	DCO Propagation Delay – Rising Edge (t_{CPDR})	Full	VI		3.9		nS
	DCO Propagation Delay – Falling Edge (t_{CPDF})	Full	VI		3.8		nS
	Data to DCO Skew (t_{PD} – t_{CPD})	Full	IV		-.3		nS
	DS+ Input Setup Time (t_{SDS})[2]	Full	IV		0.5		nS
	DS+ Input Hold Time (t_{HDS})	Full	IV		0.5		nS
	Interleaved Mode (A, B Latency)	25°C	VI		8, 8		cycles
	Parallel Mode (A, B Latency)	25°C	VI		9, 8		cycles
Tpwrdown	Power Down Delay	25°C	VI				nS
Tpwrdnrecovery	Power Down Recovery	25°C	VI				nS
Tovr	Overvoltage Recovery Time	25°C	VI				nS
OUTPUT PARAMETERS IN LVDS MODE	Valid Time (t_V)[1]	Full	VI				nS
	Propagation Delay (t_{PD})[1]	Full	VI		2.8		nS
	Rise Time (t_R) (20% to 80%)	Full	V		0.5		nS
	Fall Time (t_F) (20% to 80%)	Full	V		0.5		nS
	DCO Propagation Delay (t_{CPD})	Full	VI		2.6		nS
	Data to DCO Skew (t_{PD} – t_{CPD})	Full	IV		.2		nS
	Pipeline Latency	25°C	VI		8		cycles
Tpwrdown	Power Down Delay	25°C	VI				nS
Tpwrdnrecovery	Power Down Recovery	25°C	VI				nS
Tovr	Overvoltage Recovery Time	25°C	VI				nS
APERTURE	Aperture Delay (t_A)	25°C	V		1.5		nS
	Aperture Uncertainty (Jitter)	25°C	V		0.25		pS rms

Table 4: Switching Specifications

[1] t_V and t_{PD} are measured from the transition points of the CLK input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 10 pF or a dc current of ±40 µA. Rise and fall times measured from 10% to 90%.
[2] DS inputs used in CMOS mode only.

EXPLANATION OF TEST LEVELS

TEST LEVEL

I 100% production tested.

II 100% production tested at +25°C and guaranteed by design and characterization at specified temperatures.

III Sample Tested Only

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at +25°C and guaranteed by design and characterization for industrial temperature range.

Absolute Maximum Ratings

Parameter		Rating
Electrical	AVDD Voltage	4 V max
	DRVDD Voltage	4 V max
	Analog Input Voltage	+0.5 V to AVDD – 0.5 V
	Analog Input Current	0.4 mA
	Digital Input Voltage	+0.5 V to AVDD – 0.5 V
	Digital Output Current	20 mA max
	VREF Input Voltage	+0.5 V to AVDD – 0.5 V
Environmental	Operating Temperature Range (Ambient)	-40°C to +85°C
	Maximum Junction Temperature	150°C
	Lead Temperature (Soldering, 10 sec)	150°C
	Maximum Case Temperature	°C
	Storage Temperature Range (Ambient)	-65°C to +150°C

Table 5: Absolute Maximum Ratings

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Impedance (θja) = 46.4 C/W (4 Layer PCB)

DEFINITIONS

ANALOG BANDWIDTH

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

APERTURE DELAY

The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

APERTURE UNCERTAINTY (JITTER)

The sample-to-sample variation in aperture delay.

CROSSTALK

Coupling onto one channel being driven by a low level (-40 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal.

DIFFERENTIAL ANALOG INPUT RESISTANCE, DIFFERENTIAL ANALOG INPUT CAPACITANCE, AND DIFFERENTIAL ANALOG INPUT IMPEDANCE

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

DIFFERENTIAL ANALOG INPUT VOLTAGE RANGE

The peak to peak differential voltage that must be applied to the converter to generate a full scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak to peak differential is computed by rotating the inputs phase 180 degrees and taking the peak measurement again. Then the difference is computed between both peak measurements.

DIFFERENTIAL NONLINEARITY

The deviation of any code width from an ideal 1 LSB step.

EFFECTIVE NUMBER OF BITS

The effective number of bits (ENOB) is calculated from the measured SNR based on the equation:

$$ENOB = \frac{SNR_{MEASURED} - 1.76dB}{6.02}$$

ENCODE PULSE WIDTH/DUTY CYCLE

Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing tENCH in text. At a give clock rate, these specs define an acceptable Encode duty cycle.

FULL SCALE INPUT POWER

Expressed in dBm. Computed using the following equation:

$$Power_{Fullscale} = 10\log\left(\frac{\frac{V^2_{Fullscale_{rms}}}{Z_{Input}}}{.001}\right)$$

GAIN ERROR

Gain error is the difference between the measured and ideal full scale input voltage range of the ADC.

HARMONIC DISTORTION, SECOND

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

HARMONIC DISTORTION, THIRD

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

INTEGRAL NONLINEARITY

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

MINIMUM CONVERSION RATE

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

MAXIMUM CONVERSION RATE

The encode rate at which parametric testing is performed.

OUTPUT PROPAGATION DELAY

The delay between a differential crossing of CLK+ and CLK- and

the time when all output data bits are within valid logic levels.

NOISE (FOR ANY RANGE WITHIN THE ADC)

$$V_{noise} = \sqrt{Z * .001 * 10^{\left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10}\right)}}$$

Where Z is the input impedance, FS is the full scale of the device for the frequency in question, SNR is the value for the particular input level and Signal is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

POWER SUPPLY REJECTION RATIO

The ratio of a change in input offset voltage to a change in power supply voltage.

SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

SIGNAL-TO-NOISE RATIO (WITHOUT HARMONICS)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

SPURIOUS-FREE DYNAMIC RANGE (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. It also may be reported in dBc (i.e., degrades as signal level is lowered) or dBFS (i.e., always related back to converter full scale).

TWO-TONE INTERMODULATION DISTORTION REJECTION

The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

TWO-TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. It also may be reported in dBc (i.e., degrades as signal level is lowered) or in dBFS (i.e., always relates back to converter full scale).

WORST OTHER SPUR

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonic) reported in dBc.

TRANSIENT RESPONSE TIME

Transient response time is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

OUT-OF-RANGE RECOVERY TIME

Out of range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

THEORY OF OPERATION

The AD9480 uses a 1.5 bit per stage architecture. The analog inputs drive an integrated high bandwidth track-and-hold circuit that samples the signal prior to quantization by the 8-bit core. For ease of use, the part includes an onboard reference and input logic that accepts TTL, CMOS, or LVPECL levels. The digital output logic levels are user selectable as standard 3 V CMOS or LVDS (ANSI 644-compatible) via pin 30 (S2).

S2 Voltage	Digital Outputs
AVDD (Default)	CMOS Interleaved
2/3 AVDD	CMOS Parallel
AGND	LVDS

Table 6: S2 Voltage Levels

Clocking the AD9480

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer, and any noise, distortion, or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the CLOCK input of the AD9480, and the user is advised to give commensurate thought to the clock source.

The AD9480 has an internal clock duty cycle stabilization circuit that locks to the rising edge of CLOCK (falling edge of CLOCK if driven differentially) and optimizes timing internally for sample rates between 100 and 250 MSPS. This allows for a wide range of input duty cycles at the input without degrading performance. Jitter on the rising edge of the input is still of paramount concern and is not reduced by the internal stabilization circuit. The clock duty cycle stabilizer can be disabled at pin 28 (S1).

S1 Voltage	Data Format	Duty Cycle Stabilizer
AVDD (Default)	Offset Binary	Disabled
2/3 AVDD	Offset Binary	Enabled
1/3 AVDD	Twos Complement	Enabled
AGND	Twos Complement	Disabled

Table 7: S1 Voltage Levels

Driving the Analog Inputs

The analog input to the AD9480 is a differential buffer. For best dynamic performance, impedances at VIN+ and VIN- should match. Optimal performance is obtained with the analog inputs are driven differentially. SNR and SINAD performance will degrade if the analog input is driven with a single-ended signal. A wideband transformer, such as the Minicircuits ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion.

The AD9480 can be configured for a 1 Vpp or 0.5 Vpp input. See the Voltage Reference section for more information. Optimal performance is achieved with a 1 Vpp analog input.

Voltage Reference

A stable and accurate 0.5 V reference is built into the AD9480. Users can choose this internal reference or provide an external reference for greater accuracy and flexibility. The available reference configurations are summarized in Table 8.

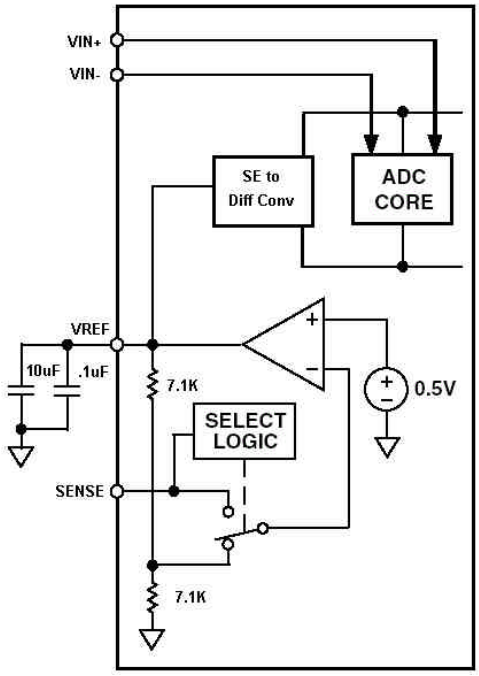


Figure 3 Internal Reference Equivalent Circuit

FIXED REFERENCE

The internal reference can be configured for a differential span of 0.5 Vp-p or 1 Vp-p. Figures 4 and 5 show the two configurations.

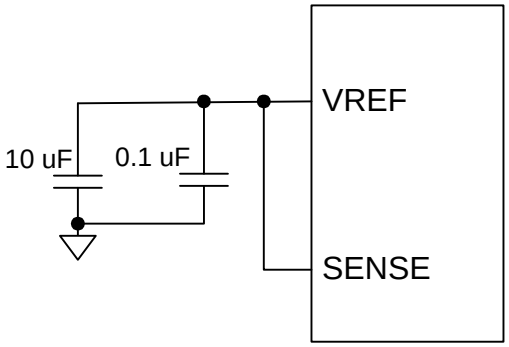


Figure 4 Internal Fixed Reference (0.5 Vpp)

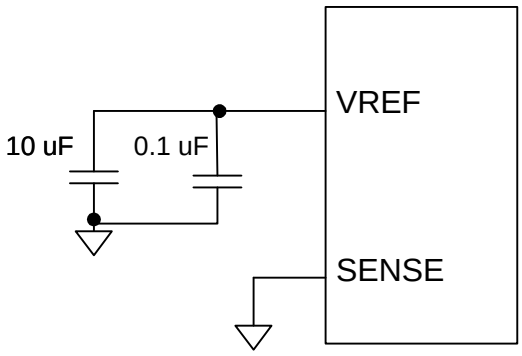


Figure 5 Internal Fixed Reference (1 Vpp)

If the internal reference of the AD9480 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 5 depicts how the internal reference voltage is affected by loading.

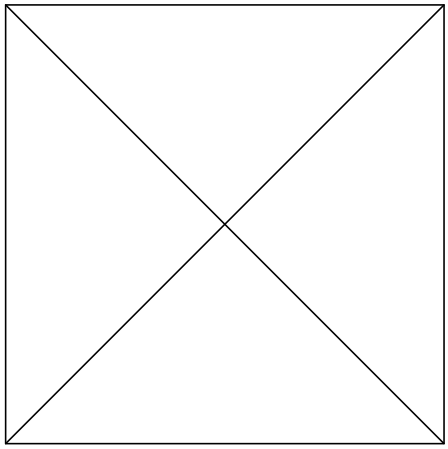


Figure 6 Internal VREF v. Load

EXTERNAL REFERENCE

An external reference can be used for greater accuracy and temperature stability when required. The gain of the AD9480 can also be varied using this configuration. A voltage output DAC can be used to set VREF, providing for a means to digitally adjust the full scale voltage. VREF can be externally set to voltages from 0.5V to 1.1V; optimum performance is obtained at VREF = 1V. *(See TPC section)*

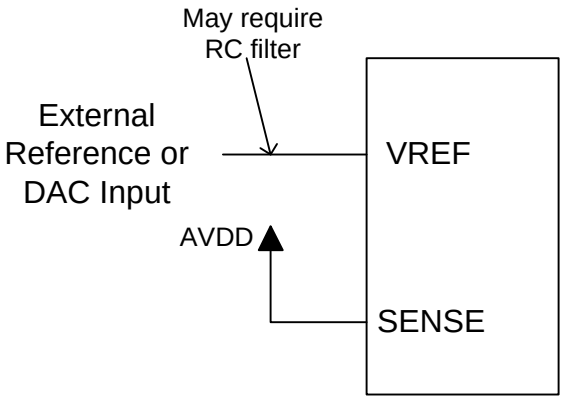


Figure 7 External Reference

PROGRAMMABLE REFERENCE

The programmable reference can be used to set a differential input span anywhere between 0.5 Vpp and 1.1 Vpp. The resulting VREF is equal to 0.5 x (1 + R2/R1).

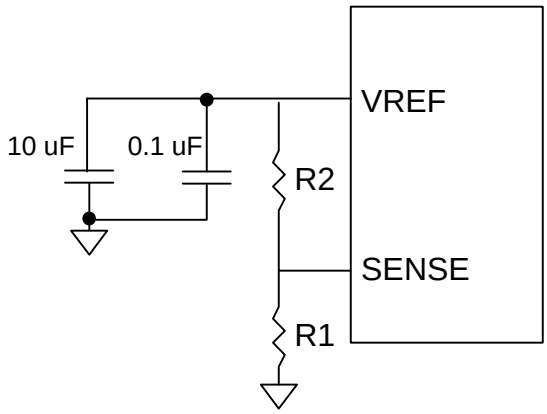


Figure 8 Programmable Reference

SENSE Voltage	Resulting VREF	Mode	Differential Span
AVDD	N/A (External Reference Input)	External Reference	1 x External Reference Voltage
VREF	0.5 V	Internal Fixed Reference	0.5 Vpp
0.2 V to VREF	0.5 x (1+R2/R1) V	Programmable Reference	1 x VREF (0.5 Vpp to 1.1 Vpp)
AGND to 0.2 V	1.0 V	Internal Fixed Reference	1 Vpp

Table 8 : Reference Configuration

Pin	AD9054A Pin Name	AD9480 Pin Name	Connecting the AD9480 for AD9054A-Compatibility
15	VDD	DGND	Pin must be changed to a GND connection
16	GND	DCO-	A data clock out (DCO) was not available on the AD9054A. DCO can be disabled with pin 42 (S3).
17	GND	DCO+	A data clock out (DCO) was not available on the AD9054A. DCO can be disabled with pin 42 (S3).
28	VDD	S1	An output data format select and a duty cycle stabilizer (DCS) were not available on the AD9054A. The AD9054A output data was in binary format. Tie HIGH for binary output data and DCS disabled.
29	GND	PDWN	Power down was not available on the AD9054A. Tie LOW for normal operation.
30	VDD	S2	Tie HIGH for compatibility with the AD9054A. This sets the digital outputs to CMOS Interleaved.
33	VREFOUT	SENSE	Operation is slightly different. See Reference Operation section for more information.
34	VREFIN	VREF	Operation is slightly different. See Reference Operation section for more information.
42	DEMUX	S3	Tie to GND to put DCO+ and DCO- in a high impedance state (pins 16 and 17). DCO+ and DCO- were not available on the AD9054A. On the AD9054A, tying pin 42 to GND selected Single Channel CMOS Mode. This mode is not available on the AD9480.

Table 9: Differences between AD9054A and AD9480

Compatibility with the AD9054A

The AD9480 is pin-similar to the AD9054A, an 8-bit, 200 MSPS ADC with CMOS outputs. Every attempt has been made to keep the pin out of these two ADCs as close as possible. However, to use the AD9480 in place of the AD9054A, a few changes must be made. First, the AD9480 requires a +3.3 V supply in place of a +5 V supply. The AD9480 also includes some additional features that were not available on the AD9054A including LVDS outputs, a data clock out (DCO), power down, data output options, and a flexible reference. Table X provides a summary of the changes to the AD9054A pin out and how to connect the AD9480 to function the same as the AD9054A.

Digital Outputs

The off-chip drivers on the chip can be configured to provide CMOS- or LVDS-compatible output levels via Pin S2. See Table 1 for more information.

The CMOS digital outputs are TTL/CMOS-compatible for lower power consumption. The outputs are biased from a separate supply (DRVDD), allowing easy interface to external logic. The outputs are CMOS devices that will swing from ground to DRVDD (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (<1 inch, for a total CLOAD < 5 pF). When operating in CMOS mode, it is also recommended to place low value series damping resistors on the data lines to reduce switching transient effects on performance.

LVDS OUTPUTS

LVDS outputs are available when pin 30 is tied to ground and a 3.4 kΩ RSET resistor is placed at Pin 42 (LVDSBIAS) to ground. The RSET resistor current (~ 1.2/RSET) is ratioed on-chip setting the output current at each output equal to a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing at the receiver. LVDS mode facilitates interfacing with LVDS receivers in custom ASICs and FPGAs that have LVDS capability for superior switching performance in noisy environments. Single point-to-point net topologies are recommended with a 100 Ω termination resistor as close to the receiver as possible. It is recommended to keep the trace length no longer than 3–4 inches and to keep differential output trace lengths as equal as possible. Note that LVDS mode typically offers superior SFDR performance at higher analog input frequencies compared to CMOS mode operation.

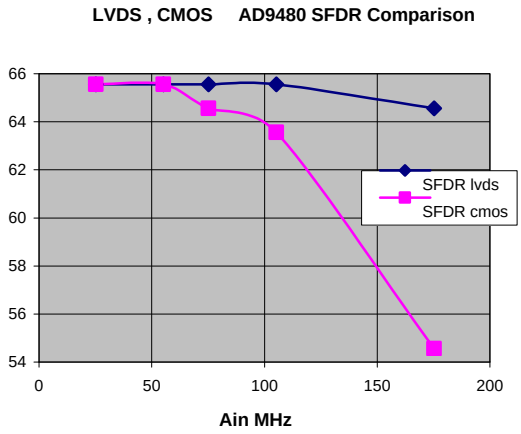


Figure 9 LVDS/CMOS SFDR Comparison

Output Coding

Code	Ain+ - Ain-	Offset Binary	Two's Complement
255	?> 0.512 V	1111 1111	0111 1111
255	0.512 V	1111 1111	0111 1111
254	0.508 V	1111 1110	0111 1110
.	.	.	.
.	.	.	.
129	0.004 V	1000 0001	0000 0001
128	0.0 V	1000 0000	0000 0000
127	–0.004 V	0111 1111	1111 1111
.	.	.	.
.	.	.	.
2	-0.504 V	0000 0010	1000 0010
1	–0.508 V	0000 0001	1000 0001
0	–0.512 V	0000 0000	1000 0000
0	< –0.512 V	0000 0000	1000 0000

Table 10: Output Coding

Data Clock Out

A data clock out is available at DCO+ and DCO- for both CMOS and LVDS outputs. These clocks can facilitate latching off-chip, providing a low skew clocking solution. If the AD9480 is in CMOS mode, the DCO rate is half of the input clock (CLK) rate, and the DCO levels are CMOS. The on-chip clock buffers should not drive more than X pf of capacitance to limit switching transient effects on performance. In LVDS mode, the DCO rate is equal to the input clock rate and the levels are LVDS. Note that in LVDS mode, the DCO requires a 100 Ω differential termination at the receiver.

The DCO is an optional feature. To activate the DCO, tie pin S3 to VDD, as shown in Table X. To disable the DCO, tie S3 to GND. If the DCO is disabled, the DCO outputs are placed in a high impedance state.

Powerdown

The AD9480 can be placed in a low power dissipation state by asserting PDWN (pin 29). Driving PDWN to AVDD places the part in a low power down state where power dissipation is typically less than 15mW. The data outputs go to a high impedance state when PDWN is asserted when operating in LVDS or CMOS mode.

S3 Voltage	Data Clock Out
AVDD	Active
AGND	High impedance

Table 11: S3 Voltage Levels

Interleaving Two AD9480s

Instrumentation applications may prefer to interleave ("ping-pong") two AD9480s to achieve twice the sample rate, or 500 MSPS. In these applications, it is important to match the gain and offset of the two ADCs. Varying the reference voltage allows adjustment of the ADC's gain, external DC Offset compensation can be used to reduce offset mismatch between two ADCs.

DS INPUTS

In CMOS output mode, the Data Sync inputs (DS+, DS–) can be used in applications requiring that a given sample will appear at a specific output port (A or B) relative to a given external timing signal.

The DS inputs can also be used to synchronize two or more ADCs in a system to maintain phasing between Ports A and B on separate ADCs (in effect, synchronizing multiple DCO outputs).

When DS+ is held high (DS– low), the ADC data outputs do not switch and are held static. Synchronization is accomplished by the assertion (falling edge) of DS+ within the timing constraints tSDS and tHDS, relative to a clock rising edge. (On initial synchronization, tHDS is not relevant.) If DS+ falls within the required setup time (tSDS) before a given clock rising edge N, the analog value at that point in time will be digitized and available at Port A, 8 cycles later in interleaved mode. The very next sample, N + 1, will be sampled by the next rising clock edge and available at Port B, 8 cycles after that clock edge. In dual parallel mode, Port A has a 9 cycle latency and Port B has a 8 cycle latency, but data is available at the same time.

Driving each ADC's DS inputs by the same sync signal will accomplish synchronization between multiple ADC's. An easy way to accomplish synchronization is by a one-time sync at power-on reset. Note that when running the AD9480 in LVDS mode, set DS+ to ground and DS– to 3.3 V, as the DS inputs are relevant only in CMOS output mode. LVDS mode can simplify the design for some applications as well as potentially affording superior SNR/SINAD performance at higher encode/analog frequencies

EQUIVALENT CIRCUITS

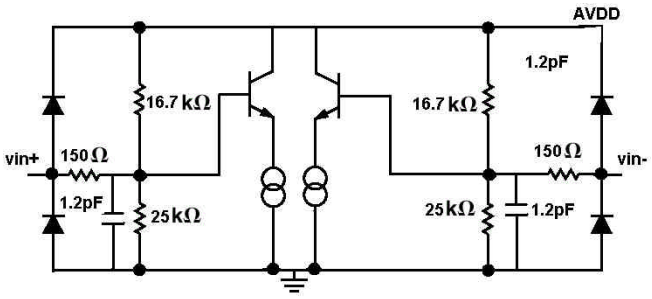


Figure 10 Analog Inputs

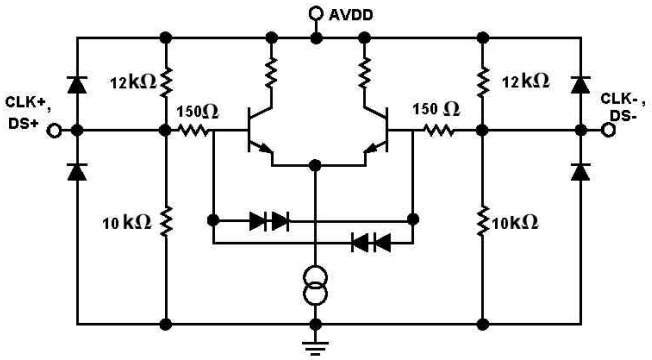


Figure 11 Clock/DS Inputs

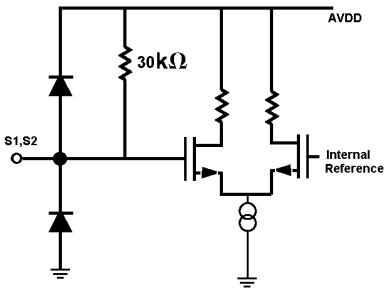


Figure 12 S1,S2 Logic Inputs

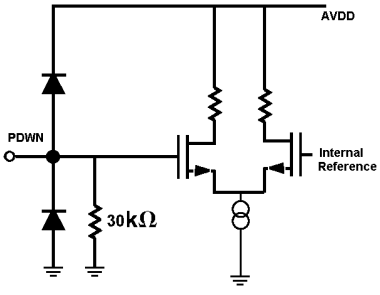


Figure 13 PDWN Input

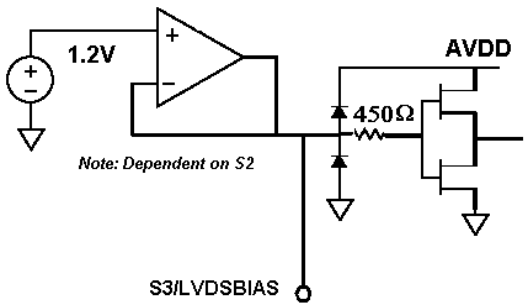


Figure 14 S3/LVDSBIAS Pin

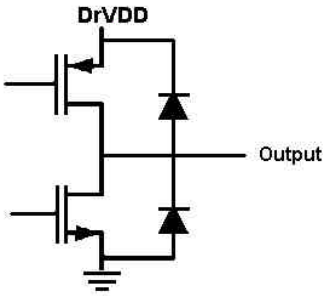


Figure 15 CMOS Outputs

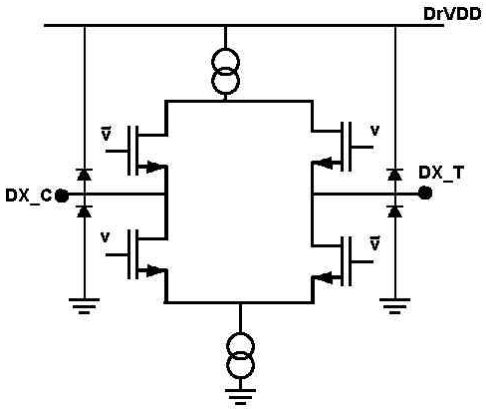


Figure 16 LVDS Outputs

PIN FUNCTION DESCRIPTIONS

LVDS MODE

Pin No.	Name	Description	Pin No.	Name	Description
1	CLK+	Input Clock – True	23	D6_C	Data Output Bit 6 – Complement
2	CLK-	Input Clock – Complement	24	D6_T	Data Output Bit 6 – True
3	AVDD	3.3 V Analog Supply	25	D7_C	Data Output Bit 7 – Complement (MSB)
4	AGND	Analog Ground	26	D7_T	Data Output Bit 7 – True (MSB)
5	DRVDD	3.3 V Digital Output Supply	27	DrGND	Digital Ground
6	DrGND	Digital Ground	28	S1	Data Format Select and Duty Cycle Stabilizer Selection
7	D0_C	Data Ouput Bit 0 – Complement (LSB)	29	PDWN	Power Down Selection
8	D0_T	Data Output Bit 0 – True (LSB)	30	S2	Output Mode State (AGND = LVDS)
9	D1_C	Data Output Bit 1 - Complement	31	AVDD	3.3 V Analog Supply
10	D1_T	Data Output Bit 1 - True	32	AGND	Analog Ground
11	D2_C	Data Output Bit 2 – Complement	33	SENSE	Reference Mode Selection
12	D2_T	Data Output Bit 2 – True	34	VREF	Voltage Reference Input/Output
13	D3_C	Data Output Bit 3 – Complement	35	AGND	Analog Ground
14	D3_T	Data Output Bit 3 – True	36	AVDD	3.3 V Analog Supply
15	DrGND	Digital Ground	37	AGND	Analog Ground
16	DCO-	Data Clock Output – Complement	38	VIN-	Analog Input – Complement
17	DCO+	Data Clock Output – True	39	VIN+	Analog Input – True
18	DRVDD	3.3 V Digital Output Supply	40	AGND	Analog Ground
19	D4_C	Data Output Bit 4 – Complement	41	AVDD	3.3 V Analog Supply
20	D4_T	Data Output Bit 4 – True	42	LVDSBIAS	LVDS Output Current
21	D5_C	Data Output Bit 5 – Complement	43	DS-	Data Sync Complement (Not Used in LVDS Mode, Tie to DRVDD)
22	D5_T	Data Output Bit 5 - True	44	DS+	Data Sync True (Not Used in LVDS Mode, Tie to DGND)

Table 12: Pin Function Descriptions — LVDS Mode

CMOS MODE

Pin No.	Name	Description	Pin No.	Name	Description
1	CLK+	Input Clock – True	23	D4B	Data Output Bit 4 – Channel B
2	CLK-	Input Clock – Complement	24	D5B	Data Output Bit 5 – Channel B
3	AVDD	3.3 V Analog Supply	25	D6B	Data Output Bit 6 – Channel B
4	AGND	Analog Ground	26	D7B	Data Output Bit 7 – Channel B (MSB)
5	DRVDD	3.3 V Digital Output Supply	27	DrGND	Digital Ground
6	DrGND	Digital Ground	28	S1	Data Format Select and Duty Cycle Stabilizer Select
7	D7A	Data Output Bit 7 – Channel A (MSB)	29	PDWN	Power Down Selection
8	D6A	Data Output Bit 6 – Channel A	30	S2	Output Mode State
9	D5A	Data Output Bit 5 – Channel A	31	AVDD	3.3 V Analog Supply
10	D4A	Data Output Bit 4 – Channel A	32	AGND	Analog Ground
11	D3A	Data Output Bit 3 – Channel A	33	SENSE	Reference Mode Selection
12	D2A	Data Output Bit 2 – Channel A	34	VREF	Voltage Reference Input/Output
13	D1A	Data Output Bit 1 – Channel A	35	AGND	Analog Ground
14	D0A	Data Output Bit 0 – Channel A (LSB)	36	AVDD	3.3 V Analog Supply
15	DrGND	Digital Ground	37	AGND	Analog Ground
16	DCO-	Data Clock Output – Complement	38	VIN-	Analog Input – Complement
17	DCO+	Data Clock Output – True	39	VIN+	Analog Input – True
18	DRVDD	3.3 V Digital Output Supply	40	AGND	Analog Ground
19	D0B	Data Output Bit 0 – Channel B (LSB)	41	AVDD	3.3 V Analog Supply
20	D1B	Data Output Bit 1 – Channel B	42	S3	DCO Enable Select
21	D2B	Data Output Bit 2 – Channel B	43	DS-	Data Sync Complement (If Unused, tie to DRVDD)
22	D3B	Data Output Bit 3 – Channel B	44	DS+	Data Sync True (If Unused, Tie to DGND)

Table 13: Pin Function Descriptions – CMOS Mode

PIN CONFIGURATIONS

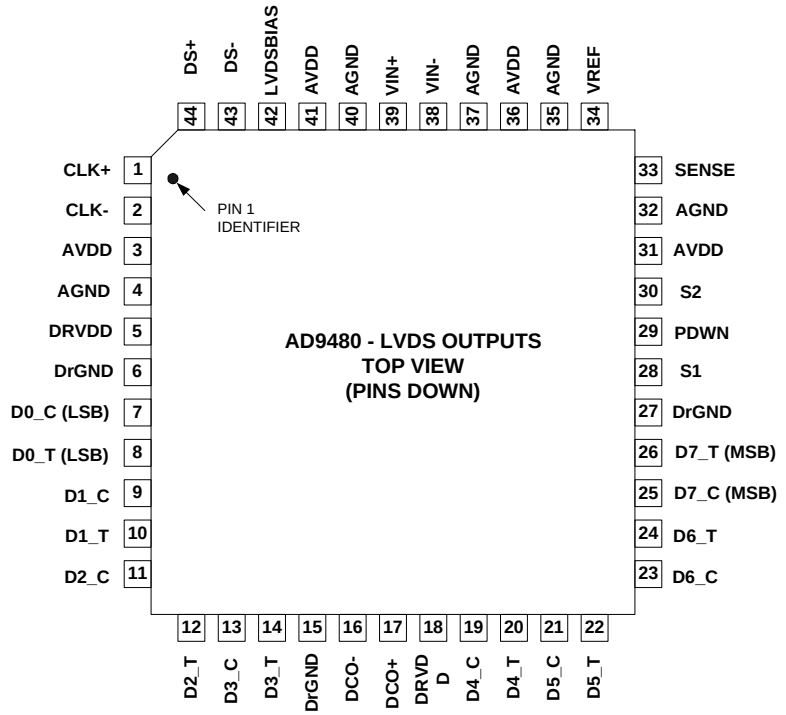


Figure 17 LVDS Mode

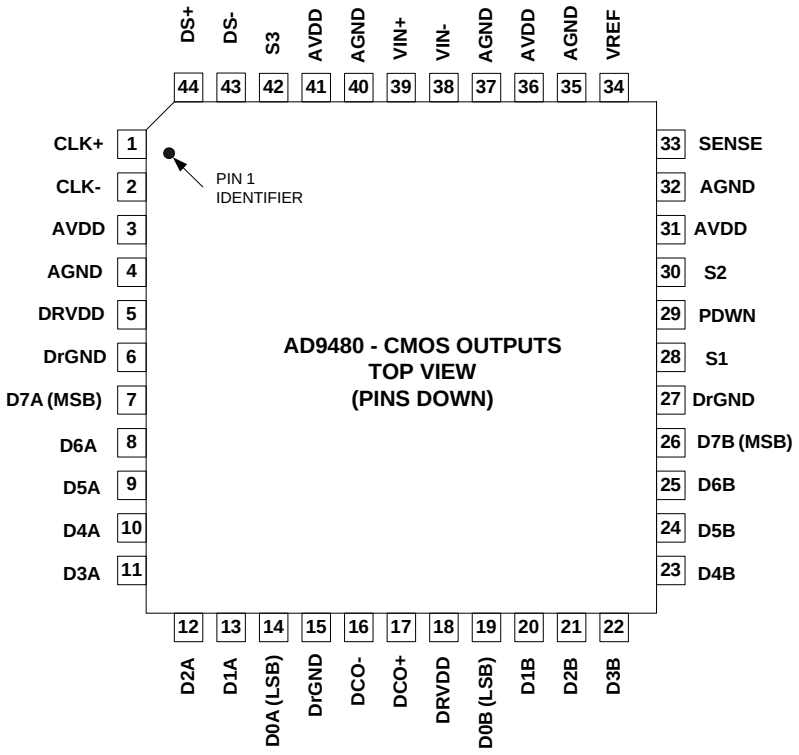
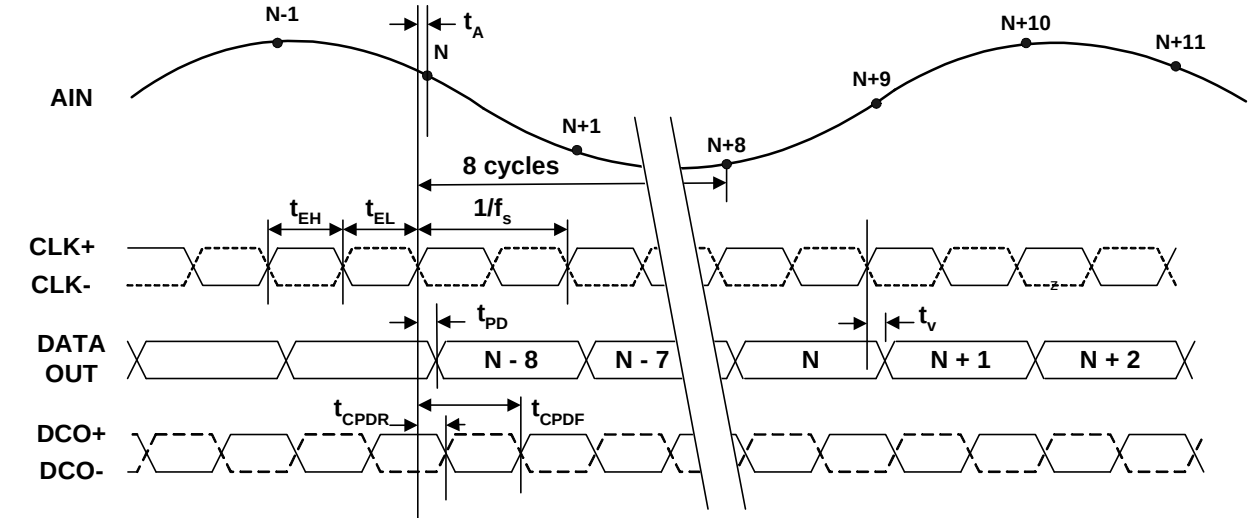


Figure 18 CMOS Mode

TIMING DIAGRAM

LVDS Timing:



Demuxed CMOS Timing:

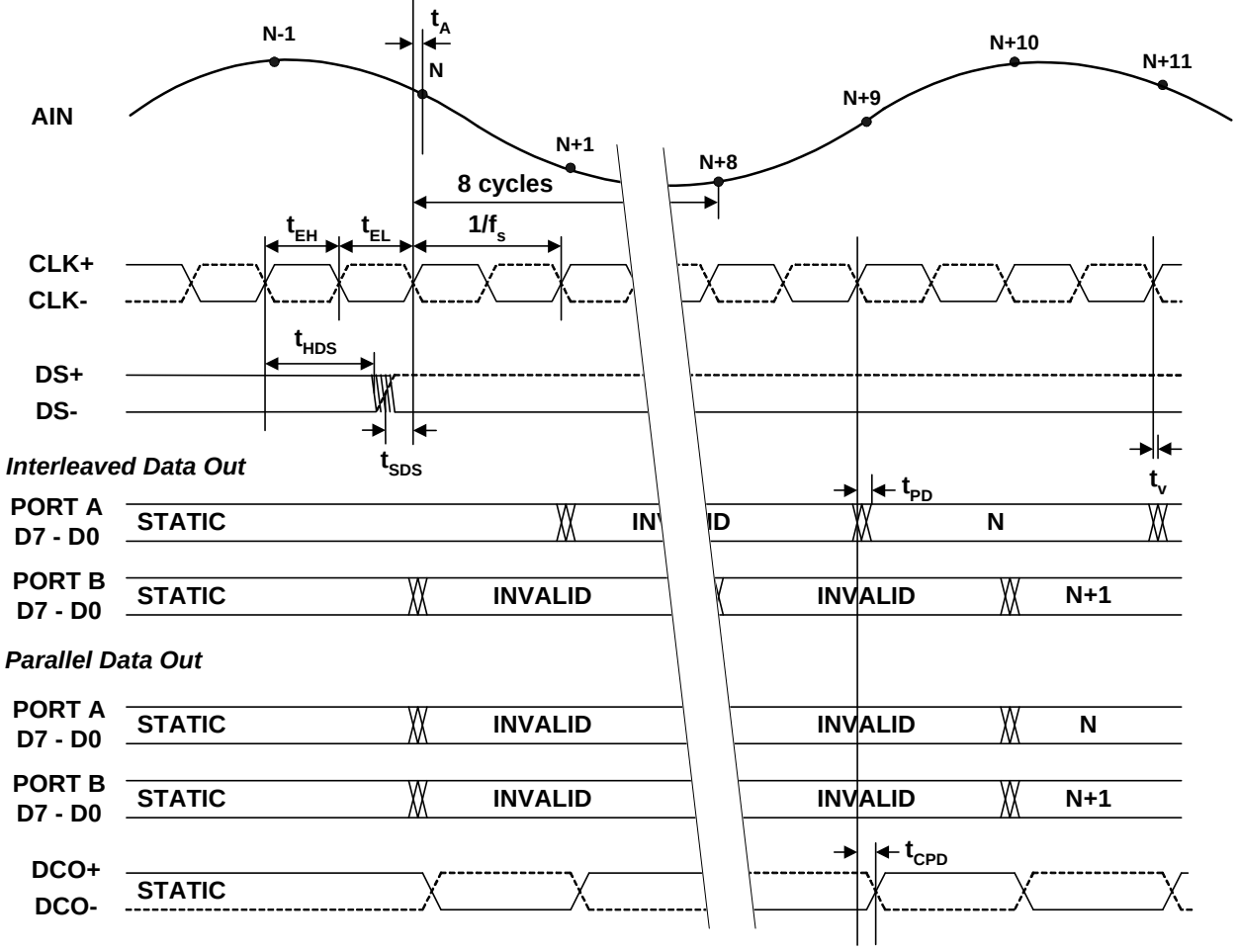


Figure 19 Timing Diagram

OUTLINE DIMENSIONS

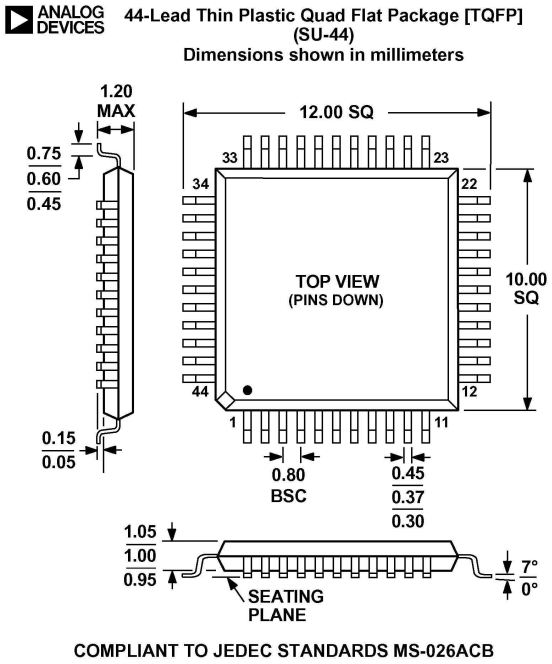


Figure 20 Mechanical Drawing

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

Model	Temperature Range	Description
AD9480BSU-250	-40°C to +85°C (Ambient)	44-pin TQFP
AD9480BSU-250EB	25°C (Ambient)	Evaluation Board

Table 14: Ordering Guide

ANALOG DEVICES

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