

1 Megabit (128K x 8) SuperFlash MTP

SST27SF010



Preliminary Specifications

FEATURES:

- **5.0-Volt Read Operation (4.5V to 5.5V)**
- **Superior Reliability**
 - Endurance: Minimum 1000 Cycles
 - Greater than 100 years Data Retention
- **Low Power Consumption**
 - Active Current: 20 mA (typical)
 - Standby Current: 10 μ A (typical)
- **Fast Access Time**
 - 70 and 90 ns
- **Fast Programming Operation**
 - 20 μ s per byte
 - 2.8 second for the entire chip
- **Features Electrical Erase**
 - Does Not Require UV Source
 - Chip Erase Time: 100 ms
- **TTL I/O Compatibility**
- **JEDEC Standard Byte-wide EPROM Pinouts**
- **12V Power Supply for Programming/Erase**
- **Packages Available**
 - 32-Pin PLCC
 - 32-Pin Plastic DIP
 - 32-Pin TSOP (8mm x 14mm)

PRODUCT DESCRIPTION

The SST27SF010 is a 128K x 8 CMOS, many-time programmable (MTP) low cost flash, manufactured with SST's proprietary, high performance SuperFlash technology. The split gate cell design and thick oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST27SF010 can be electrically erased and programmed at least 1000 times using an external programmer with a 12 volt supply. The SST27SF010 has to be erased prior to programming. The SST27SF010 conforms to JEDEC standard pinouts for byte-wide memories.

Featuring high performance byte programming, the SST27SF010 provides a byte-program time of 20 μ s. The entire memory can be programmed byte by byte in 2.8 seconds. Designed, manufactured, and tested for a wide spectrum of applications, the SST27SF010 is offered with a minimum endurance of 1000 cycles. Data retention is rated at greater than 100 years.

The SST27SF010 is suited for applications that require infrequent writes and low power nonvolatile storage. The SST27SF010 will improve flexibility, efficiency, and performance while matching the low cost in nonvolatile applications that currently use UV-EPROMs, OTPs, and mask ROMs.

To meet surface mount and conventional through hole requirements, the SST27SF010 is offered in 32-pin PLCC, 32-pin PDIP and 32-pin TSOP packages. See Figures 1 and 2 for pinouts.

Device Operation

The SST27SF010 is a low cost flash solutions that can be used to replace existing UV-EPROM, OTP, and mask ROM sockets. They are functionally (read and program) and pin compatible with industry standard EPROM products. In addition to EPROM functionality, the device also supports electrical erase operation via an external programmer. The SST27SF010 does not require a UV source to erase, and therefore the packages do not have a window.

Read

The Read operation of the SST27SF010 is controlled by CE# and OE#. Both CE# and OE# have to be low for the system to obtain data from the outputs. Once the address is stable, the address access time is equal to the delay from CE# to output (T_{CE}). Data is available at the output after a delay of T_{OE} from the falling edge of OE#, assuming that CE# pin has been low and the addresses have been stable for at least $T_{CE} - T_{OE}$. When the CE# pin is high, the chip is deselected and a typical standby current of 10 μ A is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high.

Programming operation

The SST27SF010 is programmed by using an external programmer. The programming mode is activated by asserting 12V ($\pm 5\%$) on V_{PP} pin, $V_{CC} = 5V \pm 5\%$, V_{IL} on CE# pin, and V_{IH} on OE# pin. The device is programmed byte by byte with the desired data at the desired address using a single pulse (PGM# pin low) of 20 μ s. Using the



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MTP programming algorithm, the byte programming process continues byte by byte until the entire chip (128K bytes) has been programmed.

Chip Erase Operation

The only way to change a data from a “0” to “1” is by electrical erase that changes every bit in the device to “1”. Unlike traditional EPROMs, which use UV light to do the chip erase, the SST27SF010 uses an electrical chip erase operation. This saves a significant amount of time (about 30 minutes for each erase operation). The entire chip can be erased in a single pulse of 100 ms (PGM# pin low). In order to activate the erase mode, the 12V ($\pm 5\%$) is applied to V_{PP} and A_9 pins, $V_{CC} = 5V \pm 5\%$, V_{IL} on $CE\#$ pin, and V_{IH} on $OE\#$ pin. All other address and data pins are “don’t care”. The falling edge of PGM# will start the Chip Erase operation. Once the chip has been erased, all bytes must be verified for FF. Refer to figure 8 for the flow chart.

The SST27SF010 can also be reprogrammed in the system. This requires the availability of 12V for V_{PP} to program and an additional 12V for address A_9 to erase.

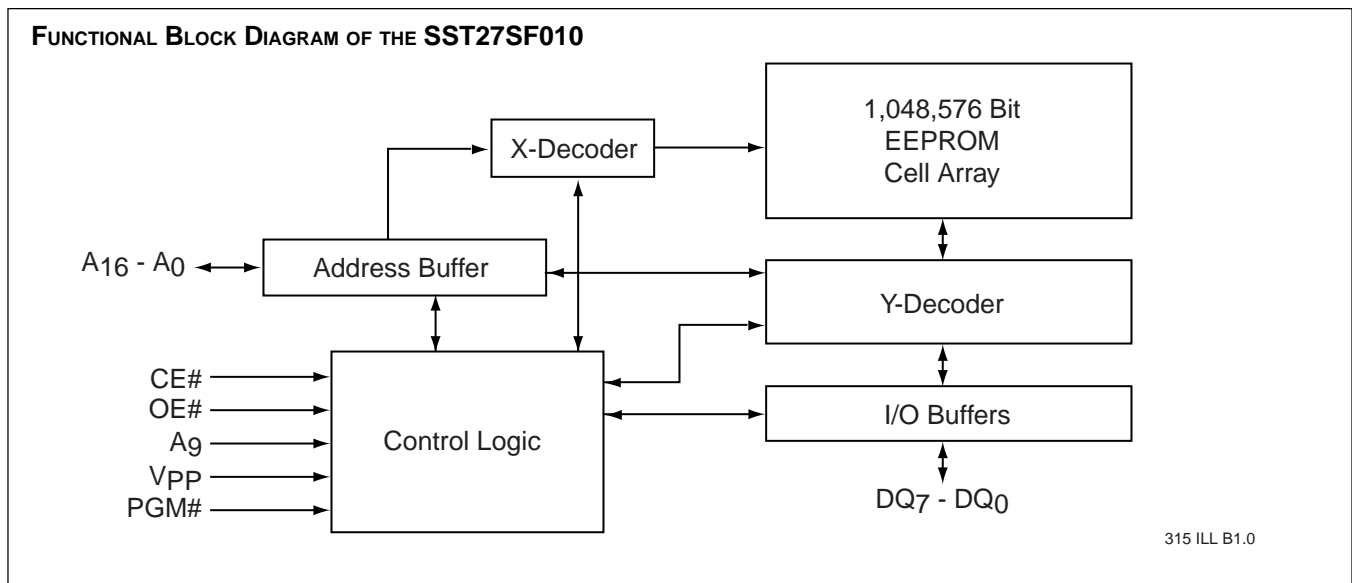
Product Identification Mode

The product identification mode identifies the device as the SST27SF010 and manufacturer as SST. This mode may be accessed by the hardware method. To activate this mode, the programming equipment must force V_H ($12V \pm 5\%$) on address A_9 with V_{PP} pin at $5V \pm 10\%$. Two identifier bytes may then be sequenced from the device outputs by toggling address line A_0 . For details, see Table 3 for hardware operation.

TABLE 1: PRODUCT IDENTIFICATION TABLE

	Byte	Data
Manufacturer's Code	0000 H	BF H
Device Code	0001 H	A5 H

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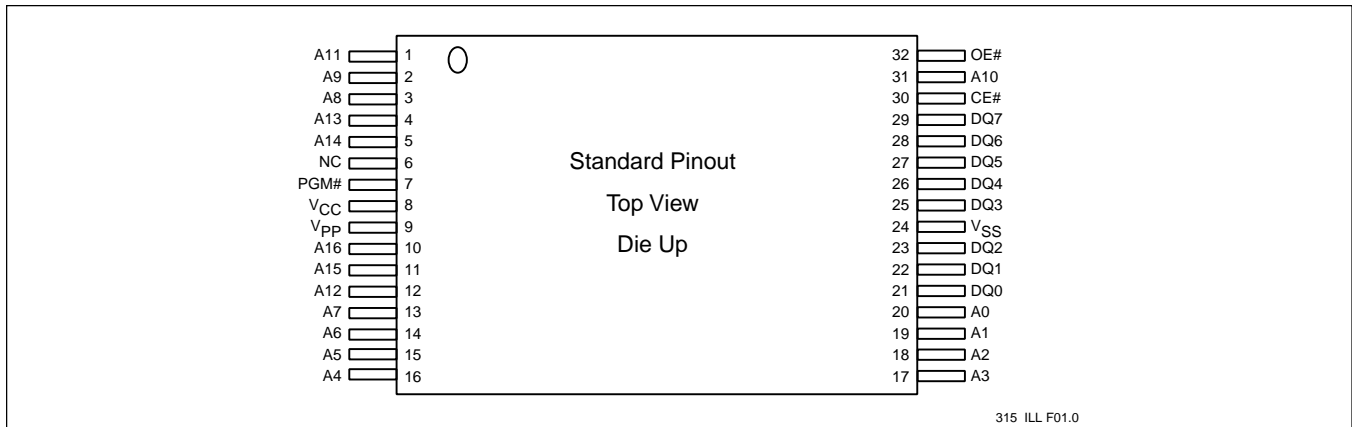


FIGURE 1: PIN ASSIGNMENTS FOR 32-PIN TSOP PACKAGES

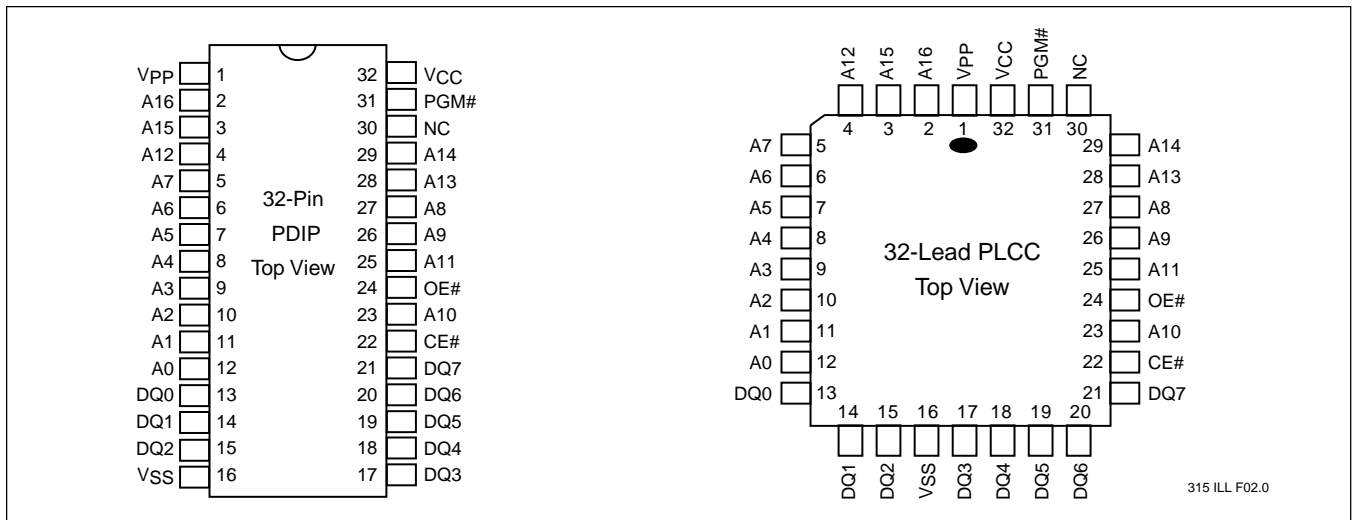


FIGURE 2: PIN ASSIGNMENTS FOR 32-PIN PLASTIC DIPs AND 32-LEAD PLCCs

TABLE 2: PIN DESCRIPTION

Symbol	Pin Name	Functions
A ₁₆ -A ₀	Address Inputs	To provide memory addresses
DQ ₇ -DQ ₀	Data Input/Output	To output data during read cycles and receive input data during program cycle, the outputs are in tri-state when OE# or CE# is high
CE#	Chip Enable	To activate the device when CE# is low
OE#	Output Enable	To gate the data output buffers during read operation
PGM#	Program/Erase Pin	Used for program or erase (PGM# = V _{IL} pulse during program or erase)
V _{PP}	Power Supply for Program or Erase	High voltage pin during chip erase and programming operation 12-volt (±5%)
V _{CC}	Power Supply	To provide 5-volt supply (±10%)
V _{SS}	Ground	
NC	No Connection	Unconnected pins

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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	PGM#	A ₉	V _{PP}	DQ	Address
Read	V _{IL}	V _{IL}	X	A _{IN}	V _{CC} or V _{SS}	D _{OUT}	A _{IN}
Output Disable	V _{IL}	V _{IH}	X	X	V _{CC} or V _{SS}	High Z	A _{IN}
Program	V _{IL}	V _{IH}	V _{IL}	A _{IN}	V _{PPH}	D _{IN}	A _{IN}
Standby	V _{IH}	X	X	X	V _{CC} or V _{SS}	High Z	X
Chip Erase	V _{IL}	V _{IH}	V _{IL}	V _H	V _{PPH}	High Z	X
Program/Erase Inhibit	V _{IH}	X	X	X	V _{PPH}	High Z	X
Product Identification	V _{IL}	V _{IL}	X	V _H	V _{CC} or V _{SS}	Manufacturer Code (BF) Device Code A5	A ₁₆ -A ₁ = V _{IL} , A ₀ = V _{IL} A ₁₆ -A ₁ = V _{IL} , A ₀ = V _{IH}

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Note: X = V_{IL} or V_{IH}
V_{PPH} = 12V±5%, V_H = 12V±5%

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to V _{CC} + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-1.0V to V _{CC} + 1.0V
Voltage on A ₉ and V _{PP} Pin to Ground Potential	-0.5V to 14.0V
Package Power Dissipation Capability (T _A = 25°C)	1.0W
Through Hole Lead Soldering Temperature (10 Seconds)	300°C
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ⁽¹⁾	100 mA

Note: ⁽¹⁾ Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V _{CC}
Commercial	0°C to +70°C	5V±10%
Industrial	-40°C to +85°C	5V±10%

AC CONDITIONS OF TEST

Input Rise/Fall Time	10 ns
Output Load	1 TTL Gate and C _L = 100 pF
See Figures 6 and 7	



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TABLE 4: READ MODE DC OPERATING CHARACTERISTICS

$V_{CC} = 5 V \pm 10\%$, $T_A = 0^\circ C$ to $70^\circ C$ (Commercial) or $-40^\circ C$ to $+85^\circ C$ (Industrial)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I _{CC}	V _{CC} Read Current		30	mA	CE# = OE# = V _{IL} all I/Os open, Address Input = V _{IL} /V _{IH} at f = 1/T _{RC} Min, V _{CC} = V _{CC} Max
I _{PPR}	V _{PP} Read Current		100	μA	CE# = OE# = V _{IL} , all I/Os open, Address Input = V _{IL} /V _{IH} at f = 1/T _{RC} Min, V _{CC} = V _{CC} Max, V _{PP} = V _{CC}
I _{SB1}	Standby V _{CC} Current (TTL input)		3	mA	CE# = OE# = V _{IH} , V _{CC} = V _{CC} Max
I _{SB2}	Standby V _{CC} Current (CMOS input)		50	μA	CE# = OE# = V _{CC} - 0.3V V _{CC} = V _{CC} Max.
I _{LI}	Input Leakage Current		1	μA	V _{IN} = GND to V _{CC} , V _{CC} = V _{CC} Max
I _{LO}	Output Leakage Current		10	μA	V _{OUT} = GND to V _{CC} , V _{CC} = V _{CC} Max
V _{IL}	Input Low Voltage		0.8	V	V _{CC} = V _{CC} Max
V _{IH}	Input High Voltage	2.0	V _{CC} +0.5	V	V _{CC} = V _{CC} Max
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2.1 mA, V _{CC} = V _{CC} Min
V _{OH}	Output High Voltage	2.4		V	I _{OH} = -400μA, V _{CC} = V _{CC} Min
I _H	Supervoltage Current for A ₉		100	μA	CE# = OE# = V _{IL} , A ₉ = V _H Max.

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TABLE 5: PROGRAM/ERASE DC OPERATING CHARACTERISTICS

$V_{CC} = 5 V \pm 10\%$, $V_{PP} = V_{PPH}$, $T_A = 25^\circ C \pm 5^\circ C$

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I _{CP}	V _{CC} Erase or Program Current		30	mA	CE# = V _{IL} , V _{PP} = 12V±5%, V _{CC} = V _{CC} Max
I _{PP}	V _{PP} Erase or Program Current		1	mA	CE# = V _{IL} , V _{PP} = 12V±5%, V _{CC} = V _{CC} Max
I _{LI}	Input Leakage Current		1	µA	V _{IN} = GND to V _{CC} , V _{CC} = V _{CC} Max
I _{LO}	Output Leakage Current		10	µA	V _{OUT} = GND to V _{CC} , V _{CC} = V _{CC} Max
V _H	Supervoltage for A ₉	11.4	12.6	V	CE# = OE# = V _{IL}
I _H	Supervoltage Current for A ₉		100	µA	CE# = OE# = V _{IL} , A ₉ = V _H Max
V _{PPH}	High Voltage for V _{PP} Pin	11.4	12.6	V	

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TABLE 6: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Maximum	Units
T _{PU-READ}	Power-up to Read Operation	100	µs

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TABLE 7: CAPACITANCE (T_A = 25 °C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
C _{I/O} ⁽¹⁾	I/O Pin Capacitance	V _{I/O} = 0V	12 pF
C _{IN} ⁽¹⁾	Input Capacitance	V _{IN} = 0V	6 pF

315 PGM T7.0

Note: ⁽¹⁾This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N _{END}	Endurance	1000	Cycles	MIL-STD-883, Method 1033
T _{DR} ⁽¹⁾	Data Retention	100	Years	JEDEC Standard A103
V _{ZAP_HBM} ⁽¹⁾	ESD Susceptibility Human Body Model	1000	Volts	JEDEC Standard A114
V _{ZAP_MM} ⁽¹⁾	ESD Susceptibility Machine Model	300	Volts	JEDEC Standard A115
I _{LTH} ⁽¹⁾	Latch Up	100	mA	JEDEC Standard 78

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Note: ⁽¹⁾ This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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AC CHARACTERISTICS

TABLE 9: READ CYCLE TIMING PARAMETERS

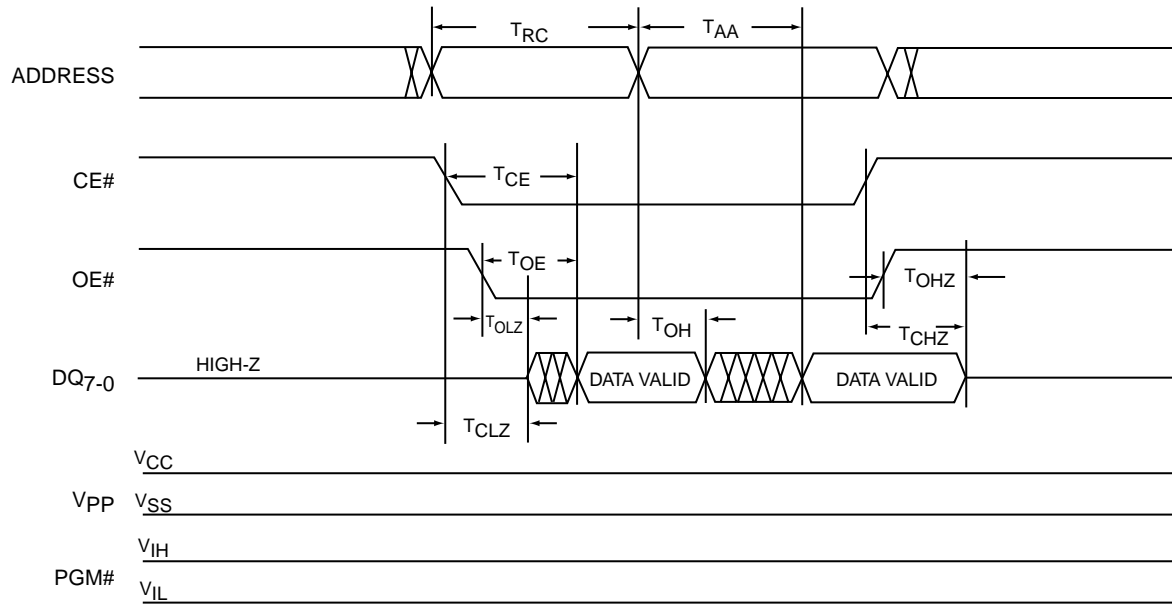
Symbol	Parameter	SST27SF010-70		SST27SF010-90		Units
		Min	Max	Min	Max	
T _{RC}	Read Cycle Time	70		90		ns
T _{CE}	Chip Enable Access Time		70		90	ns
T _{AA}	Address Access Time		70		90	ns
T _{OE}	Output Enable Access Time		30		40	ns
T _{CLZ} ⁽¹⁾	CE# Low to Active Output	0		0		ns
T _{OLZ} ⁽¹⁾	OE# Low to Active Output	0		0		ns
T _{CHZ} ⁽¹⁾	CE# High to High-Z Output		25		30	ns
T _{OHZ} ⁽¹⁾	OE# High to High-Z Output		25		30	ns
T _{OH} ⁽¹⁾	Output Hold from Address Change	0		0		ns

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TABLE 10: PROGRAMMING/ERASE CYCLE TIMING PARAMETERS

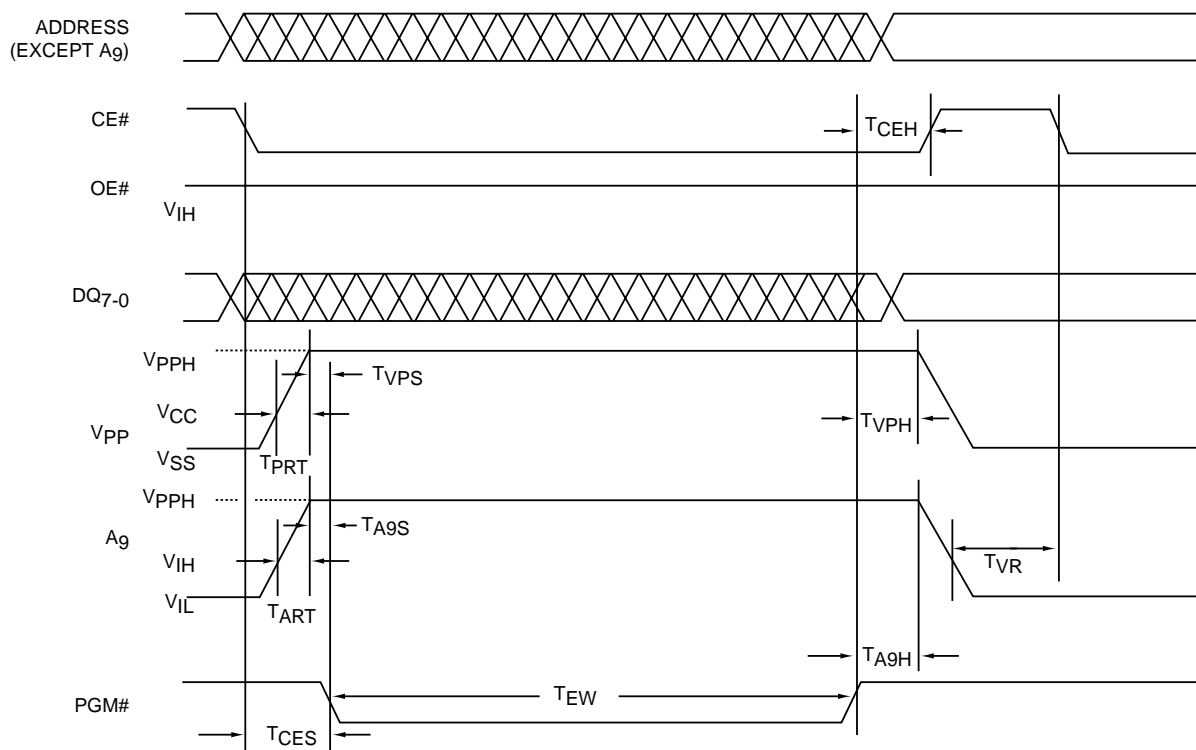
Symbol	Parameter	Min	Max	Units
T _{CES}	CE# Setup Time	2		μs
T _{CEH}	CE# Hold Time	2		μs
T _{AS}	Address Setup Time	2		μs
T _{AH}	Address Hold Time	2		μs
T _{PRT}	V _{PP} Pulse Rise Time	50		ns
T _{VPS}	V _{PP} Setup Time	2		μs
T _{VPH}	V _{PP} Hold Time	2		μs
T _{PW}	PGM# Program Pulse Width	20	40	μs
T _{EW}	PGM# Erase Pulse Width	100	500	ms
T _{DS}	Data Setup Time	2		μs
T _{DH}	Data Hold Time	2		μs
T _{VR}	A ₉ Recovery Time for Erase	2		μs
T _{ART}	A ₉ Rise Time to 12V during Erase	50		ns
T _{A9S}	A ₉ Setup Time during Erase	2		μs
T _{A9H}	A ₉ Hold Time during Erase	2		μs

315 PGM T10.0



315 ILL F03.0

FIGURE 3: READ CYCLE TIMING DIAGRAM



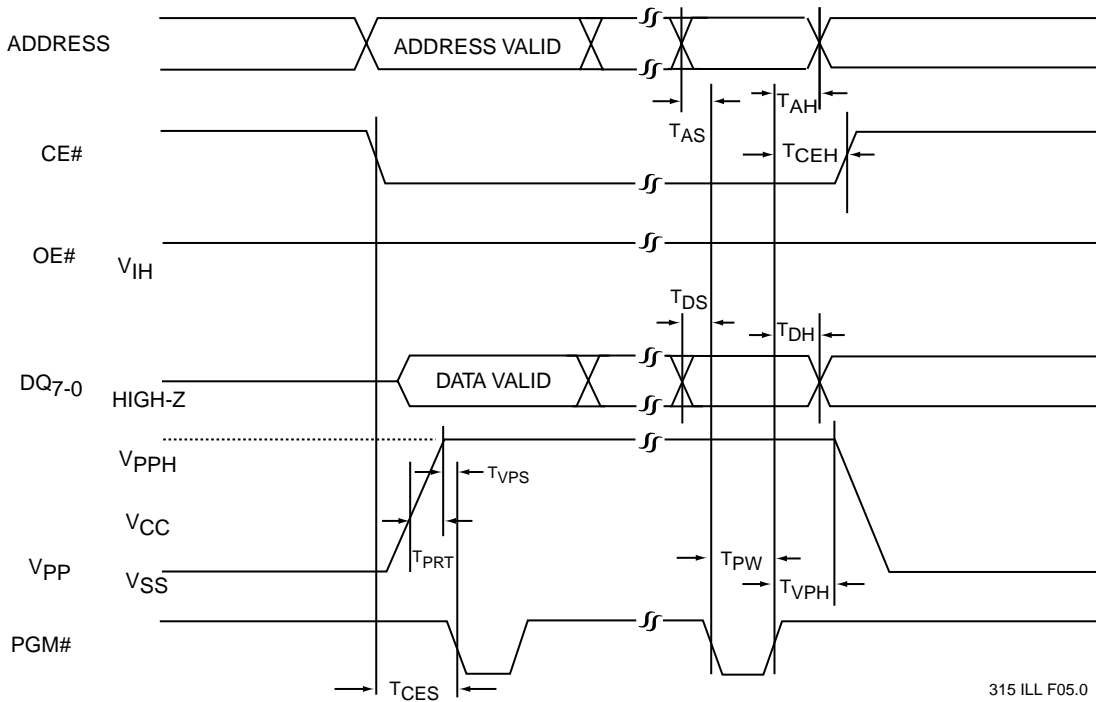
315 ILL F04.0

FIGURE 4: ERASE TIMING DIAGRAM



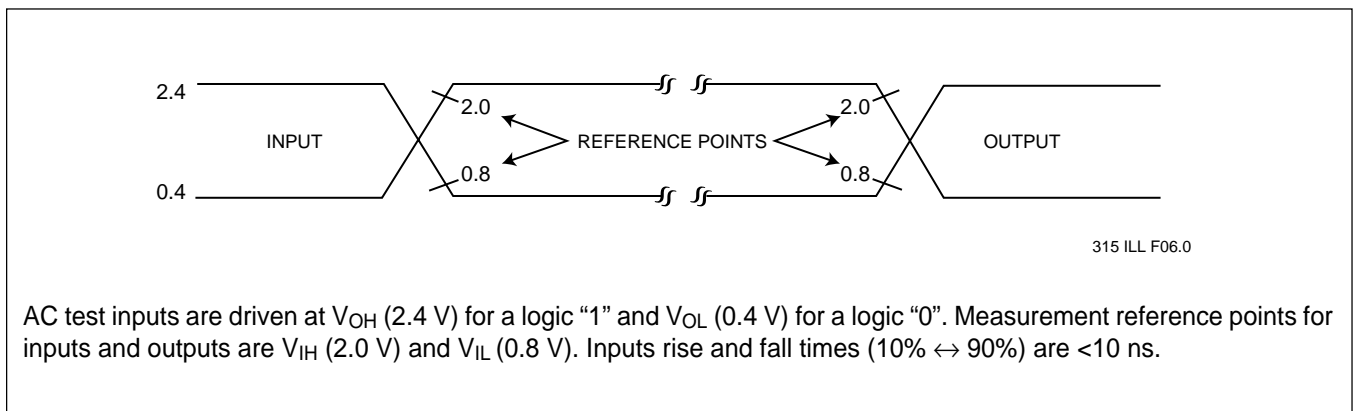
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315 ILL F05.0

FIGURE 5: PROGRAM TIMING DIAGRAM



315 ILL F06.0

AC test inputs are driven at V_{OH} (2.4 V) for a logic "1" and V_{OL} (0.4 V) for a logic "0". Measurement reference points for inputs and outputs are V_{IH} (2.0 V) and V_{IL} (0.8 V). Inputs rise and fall times (10% \leftrightarrow 90%) are <10 ns.

FIGURE 6: AC INPUT/OUTPUT REFERENCE WAVEFORMS

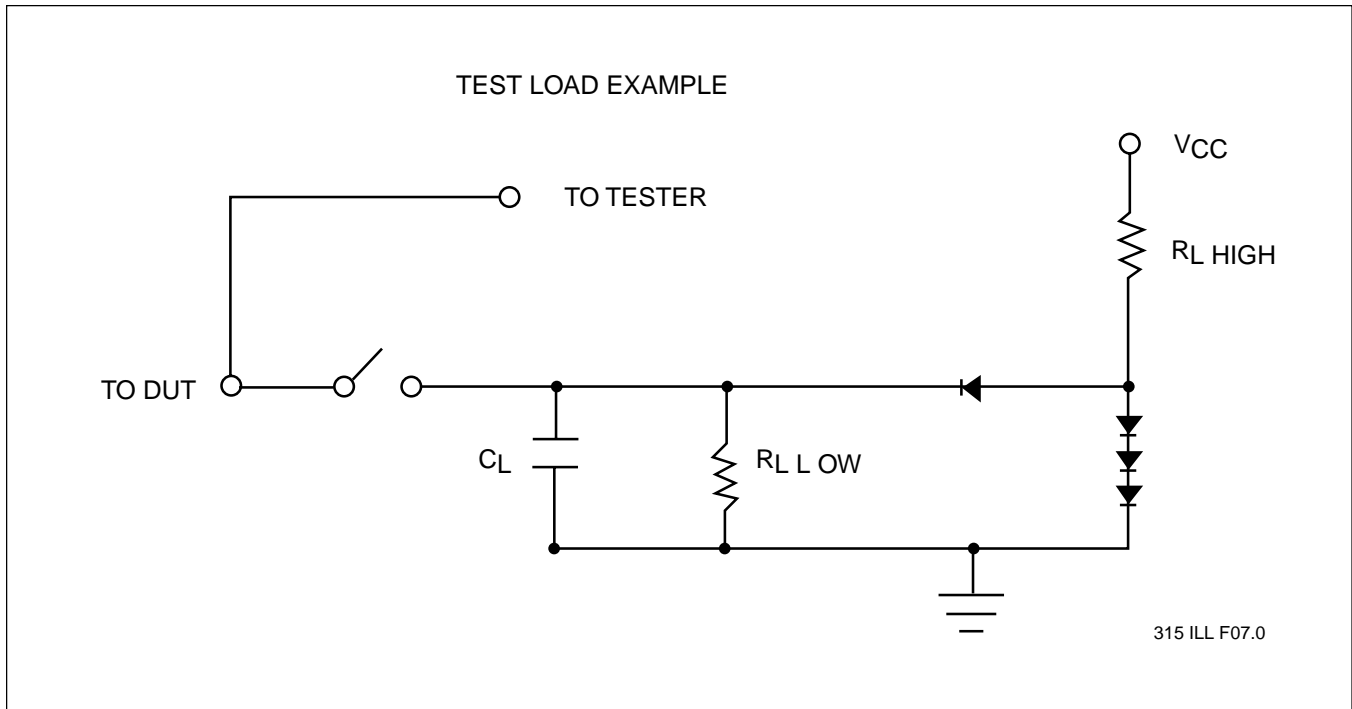


FIGURE 7: TEST LOAD EXAMPLE



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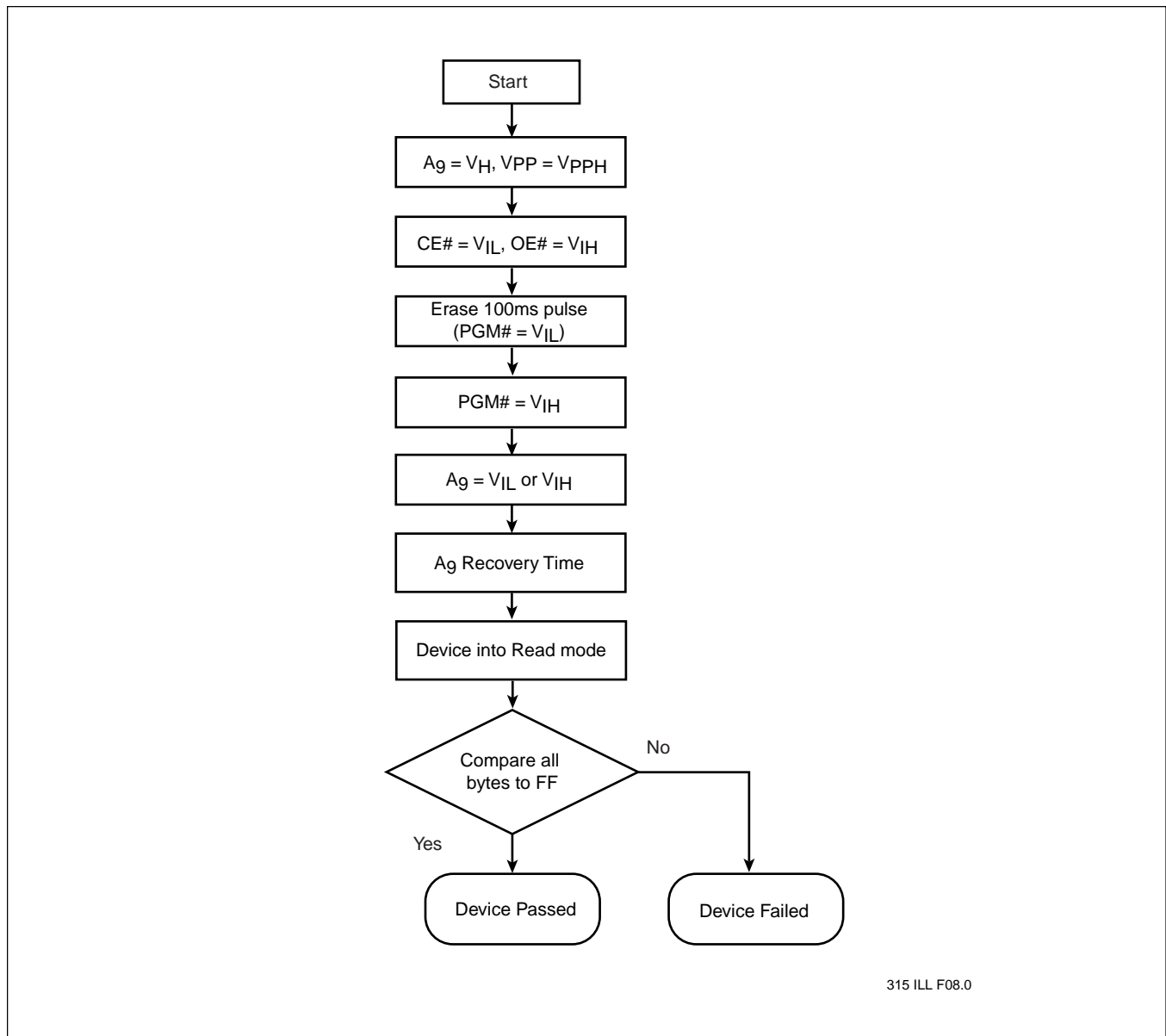
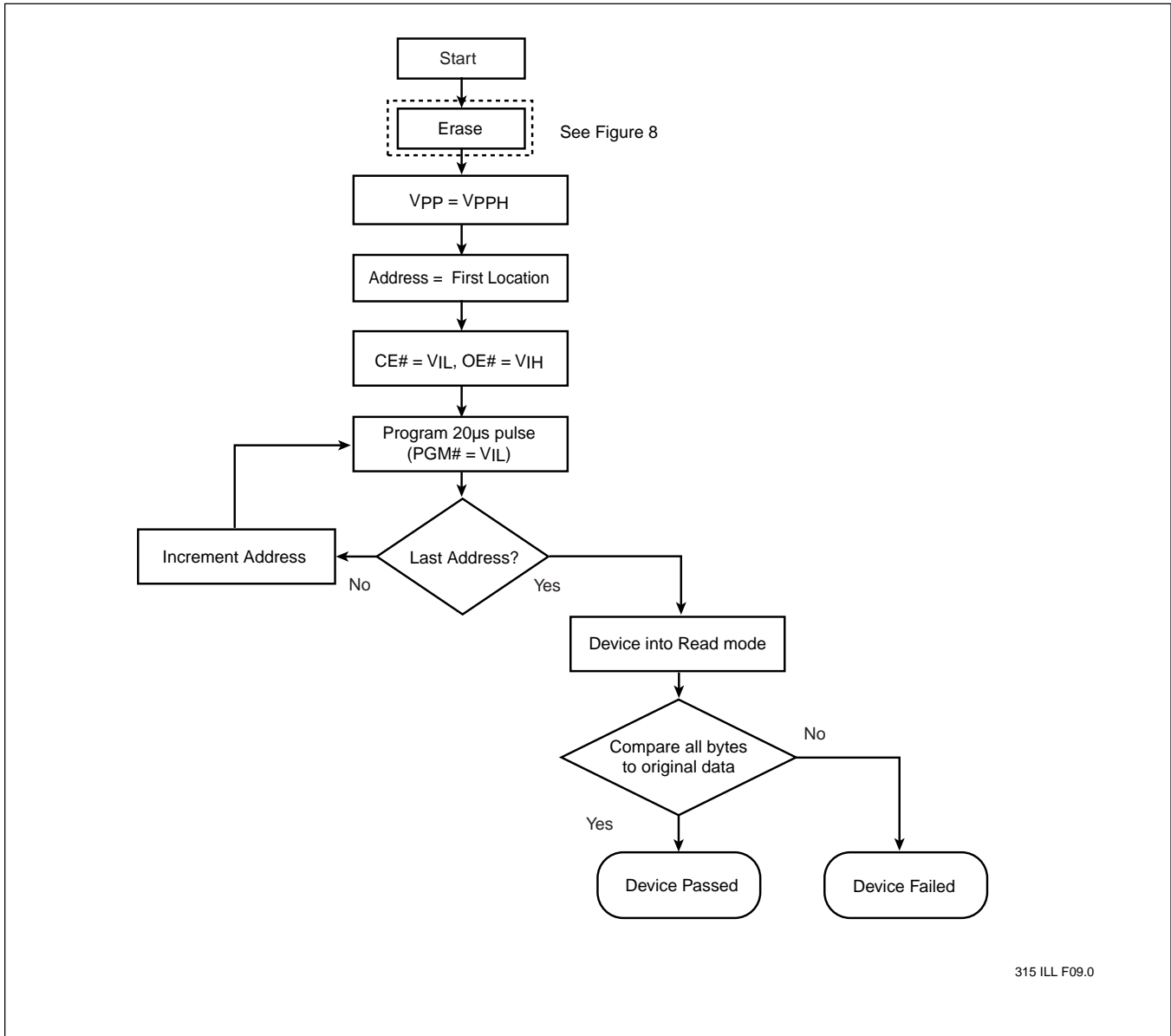


FIGURE 8: ERASE ALGORITHM



315 ILL F09.0

FIGURE 9: PROGRAMMING ALGORITHM



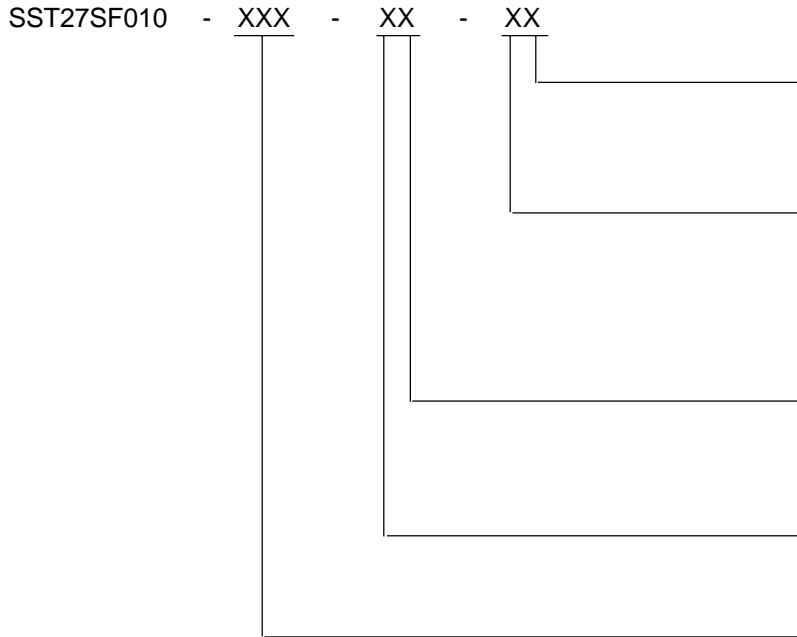
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PRODUCT ORDERING INFORMATION

Device Speed Suffix1 Suffix2



Package Modifier

H = 32 leads
 Numeric = Die modifier

Package Type

P = PDIP
 N = PLCC
 W = TSOP (die up) (8mm x 14mm)
 U = Unencapsulated die

Operating Temperature

C = Commercial = 0° to 70°C
 I = Industrial = -40° to 85°C

Minimum Endurance

3 = 1000 cycles

Read Access Speed

70 = 70 ns, 90 = 90 ns

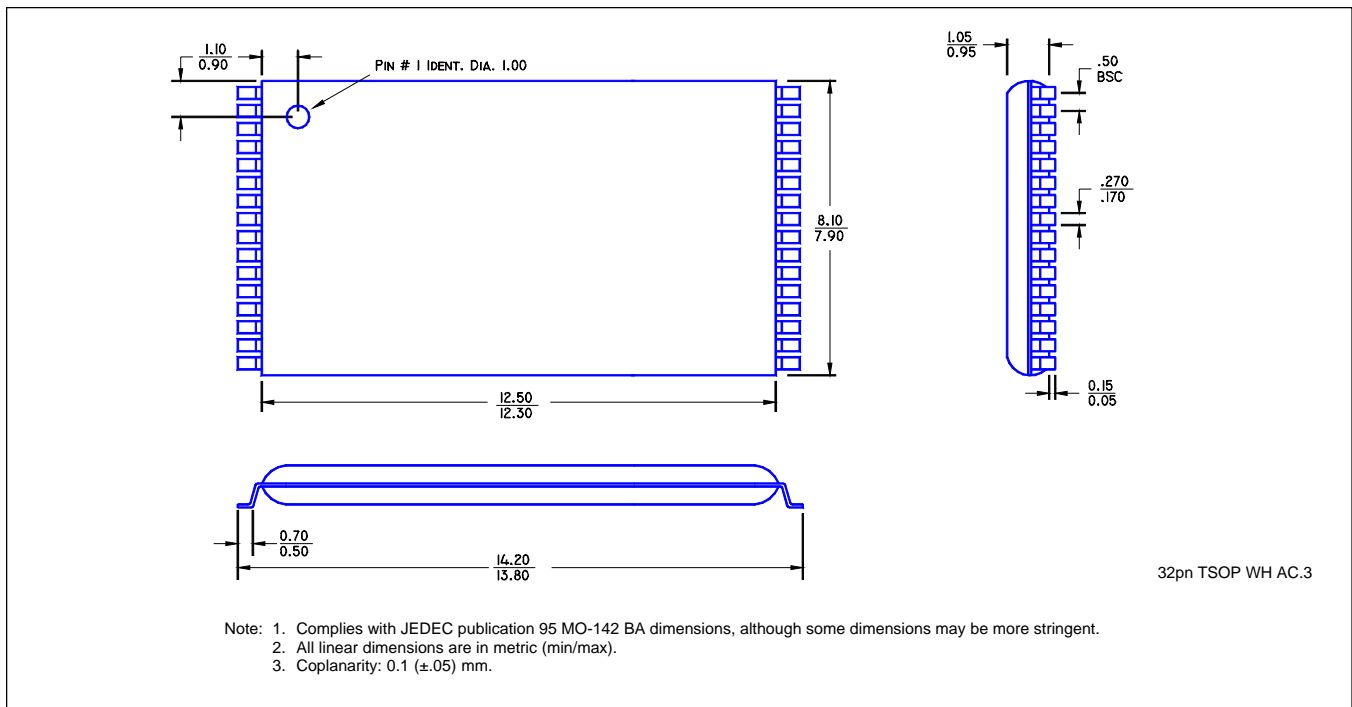
Valid combinations

SST27SF010- 70-3C-WH	SST27SF010- 70-3C-NH	SST27SF010- 70-3C-PH
SST27SF010- 90-3C-WH	SST27SF010- 90-3C-NH	SST27SF010- 90-3C-PH
SST27SF010- 70-3I-WH	SST27SF010- 70-3I-NH	
SST27SF010- 90-3I-WH	SST27SF010- 90-3I-NH	SST27SF010- 90-3C-U1

Example: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

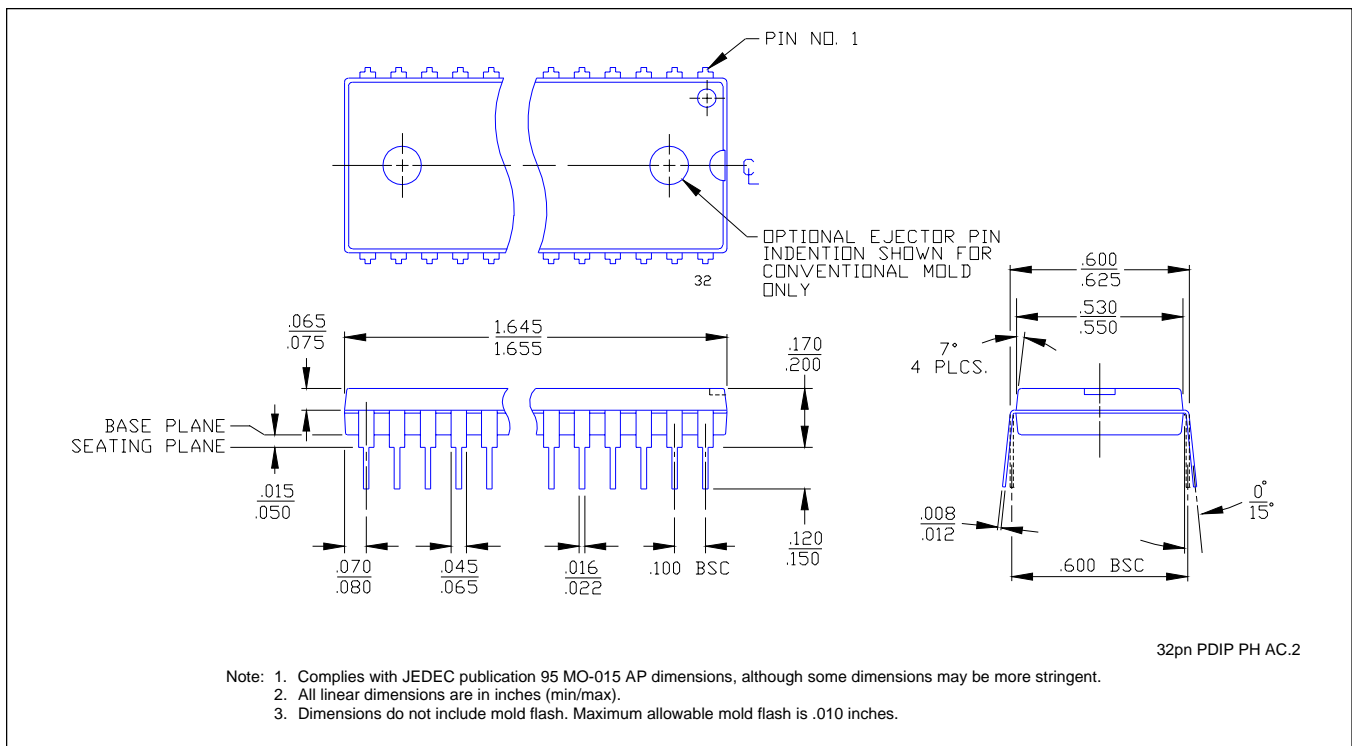


PACKAGING DIAGRAMS



32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP)

SST PACKAGE CODE: WH



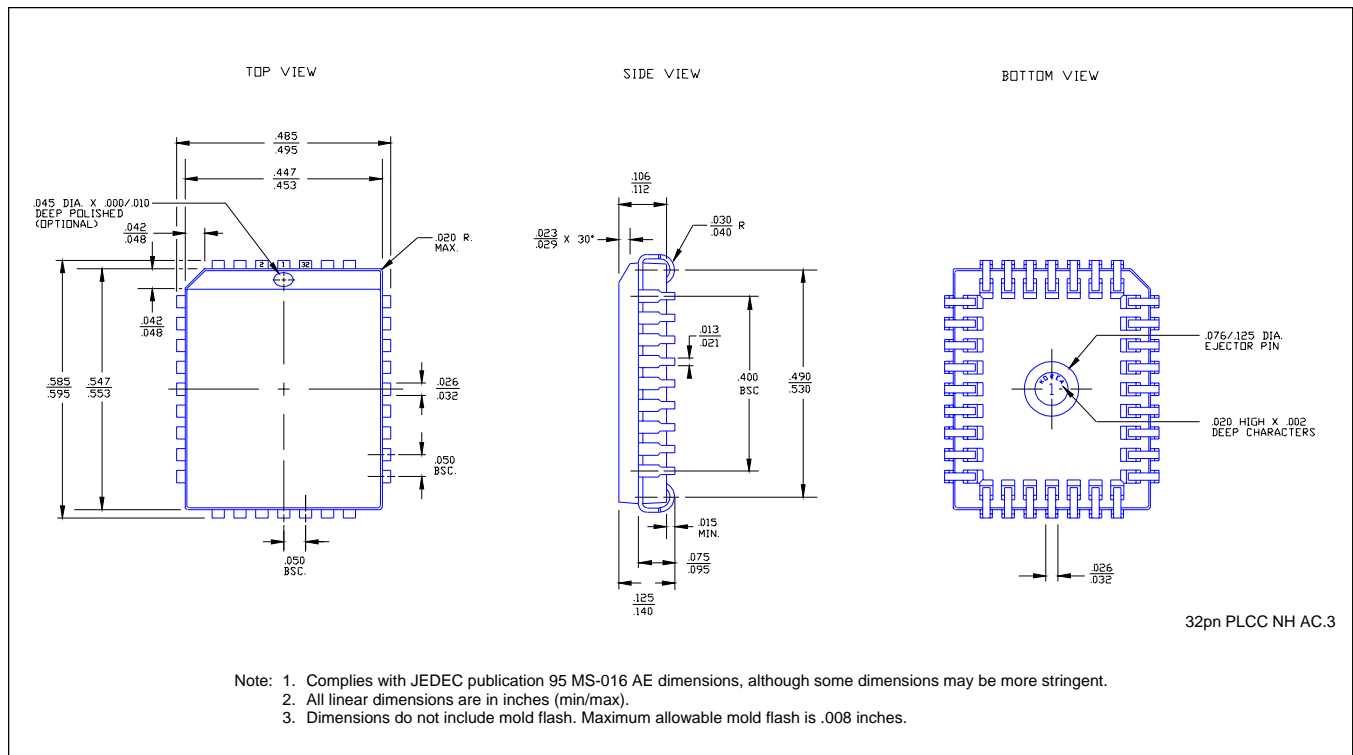
32-LEAD PLASTIC DUAL-IN-LINE PACKAGE (PDIP)

SST PACKAGE CODE: PH



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32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH