

INVERTER GRADE THYRISTORS

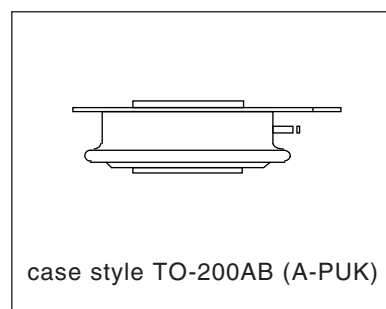
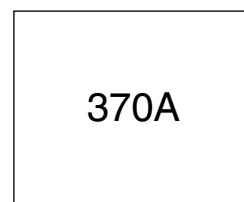
Hockey Puk Version

Features

- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance

Typical Applications

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters



Major Ratings and Characteristics

Parameters	ST203C..C	Units
$I_{T(AV)}$	370	A
@ T_{hs}	55	°C
$I_{T(RMS)}$	700	A
@ T_{hs}	25	°C
I_{TSM}	@ 50Hz 5260	A
	@ 60Hz 5510	A
I^2t	@ 50Hz 138	KA ² s
	@ 60Hz 126	KA ² s
V_{DRM}/V_{RRM}	1000 to 1200	V
t_q range	20 to 30	μs
T_J	- 40 to 125	°C

ST203C..C Series

Bulletin I25176 rev. B 04/00

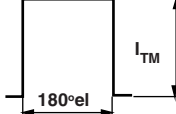
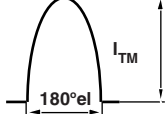
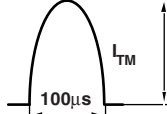
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ELECTRICAL SPECIFICATIONS

Voltage Ratings

Type number	Voltage Code	V_{DRM}/V_{RRM} , maximum repetitive peak voltage V	V_{RSM} , maximum non-repetitive peak voltage V	I_{DRM}/I_{RRM} max. @ $T_J = T_{J \text{ max.}}$ mA
ST203C..C	10	1000	1100	40
	12	1200	1300	

Current Carrying Capability

Frequency							Units
	I_{TM}	$180^\circ eI$	I_{TM}	$180^\circ eI$	I_{TM}	$100\mu s$	
50Hz	860	750	1340	1160	5620	5020	A
400Hz	840	706	1400	1220	2940	2590	
1000Hz	700	580	1350	1170	1750	1520	
2500Hz	430	340	980	830	910	780	
Recovery voltage Vr	50	50	50	50	50	50	V
Voltage before turn-on Vd	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50	50	-	-	-	-	A/ μs
Heatsink temperature	40	55	40	55	40	55	°C
Equivalent values for RC circuit	47 Ω / 0.22 μF		47 Ω / 0.22 μF		47 Ω / 0.22 μF		

On-state Conduction

Parameter	ST203C..C	Units	Conditions	
$I_{T(AV)}$ Max. average on-state current @ Heatsink temperature	370 (140)	A	180° conduction, half sine wave double side (single side) cooled	
	55 (85)	°C		
$I_{T(RMS)}$ Max. RMS on-state current	700	A	DC @ 25°C heatsink temperature double side cooled	
I_{TSM} Max. peak, one half cycle, non-repetitive surge current	5260		t = 10ms	No voltage reappplied
	5510		t = 8.3ms	reappplied
	4420		t = 10ms	100% V_{RRM}
	4630		t = 8.3ms	reappplied
I^2t Maximum I^2t for fusing	138		KA ² s	t = 10ms
	126			t = 8.3ms
	98			t = 10ms
	89	t = 8.3ms		
$I^2\sqrt{t}$ Maximum $I^2\sqrt{t}$ for fusing	1380	KA ² \sqrt{s}	t = 0.1 to 10ms, no voltage reappplied	

On-state Conduction

Parameter	ST203C..C	Units	Conditions
V_{TM} Max. peak on-state voltage	1.72	V	$I_{TM} = 600A$, $T_J = T_J \text{ max}$, $t_p = 10\text{ms}$ sine wave pulse
$V_{T(TO)1}$ Low level value of threshold voltage	1.17		$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
$V_{T(TO)2}$ High level value of threshold voltage	1.22		$(I > \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
r_{t1} Low level value of forward slope resistance	0.92	m Ω	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
r_{t2} High level value of forward slope resistance	0.83		$(I > \pi \times I_{T(AV)})$, $T_J = T_J \text{ max}$.
I_H Maximum holding current	600	mA	$T_J = 25^\circ\text{C}$, $I_T > 30A$
I_L Typical latching current	1000		$T_J = 25^\circ\text{C}$, $V_A = 12V$, $R_a = 6\Omega$, $I_G = 1A$

Switching

Parameter	ST203C..C	Units	Conditions
di/dt Max. non-repetitive rate of rise of turned-on current	1000	A/ μs	$T_J = T_J \text{ max}$., $V_{DRM} = \text{rated } V_{DRM}$ $I_{TM} = 2 \times \text{di/dt}$
t_d Typical delay time	0.8	μs	$T_J = 25^\circ\text{C}$, $V_{DM} = \text{rated } V_{DRM}$, $I_{TM} = 50A$ DC, $t_p = 1\mu\text{s}$ Resistive load, Gate pulse: 10V, 5 Ω source
t_q Max. turn-off time	Min 20 Max 30		$T_J = T_J \text{ max}$, $I_{TM} = 300A$, commutating di/dt = 20A/ μs $V_R = 50V$, $t_p = 500\mu\text{s}$, dv/dt: see table in device code

Blocking

Parameter	ST203C..C	Units	Conditions
dv/dt Maximum critical rate of rise of off-state voltage	500	V/ μs	$T_J = T_J \text{ max}$. linear to 80% V_{DRM} , higher value available on request
I_{RRM} Max. peak reverse and off-state leakage current I_{DRM}	40	mA	$T_J = T_J \text{ max}$, rated V_{DRM}/V_{RRM} applied

Triggering

Parameter	ST203C..C	Units	Conditions
P_{GM} Maximum peak gate power	60	W	$T_J = T_J \text{ max}$, $f = 50\text{Hz}$, $d\% = 50$
$P_{G(AV)}$ Maximum average gate power	10		
I_{GM} Max. peak positive gate current	10	A	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$+V_{GM}$ Maximum peak positive gate voltage	20	V	$T_J = T_J \text{ max}$, $t_p \leq 5\text{ms}$
$-V_{GM}$ Maximum peak negative gate voltage	5		
I_{GT} Max. DC gate current required to trigger	200	mA	$T_J = 25^\circ\text{C}$, $V_A = 12V$, $R_a = 6\Omega$
V_{GT} Max. DC gate voltage required to trigger	3	V	
I_{GD} Max. DC gate current not to trigger	20	mA	$T_J = T_J \text{ max}$., rated V_{DRM} applied
V_{GD} Max. DC gate voltage not to trigger	0.25	V	

ST203C..C Series

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Thermal and Mechanical Specification

Parameter	ST203C..C	Units	Conditions
T_J Max. operating temperature range	-40 to 125	°C	
T_{stg} Max. storage temperature range	-40 to 150		
R_{thJ-hs} Max. thermal resistance, junction to heatsink	0.17	K/W	DC operation single side cooled
	0.08		DC operation double side cooled
R_{thC-hs} Max. thermal resistance, case to heatsink	0.033	K/W	DC operation single side cooled
	0.017		DC operation double side cooled
F Mounting force, $\pm 10\%$	4900	N	
	(500)	(Kg)	
wt Approximate weight	50	g	
Case style	TO - 200AB (A-PUK)		See Outline Table

ΔR_{thJ-hs} Conduction

(The following table shows the increment of thermal resistance R_{thJ-hs} when devices operate at different conduction angles than DC)

Conduction angle	Sinusoidal conduction		Rectangular conduction		Units	Conditions
	Single Side	Double Side	Single Side	Double Side		
180°	0.015	0.017	0.011	0.011	K/W	$T_J = T_J \text{ max.}$
120°	0.018	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

Ordering Information Table

Device Code

ST	20	3	C	12	C	H	H	1	
①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩

- 1** - Thyristor
- 2** - Essential part number
- 3** - 3 = Fast turn off
- 4** - C = Ceramic Puk
- 5** - Voltage code: Code x 100 = V_{RRM} (See Voltage Rating Table)
- 6** - C = Puk Case TO-200AB (A-PUK)
- 7** - Reapplied dv/dt code (for t_q test condition)
- 8** - t_q code
- 9** - 0 = Eyelet term. (Gate and Aux. Cathode Unsoldered Leads)
 - 1 = Fast-on term. (Gate and Aux. Cathode Unsoldered Leads)
 - 2 = Eyelet term. (Gate and Aux. Cathode Soldered Leads)
 - 3 = Fast-on term. (Gate and Aux. Cathode Soldered Leads)
- 10** - Critical dv/dt:
 - None = 500V/ μ sec (Standard value)
 - L = 1000V/ μ sec (Special selection)

dv/dt - t_q combinations available					
dv/dt (V/ μ s)	20	50	100	200	400
t_q (μ s)	20	CK	DK	EK	--
	25	CJ	DJ	EJ	FJ*
	30	CH	DH	EH	FH

*Standard part number.
All other types available only on request.

Outline Table

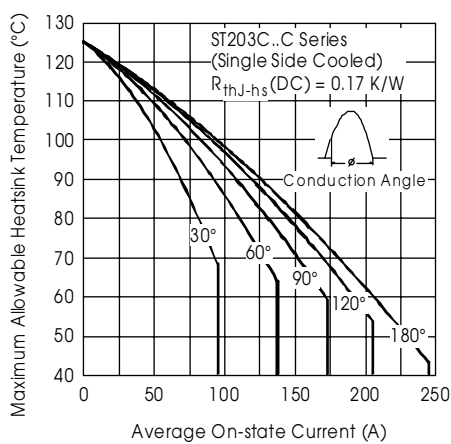
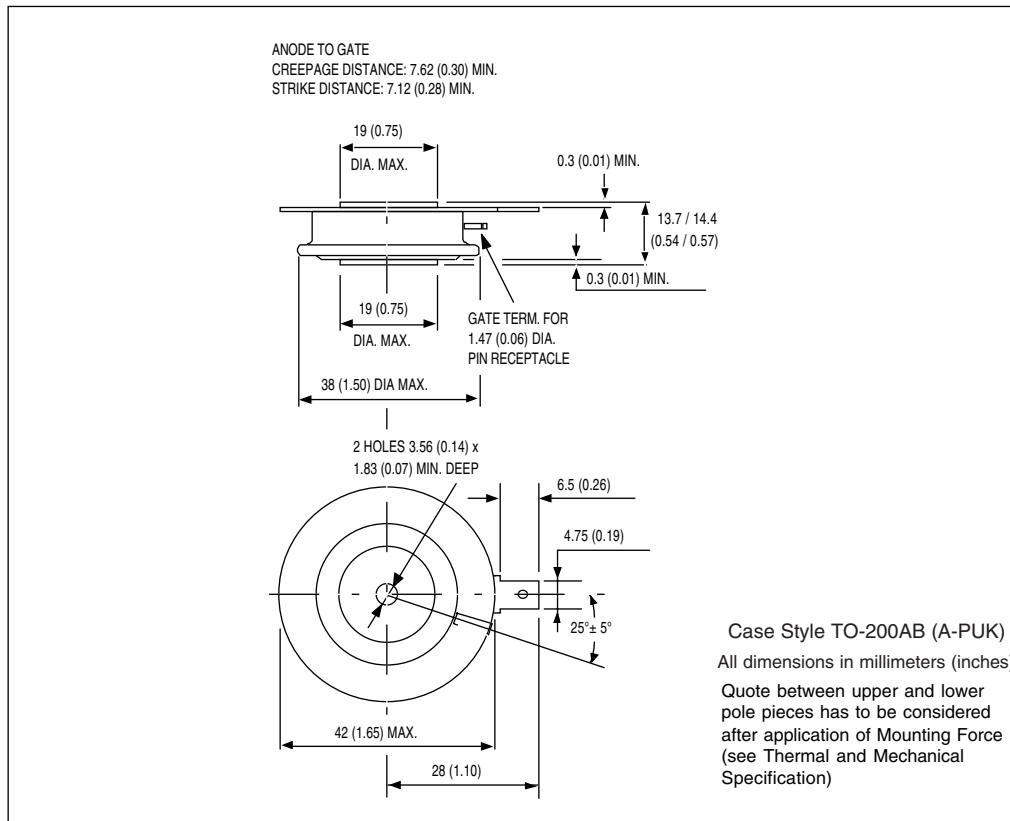


Fig. 1 - Current Ratings Characteristics

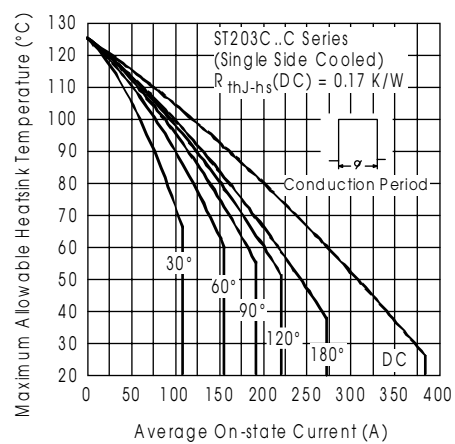


Fig. 2 - Current Ratings Characteristics

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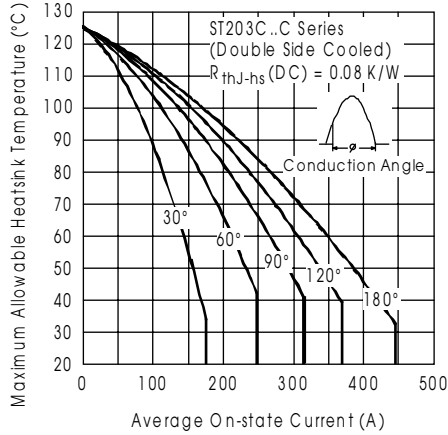


Fig. 3 - Current Ratings Characteristics

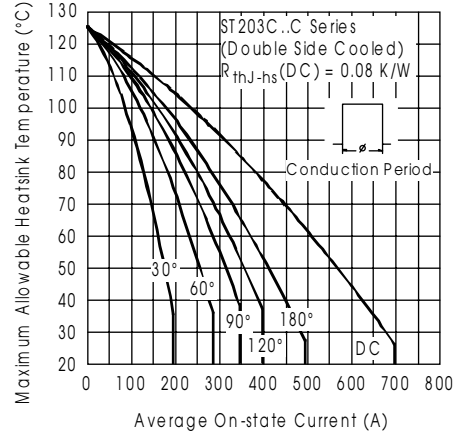


Fig. 4 - Current Ratings Characteristics

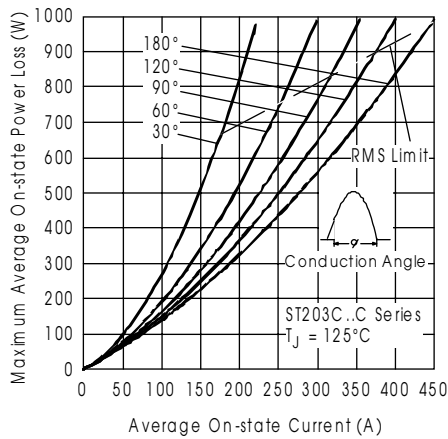


Fig. 5 - On-state Power Loss Characteristics

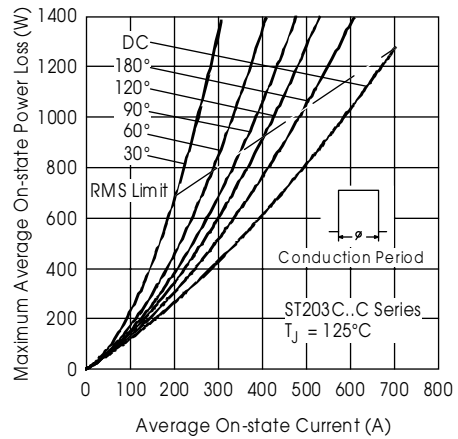


Fig. 6 - On-state Power Loss Characteristics

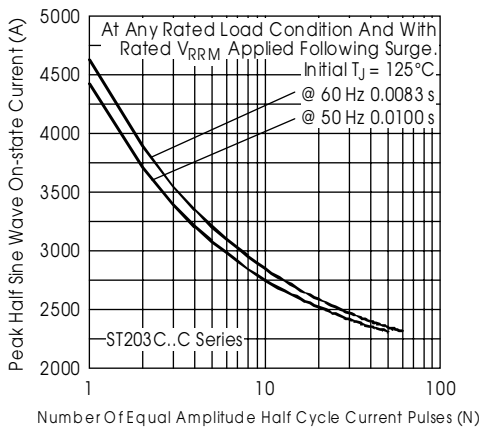


Fig. 7 - Maximum Non-repetitive Surge Current Single and Double Side Cooled

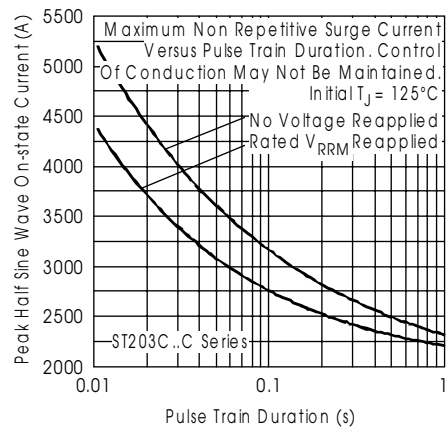


Fig. 8 - Maximum Non-repetitive Surge Current Single and Double Side Cooled

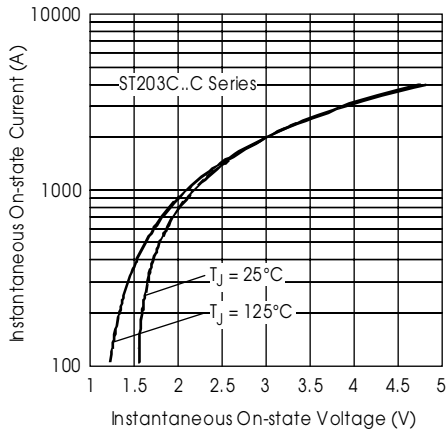


Fig. 9 - On-state Voltage Drop Characteristics

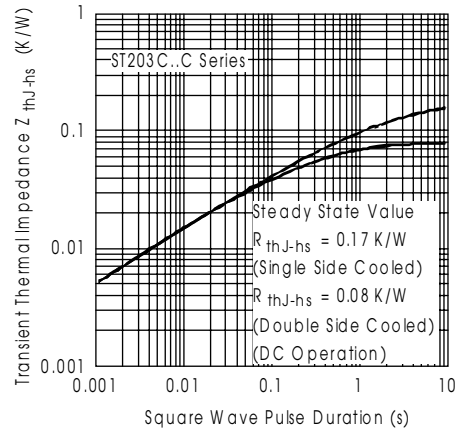


Fig. 10 - Thermal Impedance Z_{thj-hs} Characteristics

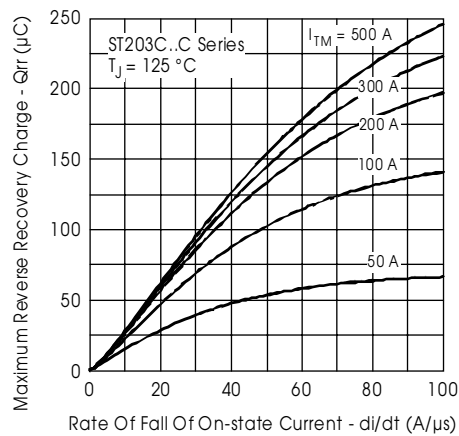


Fig. 11 - Reverse Recovered Charge Characteristics

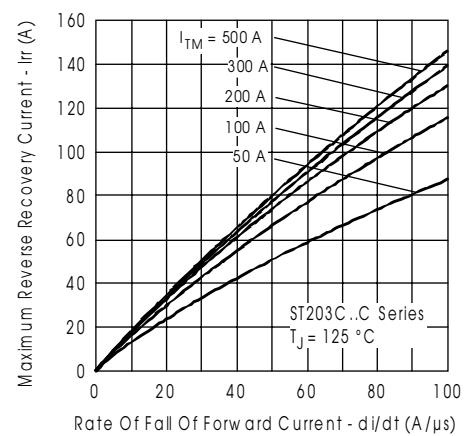


Fig. 12 - Reverse Recovery Current Characteristics

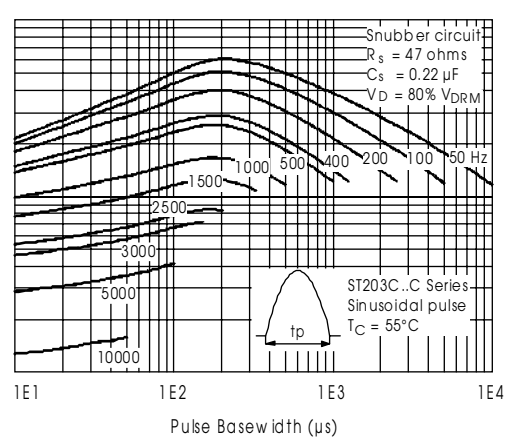
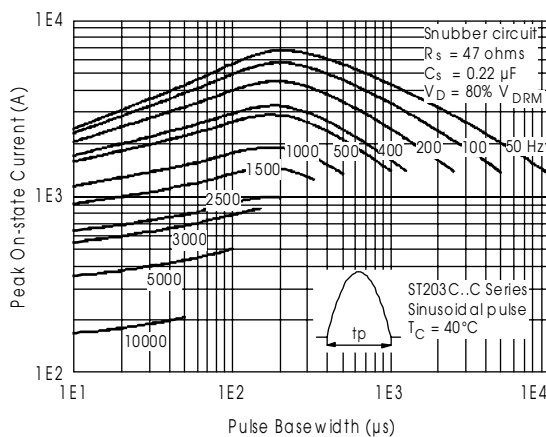


Fig. 13 - Frequency Characteristics

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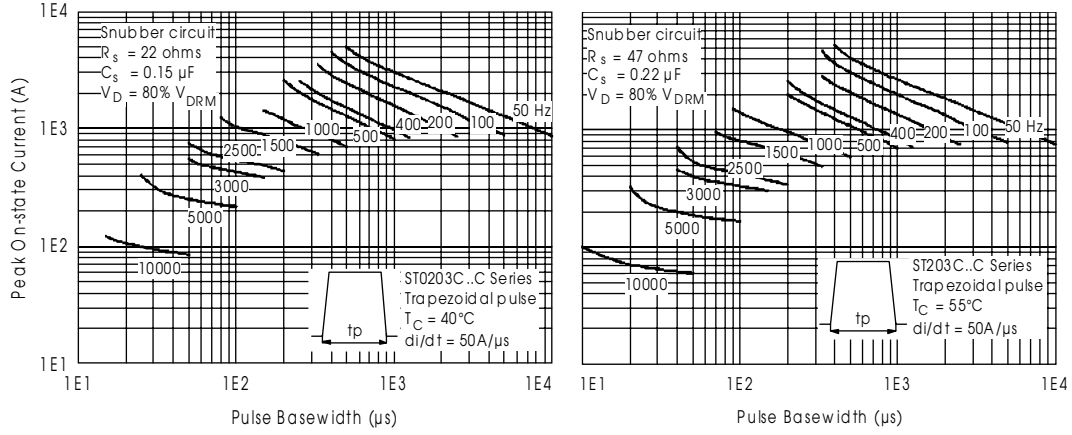


Fig. 14 - Frequency Characteristics

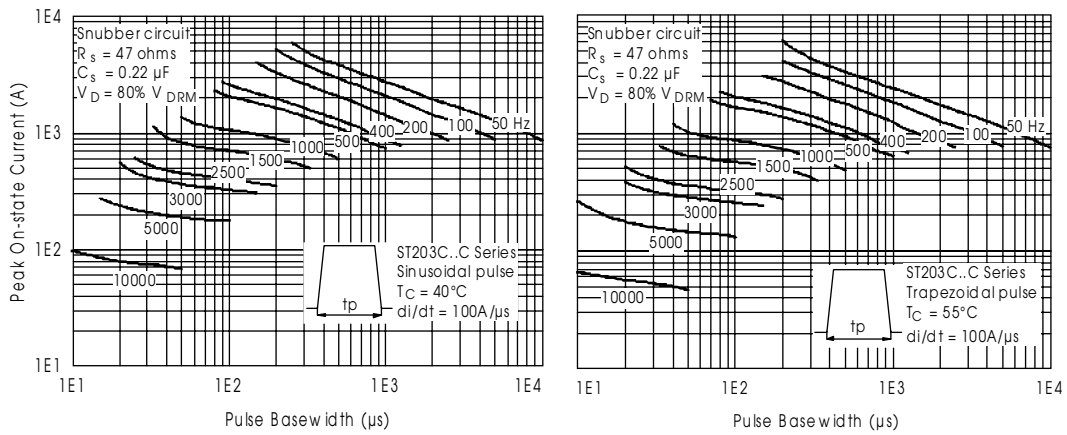


Fig. 15 - Frequency Characteristics

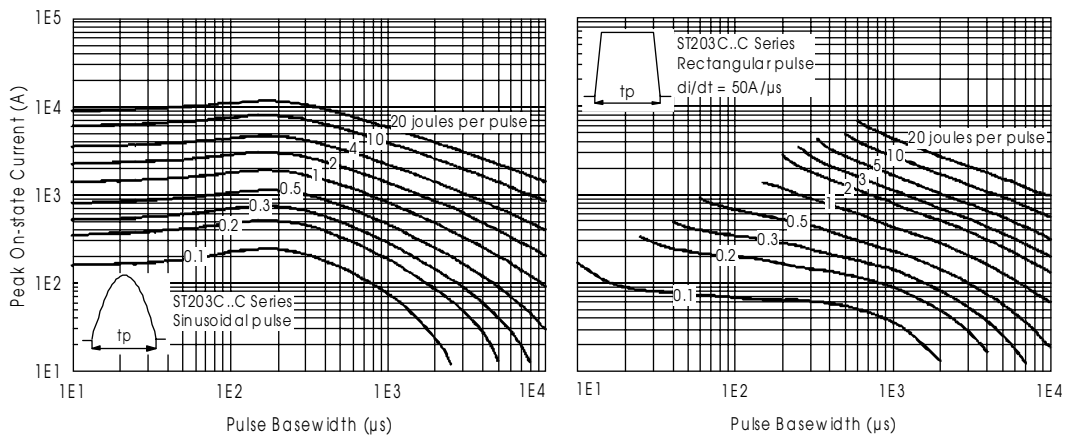


Fig. 16 - Maximum On-state Energy Power Loss Characteristics

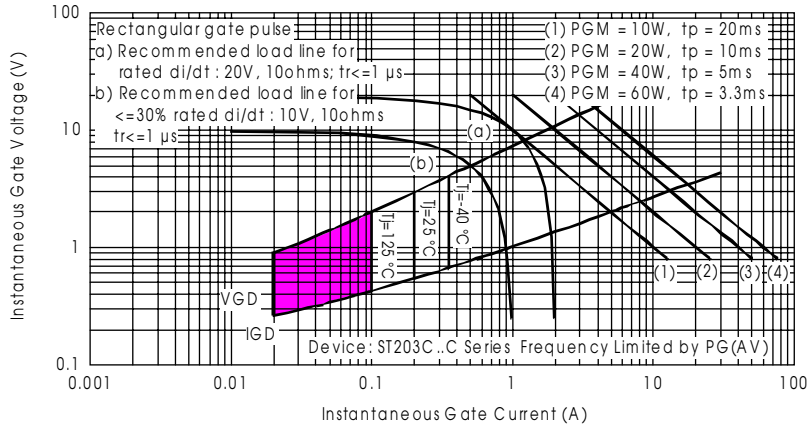


Fig. 17 - Gate Characteristics