PM5313/PM5363

SPECTRA-622 WITH-TUPP-PLUS-622

REFERENCE DESIGN

PRELIMINARY

ISSUE 2: DECEMBER 1999

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	Aug. 1999	Document created.
2	Dec. 1999	Document revised to reflect changes made to the schematic for revision of reference design. A section was added containing VHDL code for the FPGA as well as a more detailed description of the FPGA. The following changes were made to the schematic: -Addition of serial EPROM for programming of the FPGA. -Modified reference oscillator circuitry to accommodate PECL reference Oscillator, as well as HCMOS/TTL Oscillator. -Modified reset circuitry. -Corrected several minor schematic errors

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1 DEFINITIONS

LOS	Loss of signal. When a SONET receiver detects an all-zeros pattern for 10 microseconds or longer, this constitutes a LOS failure. It indicates that the upstream transmitter has failed. This condition is cleared when two consecutive valid frames are received.
LOF	Loss of frame. The absence of valid framing pattern for 3 milliseconds leads to a LOF failure condition. This is cleared when two consecutive valid A1/A2 framing patterns are received.
AIS	Alarm indication signal. This condition can occur in response to one of the conditions above. The SONET signal format provides AISs for the line (AIS-L), STS Path (AIS-P), and VT Path (AIS-V) layers.
RDI	Line remote defect indication. A signal returned to the transmitting Line Terminating Equipment (LTE) upon receipt of an AIS code or detection of an incoming line defect at the receiving LTE. The SONET signal format provides RDIs for the line (RDI-L), STS Path (RDI-P), and VT Path.
SD	Signal Degrade. A “soft failure” condition resulting from the Line BER exceeding a pre-selected threshold.
BER	Bit Error Rate
SF	Signal Fail. A “hard failure” condition detected on the incoming OC-N signal.

2 FEATURES

- 33 MHz CompactPCI (cPCI) interface.
- Implements STS-12 Add-Drop MUX and STS-12 terminal MUX using the PM5313 SPECTRA-622 OC-12 SONET/SDH payload extractor aligner and the TUPP-PLUS-622 SONET/SDH tributary unit payload processor.
- OC-12 line side interface can accommodate both 5 Volt and 3.3 Volt Optical transceivers.
- 3.3 Volt CMOS telecom bus interface to the TUPP-PLUS-622 system drop bus and to the SPECTRA-622 system add bus.
    - Telecom bus can be configured to operate in either the single STS-12 (STM-4) at 77.76 MHz or as four STS-3s (STM-1) at 19.44 MHz.
- 3.3 Volt CMOS DS3 interface to the SPECTRA-622 drop and add bus.
- Custom FPGA to provides data throughput and APS functions for the STS-12 add-drop MUX application.
    - Can be programmed via the cPCI bus or through XCHECKER port.
    - R/W registers for configuration of Add-Drop MUX and APS control and monitor.
    - Interfaces to SPECTRA-622 receive and transmit overhead and alarm signals for custom applications.
- Low cost 77.76 MHz reference uses a standard fundamental mode, inexpensive crystal or standard HCMOS/TTL oscillator.
    - 77.76 MHz reference clock can be supplied by onboard
    - oscillator or by external source.
- PLL clock drivers for the 19.44 MHz and 77.76 MHz system clocks.

3 APPLICATIONS

- Tributary pointer processing and performance monitoring.
- SONET/SDH Add Drop Multiplexers - STS-12 (STM-4/AU-3), STS-12 (STM-4/AU-4) or STS12c (STM-4-4c)
- SONET/SDH Terminal Multiplexers. - STS-12 (STM-4/AU-3), STS-12 (STM-4/AU-4) or STS12c (STM-4-4c)

4 REFERENCES

1. PCI Industrial Computers Manufacturers Group (PICMG), “CompactPCI Specification 2.0 R 2.1”, Wakefield MA, September 1997.

2. PMC-Sierra Inc., PMC-981162, “SONET/SDH Payload Extractor/Aligner for `622 Mbits/s”, November 1998, Issue 1.

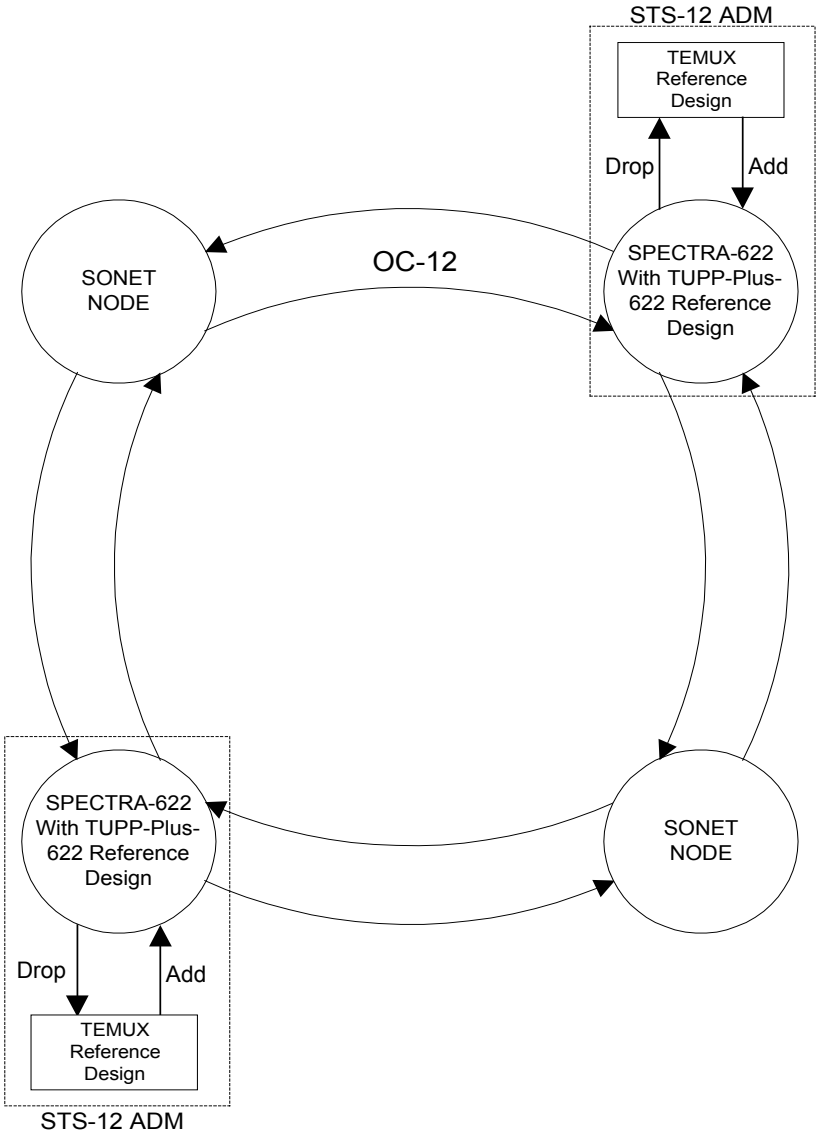
3. PMC-Sierra Inc. , PMC-981421, “SONET/SDH Tributary Unit Payload Processor For 622 Mbit/s Interfaces”, December 1998, Issue 1.

4. American National Standard for Telecommunications (ANSI) Synchronous Optical Network (SONET) Basic Description including Multiplex Structure, Rates, and formats, “T1.105-1995”, New York, NY, October 27, 1995

5 APPLICATION EXAMPLES

The SPECTRA-622 WITH TUPP-PLUS-622 reference design can be used in conjunction with the TEMUX reference design to implement an STS-12 Add Drop MUX in a Unidirectional Path Switched Ring (UPSR) as shown in Fig. 1 below or as an STS-12 Terminal MUX in a point to point network.

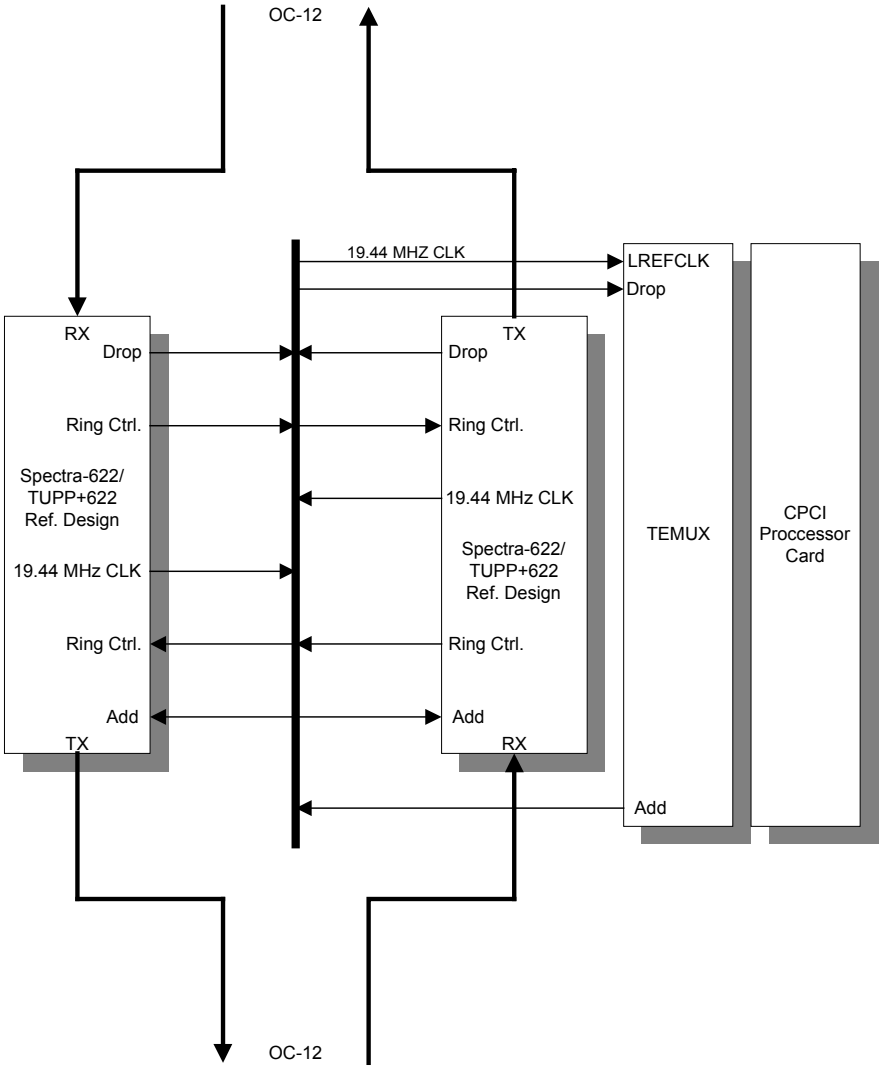
Figure 1 STS-12 ADM in a UPSR SONET Ring Network



When used as an add Drop MUX the SPECTRA-622 would be configured to operate in the quad Add/Drop bus interface STS-3 (STM-1) mode and TUPP-PLUS-622 would be configured in the STS-3 (STM-1) mode with the telecom bus clocked at 19.44 MHz. The FPGA would be configured to loop-back the throughput STS-1s from the drop bus to the add bus and perform APS related functions.

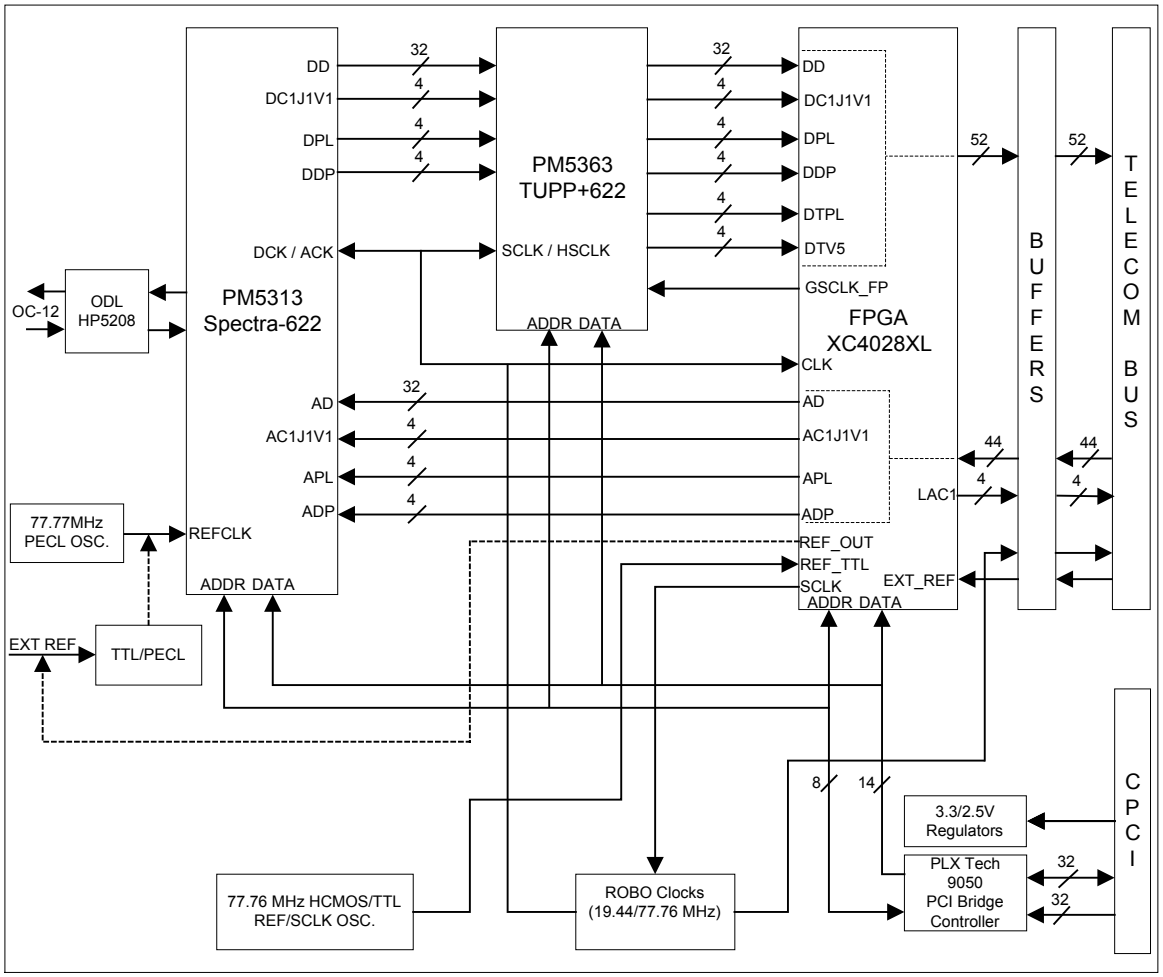
When configured to implement a Terminal MUX, the SPECTRA-622 WITH TUPP-PLUS-622 reference design would be configured as an ADM with all traffic dropped.

Figure 2 STS-12 Add Drop MUX



6 BLOCK DIAGRAM

Figure 3 Reference Design Block Diagram.



7 FUNCTIONAL DESCRIPTION

The PM5313 SPECTRA-622 takes the OC-12 SONET/SDH serial bit stream from the HP5208 optical transceiver and recovers clock, data and processes section, line, and path overhead. The telecom drop bus from the SPECTRA-622 interfaces directly to the input side of the PM5363 TUPP-PLUS-622. The TUPP-PLUS-622 will perform tributary processing and frame alignment on the SONET/SDH STS-12 byte serial data stream. The TUPP-PLUS-622 will output a frame aligned single STS-12 (STM-4) clocked at 77.76 MHz or a quad STS-3 (STM-1) clocked at 19.44 MHz and this will be clocked into the FPGA.

When the SPECTRA-622 WITH TUPP reference design is configured to implement an add drop MUX, both TUPP-PLUS-622 and the SPECTRA-622 will be configured to operate in the Quad STS-3 (STM-1) mode. The payload will be clocked into the FPGA from the TUPP-PLUS-622 drop bus output on the rising edge of the 19.44 MHz clock . The entire payload will be clocked out of the FPGA onto the telecom interface (J4, J5) drop side. Traffic to be inserted into the payload will be clocked into the FPGA from the telecom interface add side on the rising edge of 19.44 MHz clock and inserted into the appropriate STS-12 time slot along with the throughput data. The aggregate data will be clocked out of the FPGA onto the SPECTRA-622 add bus on the rising edge of the 19.44 MHz clock.

All of the drop bus signals including the system clocks can be tristated to accommodate APS switching. The management software should initiate a switch if the SPECTRA-622 detects one of the following conditions:

- Signal Degrade: soft failure condition caused by line BER exceeding a SD threshold.
- Signal Fail: hard failure caused by LOS, LOF, line AIS, or by Line BER exceeding a SF threshold.

Once one of the above conditions has been detected by the SPECTRA-622, path AIS will be sent to the upstream node, (SPECTRA-622 WITH TUPP-PLUS-622 reference design) and a switch will be initiated.

When the SPECTRA-622 WITH TUPP-PLUS-622 reference design is configured to operate in the single STS-12 (STM-4) mode. The TUPP telecom drop bus will be clocked directly through the FPGA on the rising edge of a 77.76 MHz system clock, onto the telecom bus interface connector (J4 & J5). Add bus signals will be clocked in from the same interface connector (J4 & J5), directly through the FPGA, onto the SPECTRA-622 add bus, on the rising edge of the 77.76 MHz system clock.

7.1 PM5313 SPECTRA-622

The PM5313 SPECTRA-622 is a PMC Sierra standard product that implements an STS-12 (STM-4/AU3 or STM-4/AU4) or STS-12c (STM-4-4c) SONET/SDH payload extractor aligner.

The SPECTRA-622 receives SONET/SDH streams using a 622 Mbit/s bit serial interface, recovers clock, data and processes section, line and path overhead. The SPECTRA-622 performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section line, and path bit interleaved parity (B1, B2, and B3), accumulating error counts at each level for performance monitoring purposes. The SPECTRA-622 interprets the received payload pointers (H1, H2) and extracts the SPE. The SPE will be available on the telecom drop bus as either a single STS-12 (STM-4) at 77.76 MHz or four STS-3s (STM-1) at 19.44 MHz.

The SPECTRA-622 transmits SONET/SDH streams using a bit serial interface. The SPECTRA-622 synthesizes the transmit clock from a 77.76 MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line and path bit interleaved parity codes (B1,B2,B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The SPECTRA-622 also generates the payload pointers (H1, H2) and inserts the SPE from the telecom add bus. The telecom drop bus can be configured as a single STS-12 (STM-4) at 77.76 MHz or four STS-3s (STM-1) at 19.44 MHz.

The SPECTRA-622 is implemented in low power, +3.3 Volt, CMOS technology. It has TTL compatible inputs and TTL/CMOS compatible outputs. High speed inputs and outputs support 3.3 Volt and 5.0 Volt PECL. A standard 5 signal JTAG test port for boundary scan board test purposes is provided and a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring. Both the microprocessor and the JTAG interface are 5 Volt tolerant. The SPECTRA-622 is available in a 520 pin Super BGA package and is guaranteed to operate over the industrial temperature range (-40°C to +85°C).

7.2 PM5363 TUPP-PLUS-622

The PM5363 TUPP-PLUS-622 is a SONET/SDH Tributary Unit Payload Unit Processor for 622 Mbit/s interfaces. The payload processor aligns and monitors the performance of all SONET virtual tributaries (VTs) or SDH tributary units (TUS). The TUPP-PLUS-622 provides many SONET/SDH maintenance and performance functions.

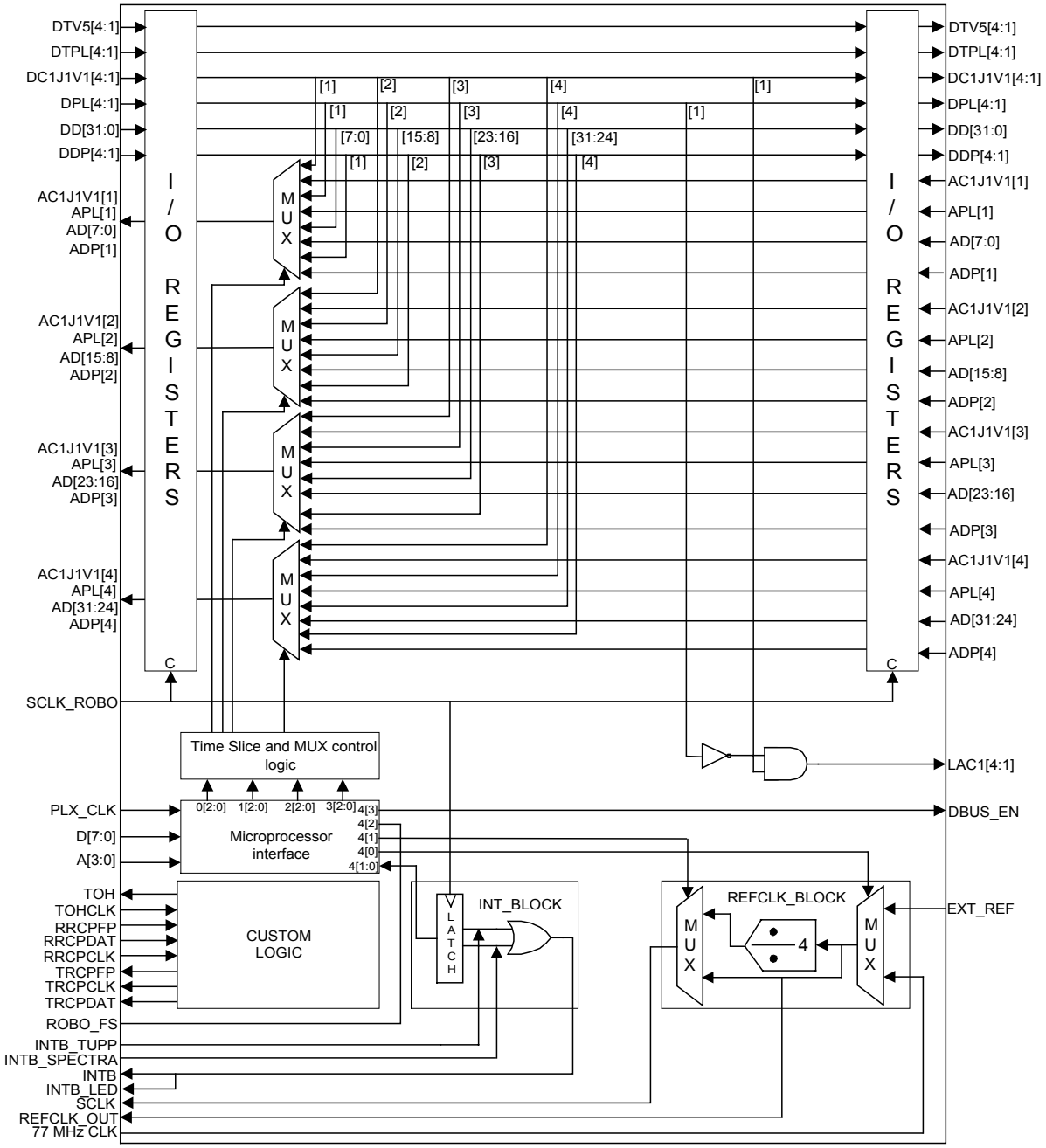
The TUPP-PLUS-622 telecom bus can be configured as a single STS-12 (STM-4) at 77.76 MHz or four STS-3^s (STM-1) at 19.44 MHz.

The TUPP-PLUS-622 is implemented in low power, +2.5 Volt core and +3.3 Volt I/O, CMOS technology. It has TTL compatible inputs and TTL/CMOS compatible outputs. High speed inputs and outputs support 3.3 Volt and 5.0 Volt PECL. A standard 5 signal JTAG test port for boundary scan board test purposes is provided and a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring. Both the microprocessor and the JTAG interface are 5 Volt tolerant. The TUPP-622 is available in a 304 pin Super BGA package and is guaranteed to operate over the industrial temperature range (-40°C to +85°C).

7.3 FPGA

7.3.1 STS-12 Add Drop MUX FPGA

Figure 4 STS-12 Add Drop MUX FPGA



The main function of the STS-12 Add Drop MUX FPGA is to provide data throughput on a STS-1 basis and insert data on the add bus on a STS-1 basis. In this application the telecom bus will be operating in the Quad STS-3 mode. As shown in Fig. 4 above, the FPGA will consist of the following blocks: 22 bit 2:1 MUXs, microprocessor interface, time slice and MUX control logic, reference clock, and some additional, general purpose glue logic.

The I/O registers simply latch the data in on the rising edge of the 19.44 MHz clock and clock the data out on the rising edge of the clock.

The MUX block consist of four 22 bit 2:1 MUXs and I/O latches. The I/O latches are on the add bus inputs only, and delay the data by two clock cycles to provide proper alignment of the inserted STS-1s and the throughput data.

The microprocessor interface provides 8 bit R/W interface to the PLX-9050 local side and contains 5 R/W registers. Read access is a standard asychronous peripheral interface (Intel mode) and the write accesses are synchronous to the PLX 33 MHz clock.

The INT_block monitors the interrupt signals from both the SPECTRA-622 and the TUPP-Plus-622. If either of these two interrupts occur, INTB will be low until the respective interrupt is cleared. The state of both interrupts is latched in a register, on the rising edge of the system clock, and can be read by the microprocessor interface at 0x05 as described in table xx below. INTB_LED is a buffered version of INTB and can be used to drive an LED.

Register 0x05: INTERRUPT

Bit	Type	Function	Default
Bit 7	R/W	unused	0
Bit 6	R/W	unused	0
Bit 5	R/W	unused	0
Bit 4	R/W	unused	0
Bit 3	R/W	unused	0
Bit 2	R/W	unused	0
Bit 1	R/W	INT_TUPP	0
Bit 0	R/W	INT_SPECTRA	0

INT_SPECTRA:

INT_SPECTRA indicates the status of the SPECTR-622's interrupt pin and

INT_TUPP

INT_SPECTRA indicates the status of the SPECTR-622's interrupt pin and

The Refclk_block contains the logic necessary to select between the external, 77.76 MHz line side reference and the on board HCMOS/TTL 77.76 MHz reference. As well as generating 19.44 and 77.76 MHz system clocks from the 77.76 MHz reference. Rfclk_block registers are described in table 2 below.

Register 0x04: Rfclk

Bit	Type	Function	Default
Bit	**Type**	**Function**	**Default**
Bit 7	R/W	unused	0
Bit 6	R/W	unused	0
Bit 5	R/W	unused	0
Bit 4	R/W	unused	0
Bit 3	R/W	DBENAB	0
Bit 2	R/W	ROBOFS	0
Bit 1	R/W	SCLKSEL	0
Bit 0	R/W	REFINT	0

REFINT:

The REFINT bit selects the source for the 77.76 MHz reference clock. When REFINT is set high, the reference clock will be source from the on board oscillator. When REFINT is set low, the reference clock source will be external.

SCLKSEL:

The SCLKSEL bit selects the clock frequency of the SCLK output. When the SCLKSEL is set high, SCLK is nominally 19.44 MHz. When SCLK is set low, SCLK is nominally 77.76 MHz.

ROBOFS:

The ROBOFS bit selects the clock frequency of the ROBO clock devices. When the ROBOFS is set high, the ROBO clocks are nominally 77.76MHz. When ROBOFS is set low, the ROBO clocks are nominally 19.44 MHz.

DBENAB

The DBENAB bit enable the drop side buffers. When the DBENAB bit is set high the drop side buffers are disabled. When the DBENAB bit is low the drop side buffers will be enable.

The MUX control logic block generates the necessary control signals to enable the appropriate MUX or MUXs during the correct time slot time slot or time slots

to provide the data throughput of the of the STS-1s. Time slots can be selected by programming the bits of registers 0-3 as described in table 1 below.

Register 0x00: STS-3 #1 MUX timing control register

Bit	Type	Function	Default
7	R/W	unused	0
6	R/W	unused	0
5	R/W	unused	0
4	R/W	unused	0
3	R/W	unused	0
2	R/W	STS-3 #3	0
1	R/W	STS-3#2	0
0	R/W	STS-3#1	0

STS-3#1:

The STS-3#1 bit selects the STS-3 #1 STS-1 # 1 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #1 STS-1 #1 will inserted on the add bus, and when this bit is low the STS-3 #1 STS-1 #1 will be throughput data.

STS-3#2

The STS-3#2 bit selects the STS-3 #1 STS-1 # 2 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #1 STS-1 #2 will inserted on the add bus, and when this bit is low the STS-3 #1 STS-1 #2 will be throughput data.

STS-3#3

The STS-3#3 bit selects the STS-3 #1 STS-1 # 3 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #1 STS-1 #3 will inserted on the add bus, and when this bit is low the STS-3 #1 STS-1 #3 will be throughput data.

Register 0x01: STS-3 #2 MUX timing control register

Bit	Type	Function	Default
7	R/W	unused	0
6	R/W	unused	0
5	R/W	unused	0
4	R/W	unused	0
3	R/W	unused	0
2	R/W	STS-3 #3	0
1	R/W	STS-3#2	0
0	R/W	STS-3#1	0

STS-3#1:

The STS-3#1 bit selects the STS-3 #2 STS-1 # 1 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #2 STS-1 #1 will inserted on the add bus, and when this bit is low the STS-3 #2 STS-1 #1 will be throughput data.

STS-3#2

The STS-3#2 bit selects the STS-3 #2 STS-1 # 2 to be inserted on the add bus. When the STS-3#2 bit is set high the STS-3 #2 STS-1 #2 will inserted on the add bus, and when this bit is low the STS-3 #2 STS-1 #2 will be throughput data.

STS-3#3

The STS-3#3 bit selects the STS-3 #2 STS-1 # 3 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #2 STS-1 #3 will inserted on the add bus, and when this bit is low the STS-3 #2 STS-1 #3 will be throughput data.

Register 0x02: STS-3 #3 MUX timing control register

Bit	Type	Function	Default
7	R/W	unused	0
6	R/W	unused	0
5	R/W	unused	0
4	R/W	unused	0
3	R/W	unused	0
2	R/W	STS-3 #3	0
1	R/W	STS-3#2	0
0	R/W	STS-3#1	0

STS-3#1:

The STS-3#1 bit selects the STS-3 #3 STS-1 # 1 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #3 STS-1 #1 will inserted on the add bus, and when this bit is low the STS-3 #3 STS-1 #1 will be throughput data.

STS-3#2

The STS-3#2 bit selects the STS-3 #3 STS-1 # 2 to be inserted on the add bus. When the STS-3#2 bit is set high the STS-3 #3 STS-1 #2 will inserted on the add bus, and when this bit is low the STS-3 #3 STS-1 #2 will be throughput data.

STS-3#3

The STS-3#3 bit selects the STS-3 #3 STS-1 # 3 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #3 STS-1 #3 will inserted on the add bus, and when this bit is low the STS-3 #3 STS-1 #3 will be throughput data.

Register 0x03: STS-3 #4 MUX timing control register

Bit	Type	Function	Default
7	R/W	unused	0
6	R/W	unused	0
5	R/W	unused	0
4	R/W	unused	0
3	R/W	unused	0
2	R/W	STS-3 #3	0
1	R/W	STS-3#2	0
0	R/W	STS-3#1	0

STS-3#1:

The STS-3#1 bit selects the STS-3 #4 STS-1 # 1 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #4 STS-1 #1 will inserted on the add bus, and when this bit is low the STS-3 #4 STS-1 #1 will be throughput data.

STS-3#2

The STS-3#2 bit selects the STS-3 #4 STS-1 # 2 to be inserted on the add bus. When the STS-3#2 bit is set high the STS-3 #4 STS-1 #2 will inserted on the add bus, and when this bit is low the STS-3 #4 STS-1 #2 will be throughput data.

STS-3#3

The STS-3#3 bit selects the STS-3 #4 STS-1 # 3 to be inserted on the add bus. When the STS-3#1 bit is set high the STS-3 #4 STS-1 #3 will inserted on the add bus, and when this bit is low the STS-3 #3 STS-1 #3 will be throughput data.

REFINT:

The REFINT bit selects the source for the 77.76 MHz reference clock. When REFINT is set high, the reference clock will be source from the on board oscillator. When REFINT is set low, the reference clock source will be external.

SCLKSEL:

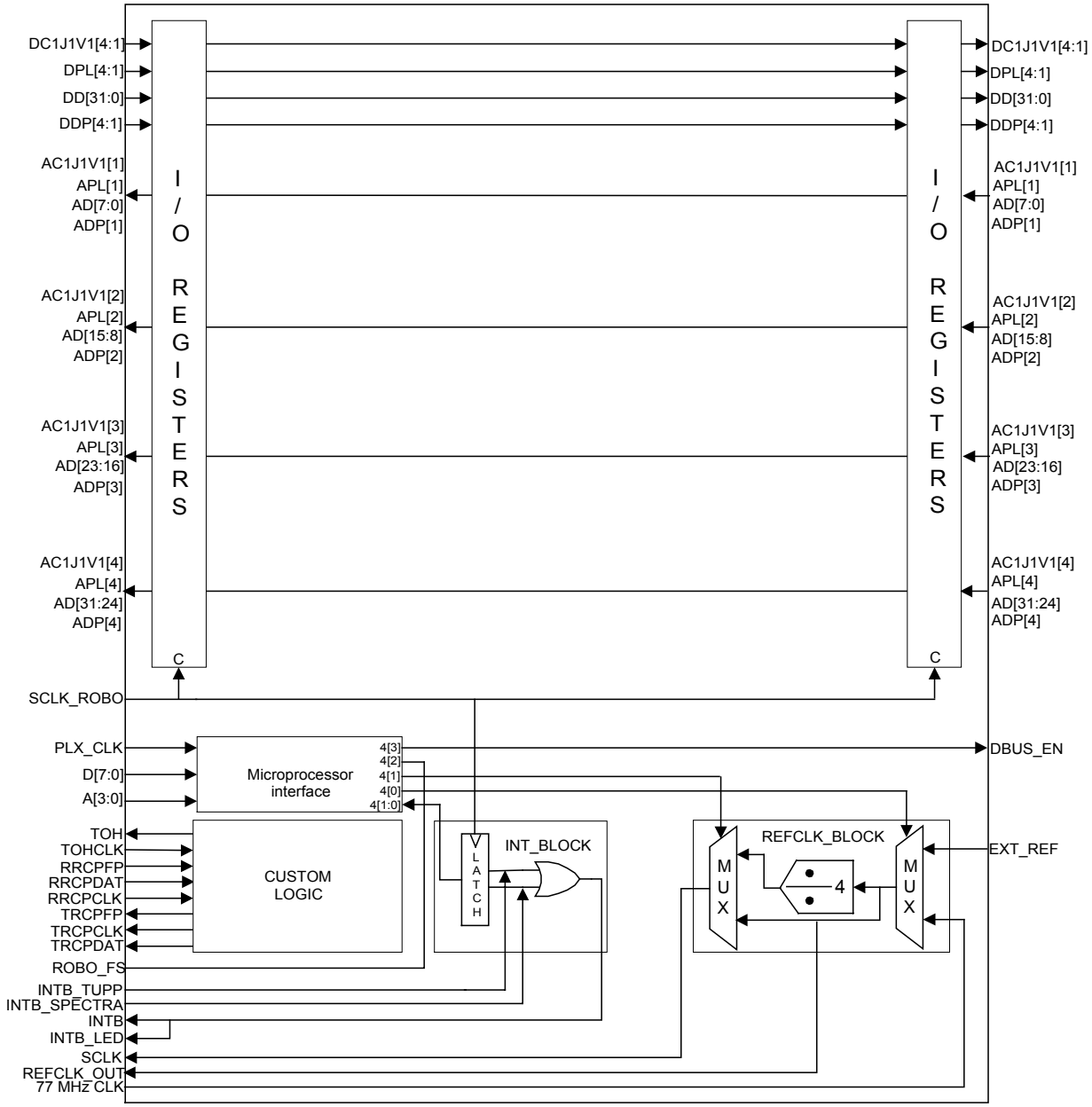
The SCLKSEL bit selects the clock frequency of the SCLK output. When the SCLKSEL is set high, SCLK is nominally 19.44 MHz. When SCLK is set low, SCLK is nominally 77.76 MHz.

ROBOFS:

The ROBOFS bit selects the clock frequency of the ROBO clock devices. When the ROBOFS is set high, the ROBO clocks are nominally 77.76MHz. When ROBOFS is set low, the ROBO clocks are nominally 19.44 MHz.

7.3.2 77.76 MHz Telecom Bus Interface FPGA

Figure 5 77.76 MHz Telecom Bus FPGA



The 77.76 MHz Telecom bus Interface FPGA provides a direct interface to all the standard telecom signals, for both the TUPP-Plus-622, and the SPECTRA-622. All signals are clocked in and out of the FPGA on the rising edge of the 77.76

MHz system clock. Although the FPGA clocks through all of the telecom bus signals, it has been designed to ensure operation at 77.76 MHz.

The 77.76 MHz Telecom Bus Interface FPGA also contains the REFCLK_BLOCK and the microprocessor interface block.

7.4 Buffers

The Telecom Bus will have both output and input buffering. The Telecom Drop Bus will have tristate buffering to accommodate APS. Buffers will be 3.3V and the inputs will be 5V tolerant.

7.5 PLX Technology 9050 PCI Bridge

The PCI 9050 provides a compact high performance PCI bus target (slave) interface for adapter boards. For more information on this device, please refer to the manufacturer's specification found on the PLX Technology web site. This device is programmed, via the external serial EEPROM, U13 at power up, for a 32 bit, local data bus. The PLX chip allows the board to map SPECTRA-622, TUPP-Plus-622, and the FPGA to the cPCI bus.

The signals from the J1 connector to the PLX chip are tightly controlled and must adhere to the cPCI physical specification for proper operation. Ten ohm series terminating resistors are used to minimize reflection in all the signals.

Any unused inputs such as the unused LAD (address/data) pins are pulled up with 4.7K resistors.

Also, all tri-state outputs, such as RDB, are pulled up via a 4.7K resistor to prevent the bus from chattering during power up.

The PLX does 32 bit, 4 byte accesses to/from the cPCI system Software selects the bottom byte only. Notice that the top three data bytes on the PLX are not connected to the bus and LA(2) is connected to A(0).

7.5.1 Serial EEPROM

The PLX chip, PCI9050, requires a configuration EEPROM during power up to configure itself. A serial device, U13, NM93CS46 contains the following code to configure the PLX for our system

Table 1 EEPROM Contents

EEPROM Offset (Hex)	Value (Hex)	PLX Register
0	9050	Device ID
2	10B5	Vendor ID
4	0680	Class Code
6	0000	ClassCode
8	7324	Subsystem ID
A	11F8	Subsystem Vendor ID
C	FFFF	Max Latency and Min Grant (not loadable)
E	00FF	Interrupt Pin
10	0FFF	MSW of Address Space 0 Range
12	0000	LSW of Address Space 0 Range
14	0FFF	MSW of Address Space 1 Range
16	0000	LSW of Address Space 1 Range
18	0FFF	MSW of Address Space 2 Range
1A	0000	LSW of Address Space 2 Range
1C	0000	MSW of Address Space 3 Range
1E	0000	LSW of Address Space 3 Range
20	0FFF	MSW of Expansion Rom Range
22	0000	LSW of Expansion Rom Range
24	0000	MSW of Address Space 0 Remap
26	0001	LSW of Address Space 0 Remap
28	0001	MSW of Address Space 1 Remap
2A	0001	LSW of Address Space 1 Remap
2C	0002	MSW of Address Space 2 Remap
2E	0001	LSW of Address Space 2 Remap
30	0000	MSW of Address Space 3 Remap
32	0000	LSW of Address Space 3 Remap
34	0000	MSW of Expansion Rom Remap

EEPROM Offset (Hex)	Value (Hex)	PLX Register
36	0000	LSW of Expansion Rom Remap
38	1681	MSW of Space 0 Bus Descriptor
3A	A1A0	LSW of Space 0 Bus Descriptor
3C	1681	MSW of Space 1 Bus Descriptor
3E	A1A0	LSW of Space 1 Bus Descriptor
40	1681	MSW of Space 2 Bus Descriptor
42	A1A0	LSW of Space 2 Bus Descriptor
44	0000	MSW of Space 3 Bus Descriptor
46	0000	LSW of Space 3 Bus Descriptor
48	0000	MSW of Expansion Rom Bus Descriptor
4A	0000	LSW of Expansion Rom Bus Descriptor
4C	0000	MSW of CS0 Register
4E	8001	LSW of CS0 Register
50	0001	MSW of CS1 Register
52	8001	LSW of CS1 Register
54	0002	MSW of CS2 Register
56	8001	LSW of CS2 Register
58	0000	MSW of CS3 Register
5A	0000	LSW of CS3 Register
5C	0000	MSW of Interrupt Control/Status
5E	0000	LSW of Interrupt Control/Status
60	0002	MSW of EEPROM and Misc. Control
62	44C0	LSW of EEPROM and Misc. Control
64 – 7F	FFFF	Unused

7.6 Reference clocks

The SPECTRA-622 WITH TUPP-PLUS-622 reference design requires a jitter free 77.76 MHz line side clock reference with a tolerance of +/- 20ppm. This reference clock can be generated onboard, with a PECL oscillator, or a HCMOS/TTL oscillator. The reference clock can also be supplied externally, through a SMB connector on the front panel, or from the backplane. It should be note that when reference clock is supplied from the backplane or the front panel, the line side clock will be synchronous with the system clock.

System clocks for the SPECTRA-622, TUPP-PLUS-622, backplane and the FPGA are generated using the Cypress CY7B991V, programmable skew clock buffer. These multiple-output clock buffers provide the system with a number of low skew clocks and if necessary, the delay between each clock, can be programmed to optimize timing.

7.7 Power

Power requirements for the board are +5 Volts and +3.3 Volts and is supplied from the backplane through CPCI connector J1. linear regulators will be used produce the +2.5 Volts for the TUPP-PLUS-622 core and the +3.3 Volts for the SPECTRA-622 analog power. Front panel LEDs will be used to indicate power status.

7.8 Telecom Bus

The telecom bus supports a single STS-12 (STM-4) 77.76 MHz byte bus or a quad STS-3 (STM-1) 19.44 MHz byte bus.

7.9 Mechanical Form Factor

The board is a based on the CPCI 6U (233.35 mm by 160 mm) board size. Rear connectors are numbered J1, J3 and J5 starting at the bottom connector. J1 is used for the 32 bit CPCI signals. J3 and J5 will carry the telecom bus and DS3 signals.

Table 2 J3 Pin Assignment

	A	B	C	D	E	F
1	DC1J1V1[3]	GND	DPL[3]	GND	DDP[3]	GND
2	DTPL[3]	DTV5[3]	ROBO[3]	RSV	RSV	GND
3	AD[24]	AD[25]	GND	AD[26]	AD[27]	GND
4	AD[28]	GND	AD[29]	GND	AD[30]	GND
5	AD[31]	AC1J1V1[4]	APL[4]	ADP[4]	LAC1[4]	GND
6	DD[24]	DD[25]	GND	DD[26]	DD[27]	GND
7	DD[28]	GND	DD[29]	GND	DD[30]	GND
8	DD[31]	DC1J1V1[4]	DPL[4]	DDP[4]	DTPL[4]	GND
9	DTV5[4]	ROBO[4]	GND	SPARE5	SPARE6	GND
10	POHCK	GND	RAD[1]	GND	RAD[2]	GND
11	RAD[3]	RAD[4]	POHFP[1]	POHFP[4]	POHFP[7]	GND
12	POHFP[10]	DS3RICLK	GND	DS3ROCLK[1]	DS3ROCLK[5]	GND
13	DS3ROCLK[9]	GND	DS3RDAT[1]	GND	DS3RDAT[9]	GND
14	RSV	DS3TICLK[1]	DS3TICLK[5]	DS3RDAT[5]	DS3TIDAT[1]	GND
15	DS3TIDAT[5]	DAS3T1DAT[9]	GND	DS3TICLK[9]	TXRNG[1]	GND
16	TXRNG[2]	GND	TXRNG[3]	GND	RXRNG[1]	GND
17	RXRNG[2]	RXRNG[3]	SPARE7	RSV	RSV	GND
18	GND	GND	GND	GND	GND	GND
19	RCLK	RSV	RSV	RSV	EXTREF	GND

Table 3 J5 Pin Assignment

	A	B	C	D	E	F
1	GND	AD[0]	GND	AD[1]	AD[2]	GND
2	AD[3]	AD[4]	AD[5]	AD[6]	AD[7]	GND
3	AC1J1V1[1]	GND	APL[1]	GND	ADP[1]	GND
4	GND	LAC1[1]	GND	SPARE1	RSV	GND
5	RSV	ROBO[1]	RSV	SPARE2	RSV	GND
6	DD[0]	GND	DD[1]	GND	DD[2]	GND
7	GND	DD[3]	GND	DD[4]	DD[5]	GND
8	DD[6]	DD[7]	DC1J1V1[1]	DPL[1]	DDP[1]	GND
9	DTPL[1]	GND	DTV5[1]	GND	SPARE3	GND
10	GND	AD[8]	GND	AD[9]	AD[10]	GND
11	AD[11]	AD[12]	AD[13]	AD[14]	AD[15]	GND
12	AC1J1V1[2]	GND	APL[2]	GND	ADP[2]	GND
13	GND	LAC1[2]	GND	DD[8]	DD[9]	GND
14	DD[10]	DD[11]	DD[12]	DD[13]	DD[14]	GND
15	DD[15]	GND	DC1J1V1[2]	GND	DPL[2]	GND
16	GND	DDP[2]	GND	DTPL[2]	DTV5[2]	GND
17	ROBO[2]	AD[16]	AD[17]	AD[18]	AD[19]	GND
18	AD[20}	GND	AD[21]	GND	AD[22]	GND
19	GND	AD[23]	GND	AC1J1V1[3]	APL[3]	GND
20	ADP[3]	LAC1_3	SPARE4	DD[16]	DD[17]	GND
21	DD[18]	GND	DD[19]	GND	DD[20]	GND
22	GND	DD[21]	GND	DD[22]	DD[23]	GND

Table 4 J3 and J5 Signal Description

Signal Name	Type	Connector/Pin	Function
AD[0]	I	J4/B1	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[7:0]) contains the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) SONET/SDH payload data to transmit. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[7:0]) contains the 1st STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit.
AD[1]	I	J4/D1	
AD[2]	I	J4/E1	
AD[3]	I	J4/A2	
AD[4]	I	J4/B2	
AD[5]	I	J4/C2	
AD[6]	I	J4/D2	
AD[7]	I	J4/E2	
AD[8]	I	J4/B10	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[15:8]) inputs are unused and should be tied low. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[15:8]) contains the 2nd STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit.
AD[9]	I	J4/D10	
AD[10]	I	J4/E10	
AD[11]	I	J4/A11	
AD[12]	I	J4/B11	
AD[13]	I	J4/C11	
AD[14]	I	J4/D11	
AD[15]	I	J4/E11	
AD[16]	I	J4/B17	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[23:16]) inputs are unused and should be tied low. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[23:16]) contains the 3rd STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit.
AD[17]	I	J4/C17	
AD[18]	I	J4/D17	
AD[19]	I	J4/E17	
AD[20]	I	J4/A18	
AD[21]	I	J4/C18	
AD[22]	I	J4/E18	
AD[23]	I	J4/B19	
AD[24]	I	J5/A3	In single ADD bus interface STS-12 (STM-4) mode, the ADD bus data (AD[31:24]) inputs are unused and should be tied low. In quad ADD bus interface STS-3 (STM-1) mode, the ADD bus data (AD[31:24]) contains the 4th STS-3/3c (STM-1/AU3/AU4) SONET/SDH payload data to transmit.
AD[25]	I	J5/B3	
AD[26]	I	J5/D3	
AD[27]	I	J5/E3	
AD[28]	I	J5/A4	
AD[29]	I	J5/C4	
AD[30]	I	J5/E4	
AD[31]	I	J5/A5	

Signal Name	Type	Connector/Pin	Function
APL[1]	I	J4/C3	The ADD bus payload active signals APL[4:1] indicate when AD[7:0], AD[15:8], AD[16:23], and AD[24:31] respectively, are carrying payload bytes.
APL[2]	I	J4/C12	
APL[3]	I	J4/E19	
APL[4]	I	J5/C5	
AC1J1V1[1]	I	J4/A3	The ADD bus composite timing signals (AC1J1V1[4:1]) indentify the frame and optionally the payload and tributary multi-frame boundaries on the ADD data bus signals AD[7:0]], AD[15:8], AD[16:23], and AD[24:31] respectively.
AC1J1V1[2]	I	J4/A12	
AC1J1V1[3]	I	J4/D19	
AC1J1V1[4]	I	J5/B5	
ADP[1]	I	J4/E3	The ADD bus data parity signals (ADP[4:1]) indicate the parity of the ADD bus signals AD[7:0], AD[15:8], AD[16:23], and AD[24:31] respectively.
ADP[2]	I	J4/E12	
ADP[3]	I	J4/A20	
ADP[4]	I	J5/D5	
LAC1[1]	O	J4/B4	The line add C1 frame pulse signals (LAC1[4:1]) identify the frame and multi-frame boundaries on the ADD data bus signals AD[7:0]], AD[15:8], AD[16:23], and AD[24:31] respectively.
LAC1[2]	O	J4/B13	
LAC1[3]	O	J4/B20	
LAC1[4]	O	J5/E5	
ROBO[1]	O	J4/B5	ROBO[4:1] provide timing signals for the ADD and Drop bus and can be set to either 19.44 MHz or 77.76 MHz. The duty cycle is nominally 50%.
ROBO[2]	O	J4/A17	
ROBO[3]	O	J5/C2	
ROBO[4]	O	J5/B9	
DD[0]	O	J4/A6	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[7:0]) contains the STS-12/12c (STM-4/AU3/AU4/AU4-Xc) received SONET/SDH payload data. In quad DROP bus interface STS-3(STM-1) mode, the DROP bus data (DD[7:0]) contains the 1st STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data.
DD[1]	O	J4/C6	
DD[2]	O	J4/E6	
DD[3]	O	J4/B7	
DD[4]	O	J4/D7	
DD[5]	O	J4/E7	
DD[6]	O	J4/A8	
DD[7]	O	J4/B8	

Signal Name	Type	Connector/Pin	Function
DD[8]	O	J4/D13	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[15:8]) is forced low. In quad DROP bus interface STS-3(STM-1) mode, the DROP bus data (DD[15:8]) contains the 2nd STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data.
DD[9]	O	J4/E13	
DD[10]	O	J4/A14	
DD[11]	O	J4/B14	
DD[12]	O	J4/C14	
DD[13]	O	J4/D14	
DD[14]	O	J4/E14	
DD[15]	O	J4/A15	
DD[16]	O	J4/D20	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[23:16]) is forced low. In quad bus interface STS-3(STM-1) mode, the DROP bus data (DD[15:8]) contains the 3rd STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data.
DD[17]	O	J4/E20	
DD[18]	O	J4/A21	
DD[19]	O	J4/C21	
DD[20]	O	J4/E20	
DD[21]	O	J4/B21	
DD[22]	O	J4/D22	
DD[23]	O	J4/E22	
DD[24]	O	J5/A6	In single DROP bus interface STS-12(STM-4) mode, the DROP bus data (DD[31:24]) is forced low. In quad bus interface STS-3(STM-1) mode, the DROP bus data (DD[31:24]) contains the 4th STS-3/3c (STM-1/AU3/AU4) received SONET/SDH payload data.
DD[25]	O	J5/B6	
DD[26]	O	J5/D6	
DD[27]	O	J5/E6	
DD[28]	O	J5/A7	
DD[29]	O	J5/C7	
DD[30]	O	J5/E7	
DD[31]	O	J5/A8	
DPL[1]	O	J4/D8	The active high DROP bus payload active signals (DPL[4:1]) indicate when DD[7:0], DD[15:8], DD[24:16], and DD[31:24] respectively are carrying payload bytes. It is set high during path overhead and payload bytes and low during transport overhead bytes.
DPL[2]	O	J4/E15	
DPL[3]	O	J5/C1	
DPL[4]	O	J5/C8	
DTPL[1]	O	J4/A9	The active high DROP bus tributary payload active signals (DTPL[4:1]) indicate when DD[7:0], DD[15:8], DD[24:16], and DD[31:24] respectively are carrying tributary payload bytes overhead bytes.
DTPL[2]	O	J4/D16	
DTPL[3]	O	J5/A2	
DTPL[4]	O	J5/E8	

Signal Name	Type	Connector/Pin	Function
DC1J1V1[1]	O	J4/C8	The DROP bus composite timing signals (DC1J1V1[4:1]) indicate the frame, payload and tributary multi-frame boundaries on the DROP data bus signals DD[7:0], DD[15:8], DD[24:16], and DD[31:24] respectively.
DC1J1V1[2]	O	J4/C15	
DC1J1V1[3]	O	J5/A1	
DC1J1V1[4]	O	J5/B8	
DTV5[1]	O	J4/C9	The DROP bus tributary V5 signals (DTV5[4:1]) mark the tributary V5 bytes on the DROP data bus signals DD[7:0], DD[15:8], DD[24:16], and DD[31:24] respectively.
DTV5[2]	O	J4/E16	
DTV5[3]	O	J5/B2	
DTV5[4]	O	J5/A9	
DDP[1]	O	J4/E8	The DROP bus data parity signals (DDP[4:1]) indicate the parity of the DROP bus signals DD[7:0], DD[15:8], DD[16:23], and DD[24:31] respectively.
DDP[2]	O	J4/B16	
DDP[3]	O	J5/E1	
DDP[4]	O	J5/D8	
RCLK	O	J5/A19	The receive clock (RCLK) output provides timing for the SPECTRA-622 line side interface outputs and is nominally 77.76 MHz with a 50% duty cycle.
EXTREF	I	J5/E19	The external reference (EXTREF) input can be fed with a 77.76 MHz CMOS/TTL clock.
POHCK	O	J5/A10	The tributary path overhead clock (POHCK) signal provides timing to sample the extracted tributary path overhead stream and the receive alarm port for the STM-1/STS-3 #1, #2, #3 and #4. POHCK is a nominally 9.72 MHz clock. The POHFP[1, 4, 7, 10] and RAD[4:1] outputs are updated on the falling edge of POHCK.
RAD[1]	O	J5/C10	The receive alarm ports (RAD[4:1]) contain the tributary path BIP error count, the RDI status and the PDI status of each tributary in the (STM-1/STS) #1,#2, #3, and #4. RAD[4:1] is updated on the falling edge of POHCK.
RAD[2]	O	J5/E10	
RAD[3]	O	J5/A11	
RAD[4]	O	J5/B11	

Signal Name	Type	Connector/Pin	Function
POHFP[1]	0	J5/C11	POHFP[1], POHFP[4], POHFP[7], and POHFP[10] identify frame boundaries of the tributary path overhead bytes from STS-1 (AU3) #1, #4, #7and #10, respectively. In AU4 mode, POHFP[1], POHFP[2] and POHFP[3] identify frame boundaries of TUG3 #1, #4, #7, and #10, respectively. Each POHFP signal is updated on the falling edge of POHCK
POHFP[4]	0	J5/D11	
POHFP[7]	0	J5/E11	
POHFP[10]	0	J5/A12	
DS3RICLK	I	J5/B12	The DS3 receive input clock (DS3RICLK) provides timing for the receive DS3 interface. It is a nominally 44.928 MHz, 50% duty cycle clock. The DS3RICLK is gapped to generate the DS3 receive output clocks (D3ROCLK[3:1]).
DS3ROCLK[1]	O	J5/D12	The DS3 receive output clocks (DS3ROCLK[1, 5, 9]) provide timing to the DS3 received streams that have been de-mapped from the SONET/SDH stream.
DS3ROCLK[5]	O	J5/E12	
DS3ROCLK[9]	O	J5/A13	
DS3RDAT[1]	O	J5/C13	The DS3 receive data (DS3RDAT[1, 5, 9]) output signals contain NRZ encoded data of the DS3 streams that have been de-mapped from the receive SONET/SDH stream STS-3/STM-1 #1.
DS3RDAT[5]	O	J5/D14	
DS3RDAT[9]	O	J5/E13	
DS3TICLK[1]	I	J5/B14	The DS3 transmit input clocks (DS3TICLK[1, 5, 9]) provide timing for the transmit DS3 data streams.
DS3TICLK[5]	I	J5/C14	
DS3TICLK[9]	I	J5/D15	
DS3TIDAT[1]	I	J5/E14	The DS3 transmit data (DS3TDAT[1, 5, 9]) signals contain the DS3 or payload streams to be mapped into the SONET/SDH transmit streams STS-3/STM-1 #1
DS3TIDAT[5]	I	J5/A15	
DS3TIDAT[9]	I	J5/B15	

Signal Name	Type	Connector/Pin	Function
TXRNG[1] : TRCPDAT	I	J5/E15	The transmit ring control port data (TRCPDAT) signal contains the transmit ring control port data stream. The data stream consists of the filtered K1, K2 bytes values, APS status bit, AIS, RDI, and the REI bit positions.
TXRNG[2] : TRCPCLK	I	J5/A16	The transmit ring control port clock (TRCPCLK) signal provides timing for the transmit ring control port. TRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock.
TXRNG[3] : TRCPFP	I	J5/C16	The transmit ring control port frame position (TRCPFP) signal identifies bit positions in the transmit ring control port data (TRCPDAT).
RXRNG[1] : RRCPCLK	O	J5/E16	The receive ring control port clock (RRCPCLK) signal provides timing for the transmit ring control port. RRCPCLK is nominally a 3.24 MHz, 50% duty cycle clock.
RXRNG[2] : RRCPDAT	O	J5/A17	The receive ring control port data (RRCPDAT) signal contains the transmit ring control port data stream. The data stream consists of the filtered K1, K2 bytes values, APS status bit, AIS, RDI, and the REI bit positions.
RXRNG[3] : RRCPFP	O	J5/B17	The receive ring control port frame position (RRCPFP) signal identifies bit positions in the transmit ring control port data (RRCPDAT).

8 IMPLEMENTATION DESCRIPTION

This section describes the hardware implementation of the SPECTRA-622 WITH TUPP-PLUS-622 reference design, as contained in the schematics in Section 9.

8.1 Root Drawing, Sheet 1

This sheet shows the interconnection between the functional blocks of the design.

8.2 OPTICS REFCLK BLOCK, Sheet 2

Sheet 2 shows the system clock PLL drivers, Optics interface, and 77.76 MHz reference clock circuitry.

The system clock (SCLK) comes from the FPGA and is used as a reference for PLL clock driver U6. The recovered clock from U6 is used to supply a reference to PLL clock driver U7. When ROBO_FS is high the PLL clock drivers will expect a 77.76 MHz reference, and when ROBO_FS is low, the clock drivers expect a 19.44 MHz reference. The delay between the clock outputs (SCLK_ROB<7..1>) can be varied by removing or adding 4.7K pull-up and pull-down resistors connected to pins 26, 27, 29, and 30 of U6 and U7 . The 51 Ohm resistors at the output of the clock divers provide some source termination to help prevent reflections.

U5 (HP HFCT-5208) is the Optical Data Link (ODL) which provides the optical to electrical (O/E) function for the SPECTRA-622 device. The HFCT-5208 transceiver is 5V PECL device in a 1 x 9-pin package with a duplex SC receptacle. The PECL signals connect to the SPECTRA-622 on 50 Ohm controlled impedance signal lines and are properly terminated at the ODL and at the SPECTRA-622 device. The 330 Ohms resistors provide source terminations for the PECL outputs and should be located as close as possible to the HFCT-5208. R77, R78, R79, and C25 provide biasing for the SPECTRA-622 PECL TX outputs and should be located as close as possible to the ODL

Y1 is a 77.76 MHz PECL oscillator and provides the line side reference clock for the SPECTRA. When 3.3V optics are used the PECL reference oscillator should be a 3.3V PECL oscillator and when using 5V optics it should be a 5V oscillator. This oscillator should be located as close as possible to the SPECTRA 622 and signal traces should be 50 ohm differential pairs. The 77.76 MHz external TTL line side reference clock is fed to U1 where it is translated to either 3.3V PECL or 5V PECL depending on the optics installed. When 3.3V OPTICS is used the MC100LVELT22 will be installed and if 5V OPTICS is used the MC100ELT22 will

be installed. The 330 ohm resistors at the outputs of U1 provide DC biasing for the PECL driver. The second pair of outputs is used to terminate the RRCLK_P and RRCLK_N inputs of the SPECTRA-622 to the appropriate PECL levels. Solder bridges SB5-SB8 are used to select between the external line side reference clock and the internal line side clock. The 77.76 MHz HCMO/TTL oscillator used to generate the system clocks, can also be used to provide the line side clock reference. This can be done, by opening solder bridge SB3, and closing solder bridge SB4.

8.3 SPECTRA_622_BLOCK, Sheet 3 & 4

The SPECTRA_622_BLOCK shows the SPECTRA-622 signals and the power circuitry.

J8 provides access to the SPECTRA-622 RX and TX overhead and alarm signals. Resistor arrays RN1-RN4 ensure no inputs are left floating.

Resistors R34, R35, and R39 provide terminations for PECL line side inputs signals, REFCLK+/-, RXD+/- and RRCLK+/-. PECREF and PREFEN are tied low through 4.7K ohm resistors to ensure that the PECL bias voltage is set by the internal bandgap reference. A 47 nF capacitor is placed across the loop filter pins C1 and C0, which sets the loop bandwidth of the clock recovery circuit to approximately 500 KHz. A 2k Ohm resistor is placed across the TDREF0 and TDREF1 pins to set calibrated currents for the PECL output transceivers TXD+/- to approximately 15 ma.

Test points T16-T21 provide access to the TPAIS, TPAISFP, TPAISCK, DPAIS, DPAIS, and DPAISCK signals.

The 48 digital power pins are decoupled using 39, .10UF capacitors. A 3.3V low dropout linear regulator (U3 LT1129-3.3) and additional filtering capacitors and resistors are provided to ensure a clean 3.3V power source to analog power pins. U19 and its' associated components can be installed if it is required to generate a clean 3.3V linear regulated supply from a 3.3V supply. The TPS60100 consists of a charge pump followed by a linear regulator.

VBIAS pins (VBIAS<1..0>) are tied to +5V through a 1K resistor, to bias the wells of the digital inputs so that the pads can tolerate 5V on their inputs without forward biasing internal ESD protection devices. PBIAS pins perform the same function for the PECL signals and must be tied to either 3.3V or 5V.

8.4 TUPP_622_BLOCK, Sheets 5, & 6

The TUPP_622_BLOCK shows the TUPP-PLUS-622 signals and the power circuitry.

J6 configures the incoming and outgoing interface mode of the TUPP-PLUS-622 to either 77.76 MHz (STS-12) STM-4 or 19.44 MHz (STS-3) STM-1. J2 and J4 connect the system clock to HSCLK and the GSCLK<0> to the TUPP SCLK when in the 77.76 MHz interface mode, and connect the system clock to the TUPP SCLK when in the 19.44 MHz interface mode.

TUPP-PLUS-622 digital power digital pins are decoupled using 24 0.1 uF capacitors. The 2.5V TUPP core power is generated from the 3.3V supply (VCC) using a low dropout linear regulator (MC3950-2.5T). This ensures that the 3.3V supply should never be at a lower voltage than the 2.5V supply (there is an internal diode between the supplies that shouldn't be forward biased). The regulator and its associated components should be located as close as possible to the TUPP-PLUS-622 device.

8.5 FPGA BLOCK Sheet, 7

The FPGA block shows the FPGA (XC4028XL) signals, decoupling caps, serial EPROM, 77.76 MHz HCMOS/TTL reference oscillator, interrupt LED, and reset circuitry.

U2, U4 and their associated components provide power up and manual reset signals for the FPGA, TUPP-PLUS-622, and SPECTRA-622.

Y2 is a 77.76 MHz, HCMOS/TTL oscillator and is used to generate the reference clock as well as the system clock. It should be located as close as possible to the FPGA.

J9 provides an interface to the FPGA programming port (Xilinx XCHKR port). Headers, J10, J11 and J12 are used to select how the FPGA is to be configured. The FPGA can be configured on power up by a serial EPROM (U15), through the XCHK port, or through the cPCI interface. When using the XCHK port the serial EPROM should be removed. Table 5 below describes the settings for these headers.

Table 5 FPGA Configuration jumper settings

MODE	J10	J11	J12
Serial EPROM	All jumpers on	Pins 2-3	N/C
XCHK Port (J9)	All jumpers off	Pins 3-3	Pins 2-3
cPCI	Only center jumper on	Pins 1-2	Pins 1-2

A number of I/O pins are connected to the SPECTRA-622's overhead and alarm signals. These signals were provided for future custom applications. Several of these pins were brought out into headers (TP's) just in case we wanted to use this device for a different function other than originally envisioned.

The XC1701L EEPROM devices contain 832,528 bits. 20 pin PLCC sockets are used to facilitate ease of changing these programmable devices

8.6 SYS INTERFACE , Sheet 8, 9, & 10

Sheet 8 shows the CPCI connector, PCI bridge chip and power connections. Fuses F1 and F2 are necessary to prevent any serious damage in the event of a short on the +5V or +3.3V power buses. D2 and D3 indicate +3.3 and +5.0V power and are front panel mounted.

Sheet 9 shows the telecom bus interface connector J5 and the telecom bus signals from the FPGA. All signals are buffered through 3.3V CMOS buffers and outputs have 22 ohm series terminations to reduce reflections. When operating at 77.76 MHz it may be necessary to provide Thevenin terminations for add bus (bits [7:0]). If Thevenin terminations are required, install 150 ohm resistors connected to U24 pins 33-36, 37, 38, 40, 41, 43, 44, 46 and 47.

Sheet 10 shows the telecom bus/DS3 bus interface connector J3 and the remainder of the telecom bus signals from the FPGA and the DS3 signals from the SPECTRA-622 signals are buffered through 3.3V CMOS buffers and outputs have 22 ohm series terminations to reduce reflections.

9 SCHEMATICS AND LAYOUT

REVISIONS				
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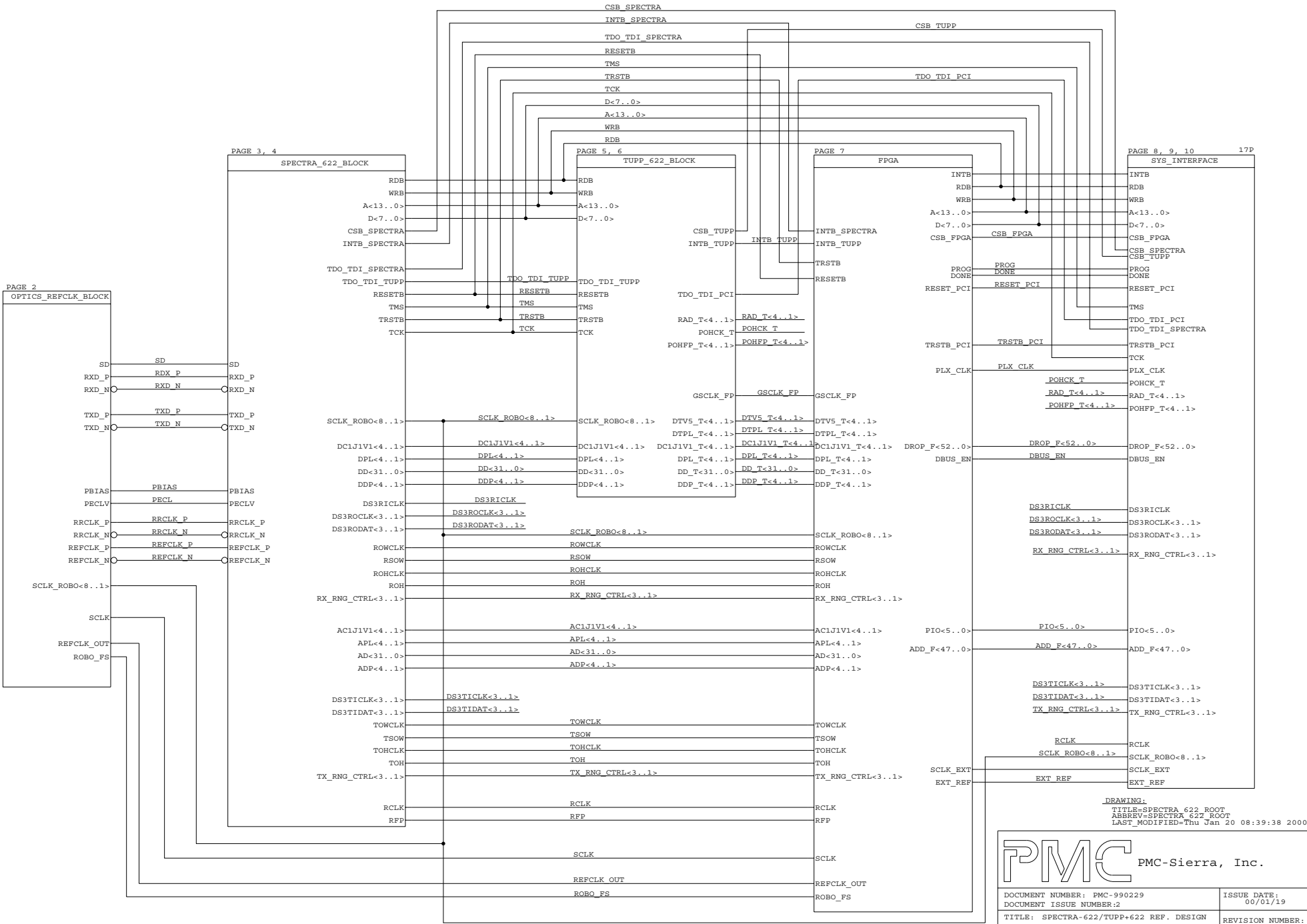

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PMC-Sierra, Inc.

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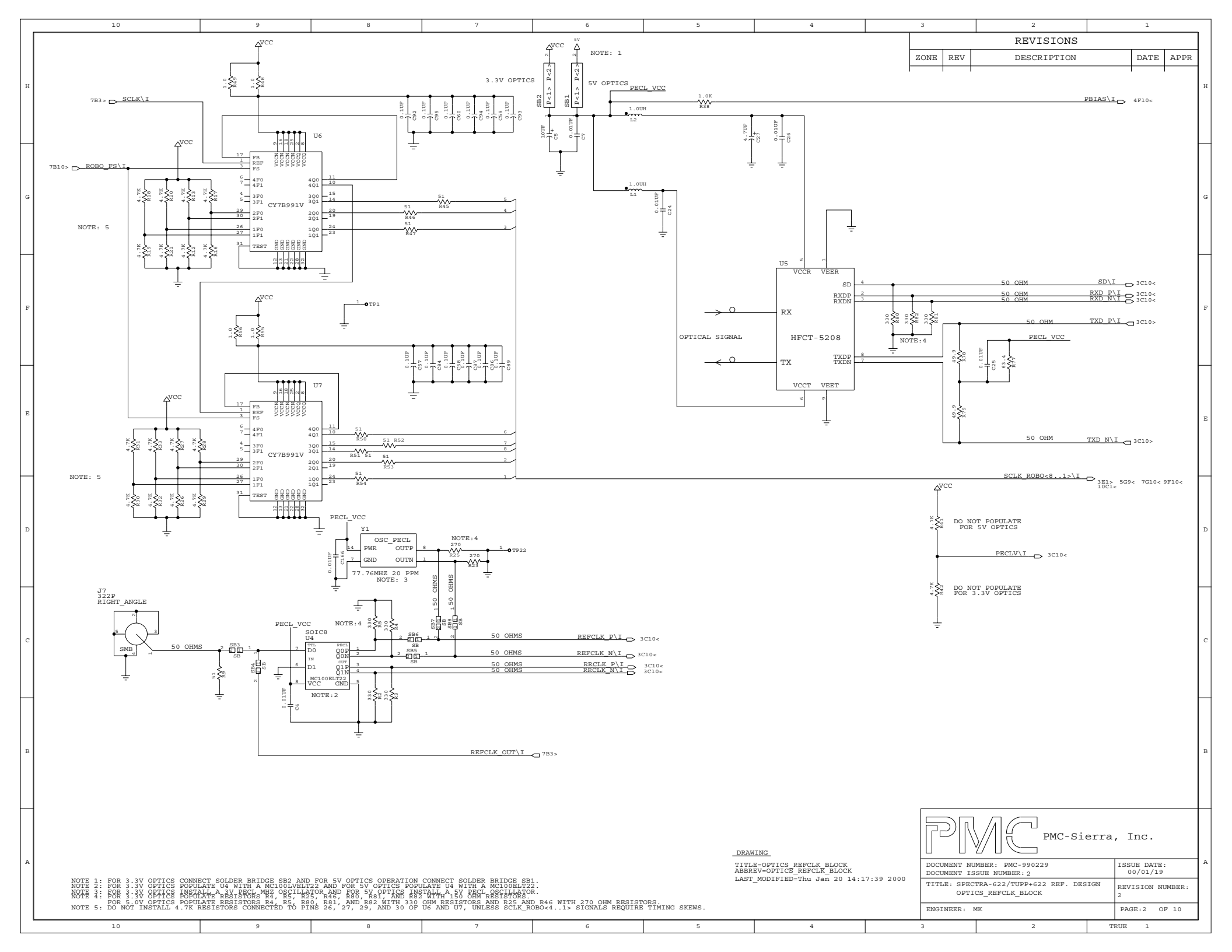
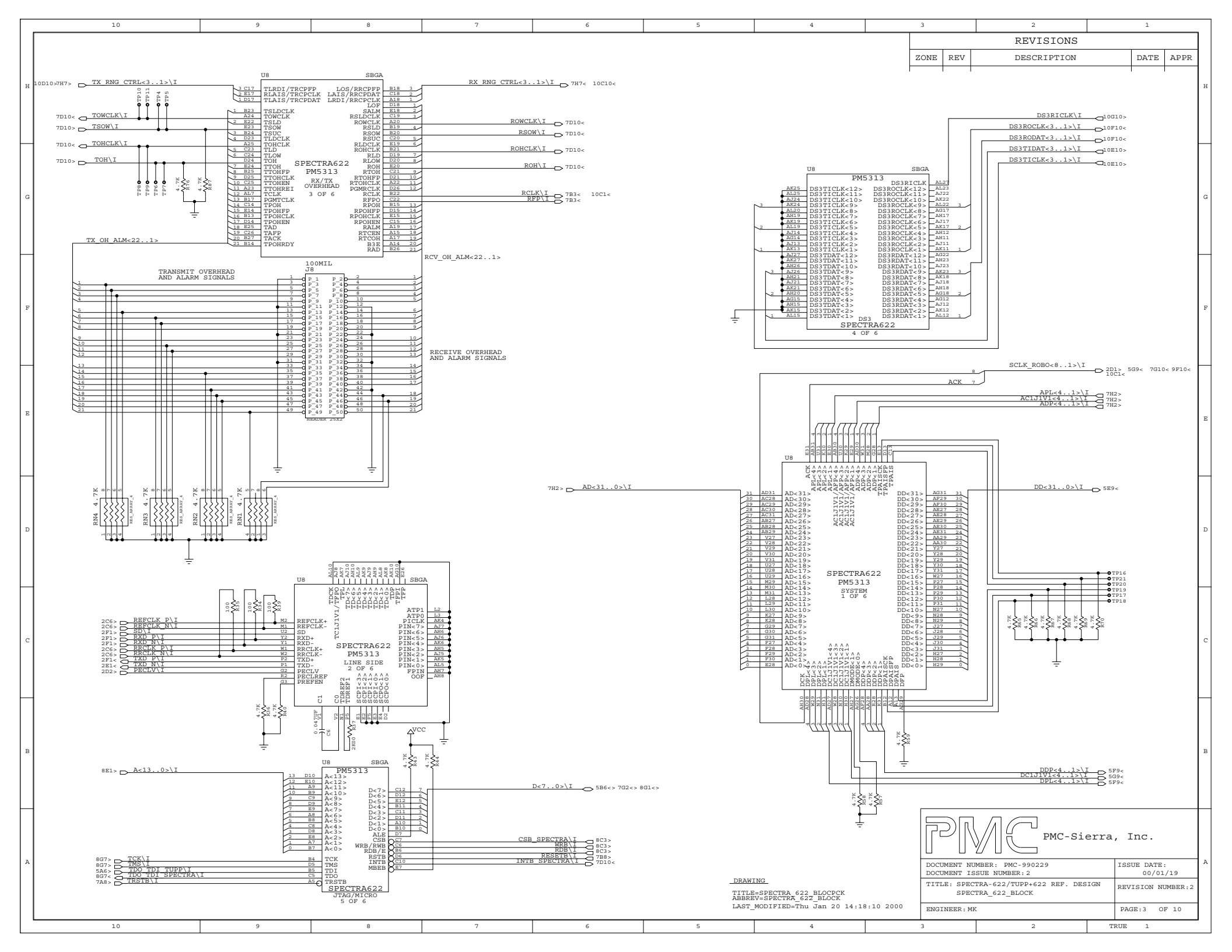
ENGINEER: MK	PAGE:1 OF 10



NOTE 1: FOR 3.3V OPTICS CONNECT SOLDER BRIDGE SB2 AND FOR 5V OPTICS OPERATION CONNECT SOLDER BRIDGE SB1.
NOTE 2: FOR 3.3V OPTICS POPULATE U4 WITH A MC100LVELT22 AND FOR 5V OPTICS POPULATE U4 WITH A MC100ELT22.
NOTE 3: FOR 3.3V OPTICS INSTALL A 3V PECL MHZ OSCILLATOR AND FOR 5V OPTICS INSTALL A 5V PECL OSCILLATOR.
NOTE 4: FOR 3.3V OPTICS POPULATE RESISTORS R4, R5, R25, R46, R80, R81, AND R82 WITH 150 OHM RESISTORS.
FOR 5.0V OPTICS POPULATE RESISTORS R4, R5, R80, R81, AND R82 WITH 330 OHM RESISTORS AND R25 AND R46 WITH 270 OHM RESISTORS.
NOTE 5: DO NOT INSTALL 4.7K RESISTORS CONNECTED TO PINS 26, 27, 29, AND 30 OF U6 AND U7, UNLESS SCLK_ROBO<4..1> SIGNALS REQUIRE TIMING SKEWS.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RX_RNG_CTRL<3..1>\I
TOWCLK\I
TSOW\I
TOHCLK\I
TOH\I
ROWCLK\I
RSOW\I
ROHCLK\I
ROH\I
RCLK\I
RFP\I
TX_OH_ALM<22..1>
RCV_OH_ALM<22..1>
TRANSMIT OVERHEAD AND ALARM SIGNALS
RECEIVE OVERHEAD AND ALARM SIGNALS
100MIL J8
HEADER 25X2
SPECTRA622 PM5313 RX/TX OVERHEAD 3 OF 6
SPECTRA622 PM5313 DS3 4 OF 6
SPECTRA622 PM5313 SYSTEM 1 OF 6
SPECTRA622 PM5313 LINE SIDE 2 OF 6
SPECTRA622 PM5313 JTAG/MICRO 5 OF 6
DS3RICLK\I
DS3ROCLK<3..1>\I
DS3RODAT<3..1>\I
DS3TIDAT<3..1>\I
DS3TICLK<3..1>\I
SCLK_ROBO<8..1>\I
ACK
APL<4..1>\I
AC1J1V1<4..1>\I
ADP<4..1>\I
AD<31..0>\I
DD<31..0>\I
DDP<4..1>\I
DC1J1V1<4..1>\I
DPL<4..1>\I
A<13..0>\I
D<7..0>\I
CSB_SPECTRA\I
WRB\I
RDB\I
RESETB\I
INTB_SPECTRA\I
TCK\I
TMS\I
TDO_TDI_TUPP\I
TDO_TDI_SPECTRA\I
TRSTB\I
VCC
RN4 4.7K
RN3 4.7K
RN2 4.7K
RN1 4.7K
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-990229
DOCUMENT ISSUE NUMBER:2
ISSUE DATE: 00/01/19
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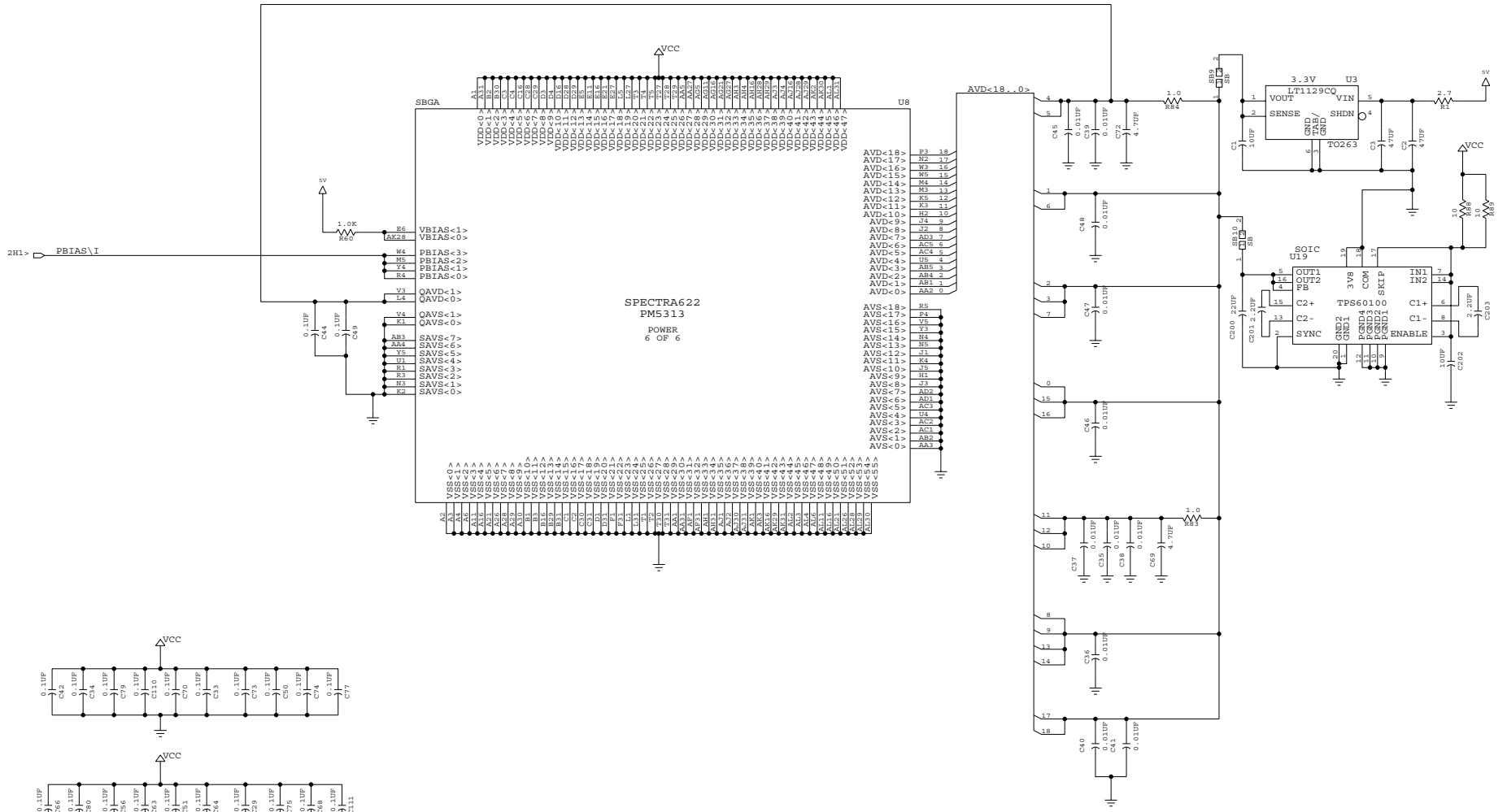

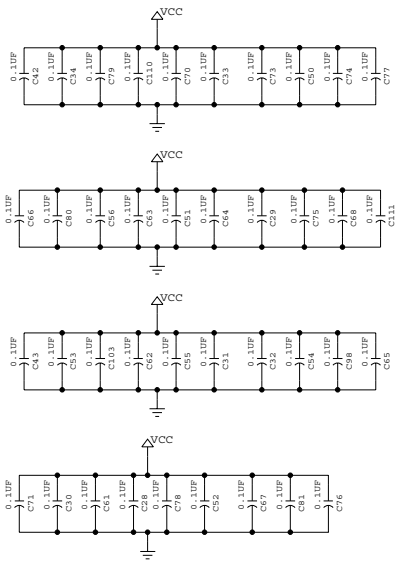

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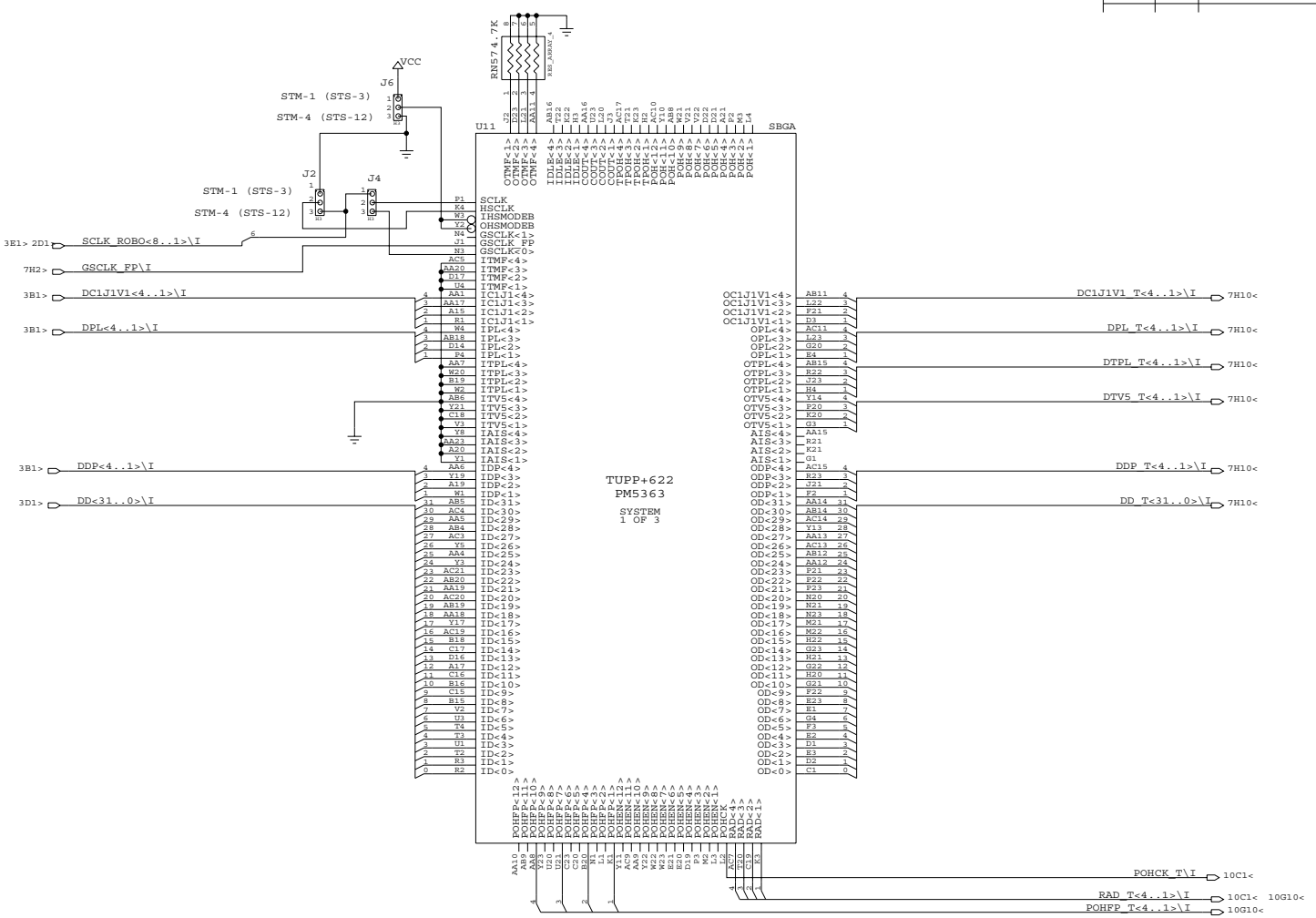

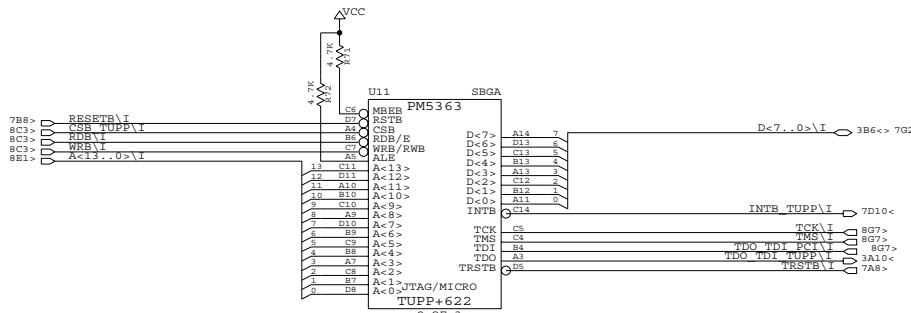

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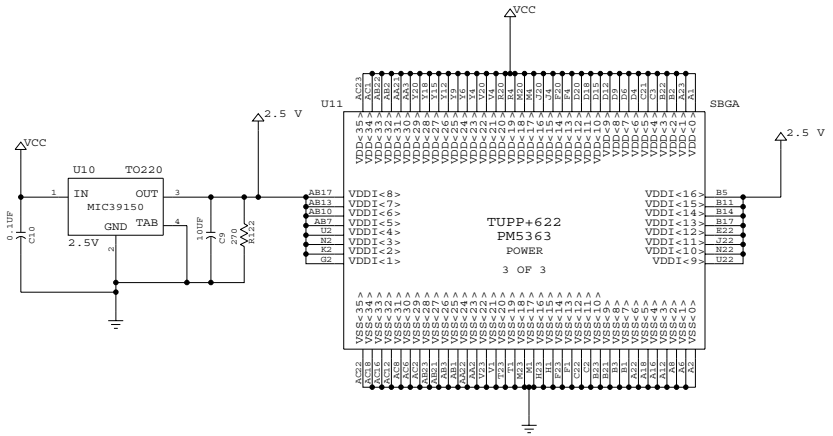

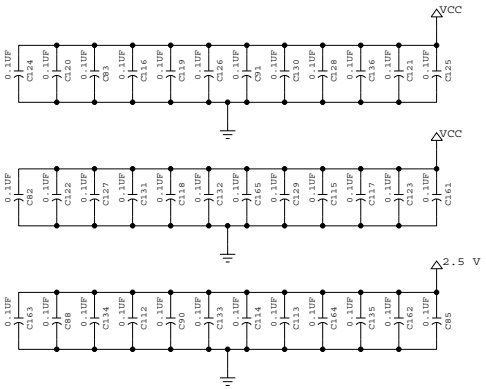

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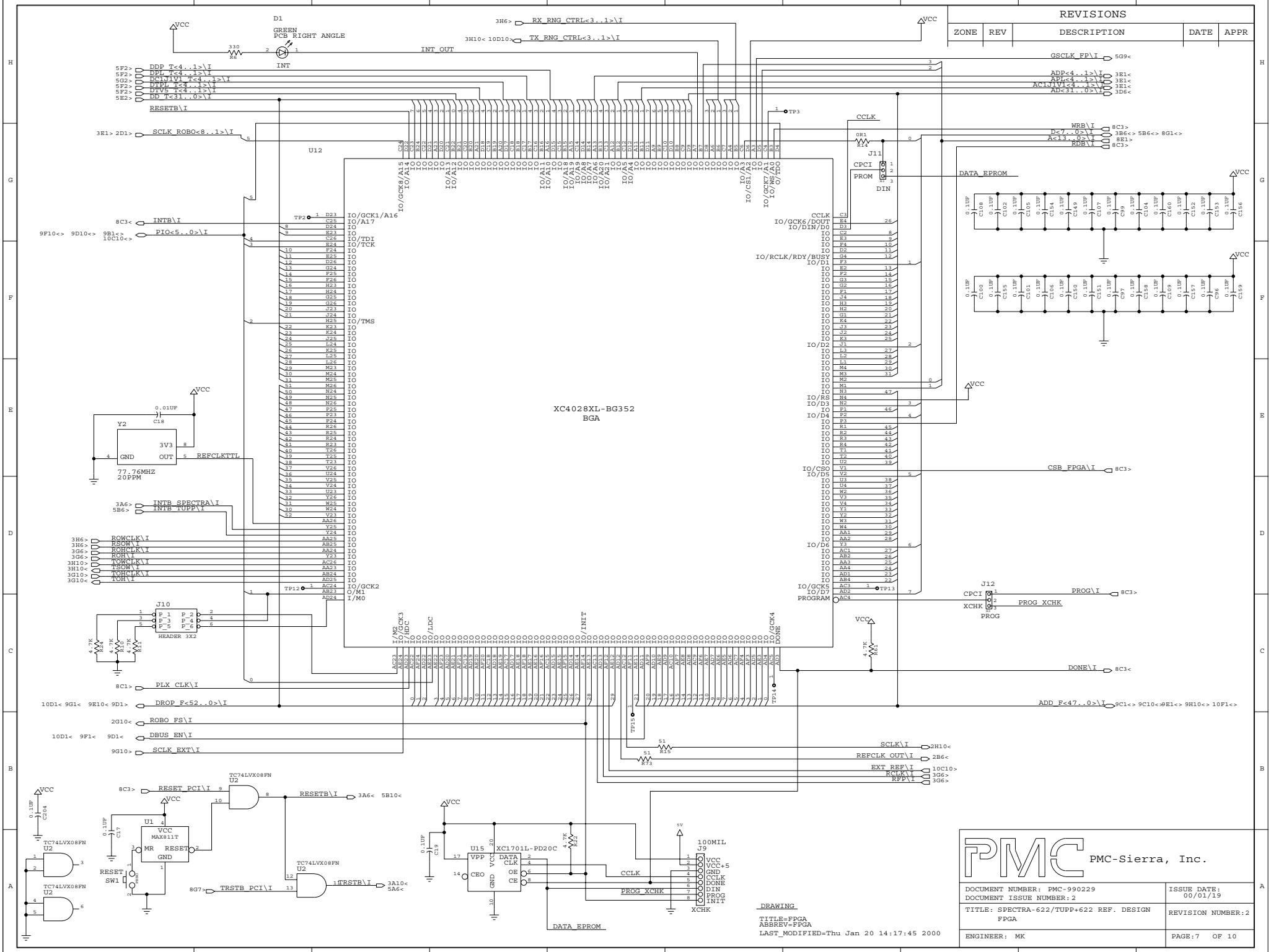
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BGA
U12
J10
HEADER 3X2
J11
CPCI
PROM
DIN
J12
PROG
XCHK
Y2
77.76MHZ
20PPM
U1
MAX811T
U2
TC74LVX08FN
U15
XC1701L-PD20C
J9
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SW1
RESET
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DOCUMENT ISSUE NUMBER:2
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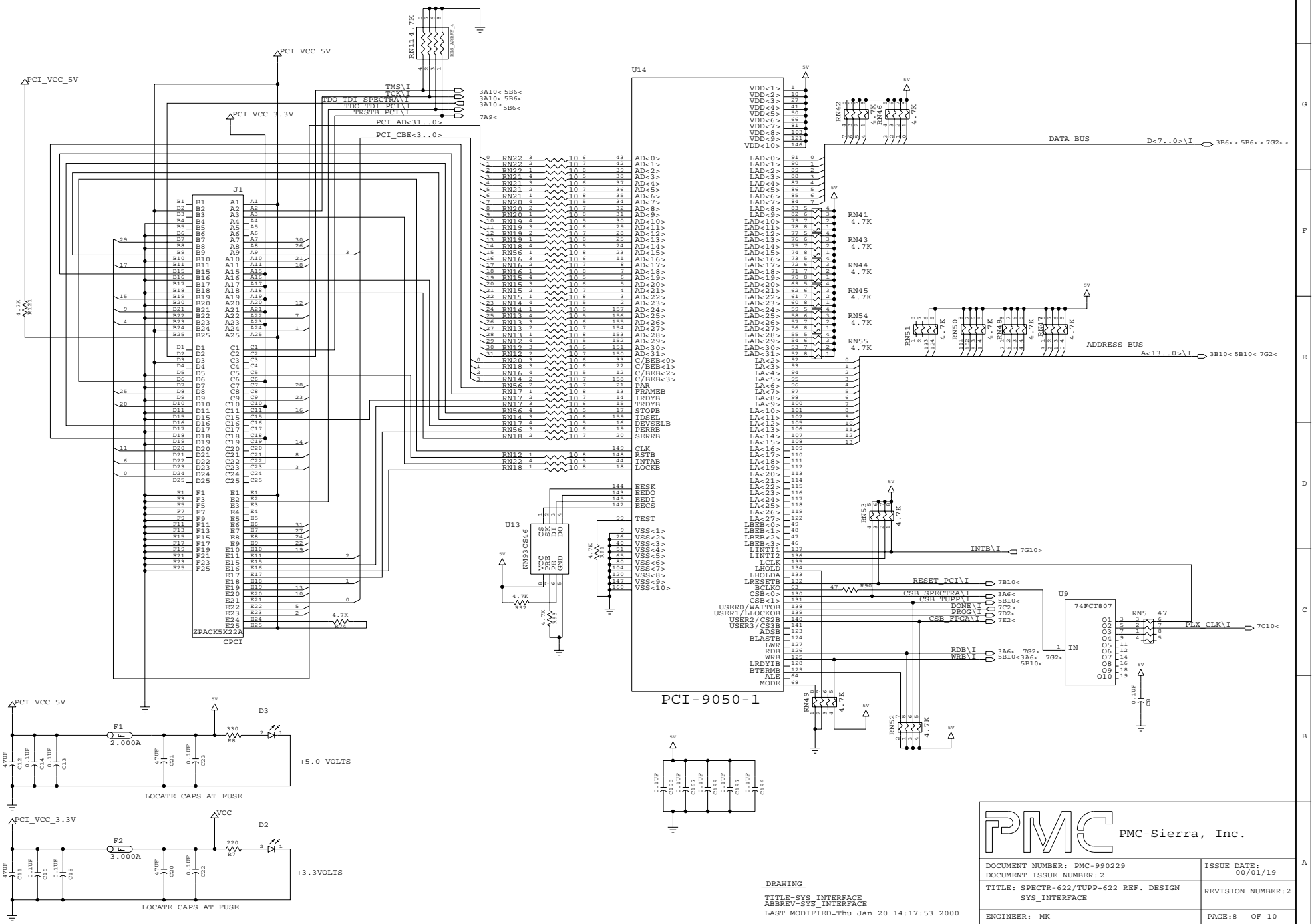

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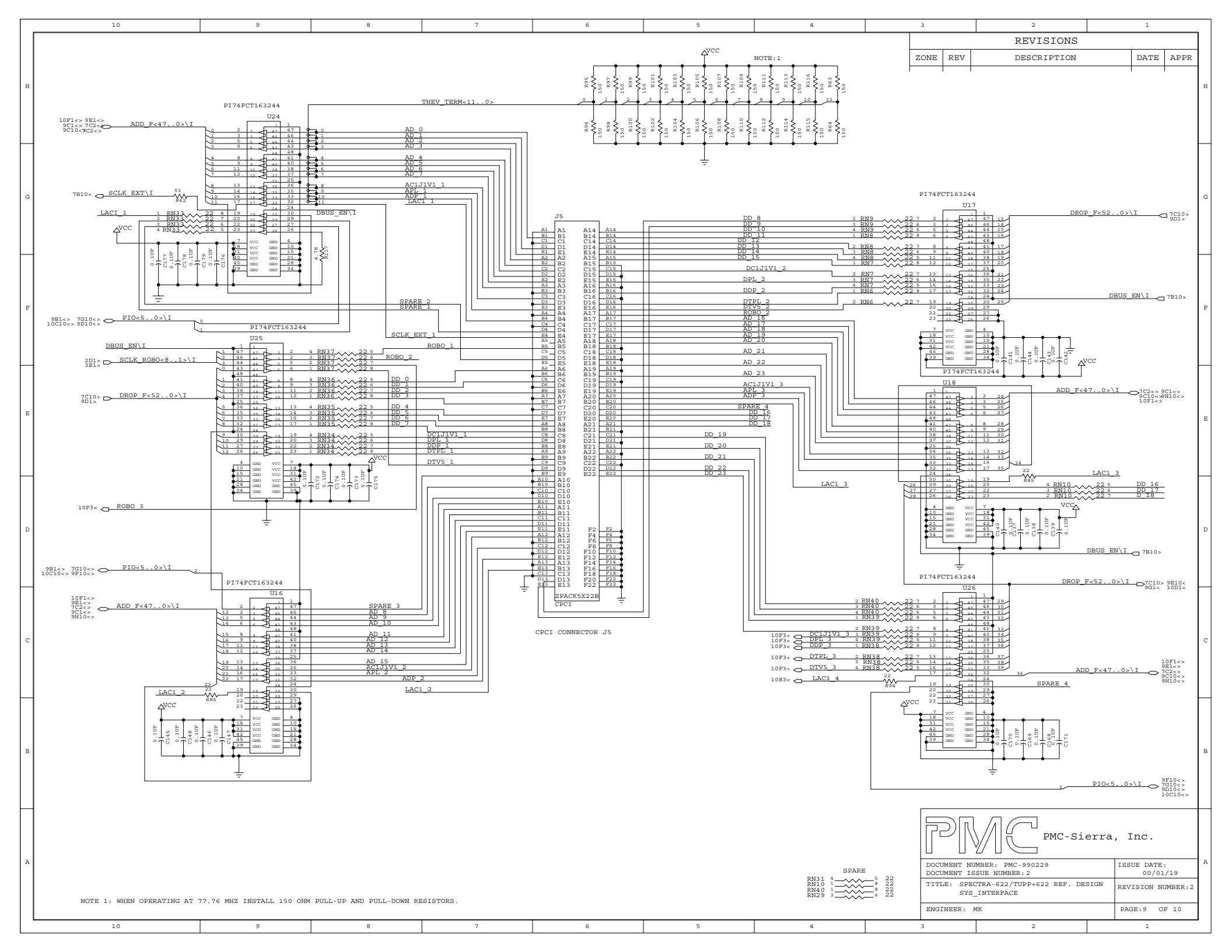
ENGINEER: MK	PAGE:8 OF 10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U24
ADD_F<47..0>\I
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AD_1
AD_2
AD_3
AD_4
AD_5
AD_6
AD_7
AC1J1V1_1
APL_1
ADP_1
LAC1_1
SCLK_EXT\I
DBUS_EN\I
PIO<5..0>\I
SPARE_2
SPARE_1
SCLK_EXT_1
ROBO_1
U25
SCLK_ROBO<8..1>\I
ROBO_2
DROP_F<52..0>\I
DD_0
DD_1
DD_2
DD_3
DD_4
DD_5
DD_6
DD_7
DC1J1V1_1
DPL_1
DDP_1
DTPL_1
DTV5_1
ROBO_3
U16
SPARE_3
AD_8
AD_9
AD_10
AD_11
AD_12
AD_13
AD_14
AD_15
AC1J1V1_2
APL_2
ADP_2
LAC1_2
J5
ZPACK5X22B
CPCI
CPCI CONNECTOR J5
DD_8
DD_9
DD_10
DD_11
DD_12
DD_13
DD_14
DD_15
DC1J1V1_2
DPL_2
DDP_2
DTPL_2
DTV5_2
ROBO_2
AD_16
AD_17
AD_18
AD_19
AD_20
AD_21
AD_22
AD_23
AC1J1V1_3
APL_3
ADP_3
SPARE_4
DD_16
DD_17
DD_18
DD_19
DD_20
DD_21
DD_22
DD_23
LAC1_3
LAC1_4
U17
U18
U26
SPARE
NOTE 1: WHEN OPERATING AT 77.76 MHZ INSTALL 150 OHM PULL-UP AND PULL-DOWN RESISTORS.
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-990229
DOCUMENT ISSUE NUMBER:2
ISSUE DATE: 00/01/19
TITLE: SPECTRA-622/TUPP+622 REF. DESIGN SYS_INTERFACE
REVISION NUMBER:2
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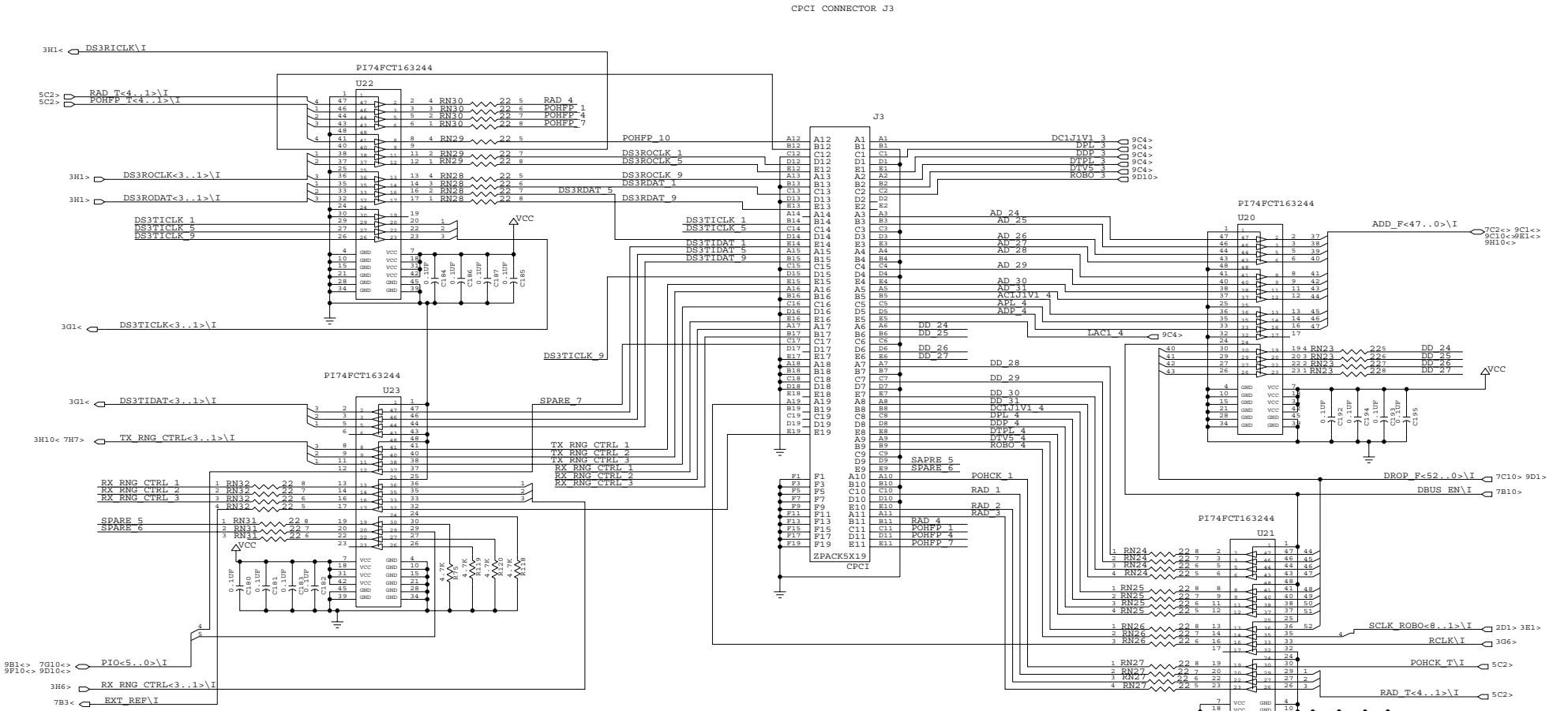

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TITLE: SPECTRA-622/TUPP+622 REF. DESIGN SYS_INTERFACE	REVISION NUMBER:2
ENGINEER: MK	PAGE:10 OF 10

10 BILL OF MATERIAL

Table 6 Bill of Materials

Item	Ref. No	Description	Manufactures Part #
1	C4, C7, C18, C24-C26, C35-C41, C45-C48, C166	CAPACITOR, 0.01UF, 50V, X7R_805 ± 10%	DIGI-KEY – PCC103BNCT-ND
2	C6	CAPACITOR, .047UF, 50V, X7R ± 5%	AVX - 08055C473JATN
3	C8, C10, C13-C17, C19, C22, C23, C28-C34, C42-C44, C49-C68, C70, C71, C73-C165, C167-C199, C204.	CAPACITOR, 0.1UF, 50V, X7R_805 ± 10%	AVX - 08055C104KAT
4	C27, C69, C72	CAPACITOR, 4.7UF, 6.3V, TANT TEH	DIGI-KEY – PCS1475CT-ND
5	C1, C5, C9	CAPACITOR, 10UF, 6.3V, TANT TEH	DIGI-KEY – PCS1106CT-ND
6	C11, C12, C20, C21	CAPACITOR, 47UF, 16V, ELECTRO	DIGI-KEY - P1210-ND
7	C2, C3	CAPACITOR, 47UF, 6.3V, TANT TEH	DIGI-KEY - PCT1476CT-ND
8	D1-D3	LED-Green, PCB Right angle	DIGI-KEY - LU20095-ND
9	F1	2.0 Amp FUSE & SOCKET	DIGI-KEY - F1224CT-ND
10	F2	3.0 Amp FUSE & SOCKET	DIGI-KEY - F1226CT-ND
11	J3	ZPACK5X19FH_SCPCI_2M M	352171-1
12	J5	ZPACK5X22FH_BSCPI_2M M	352152-1
13	J1	ZPACK5X22FH_ASCPCI_2 MM	352068-1
14	J9	HEADER .1 " 1 x 8	DIGI-KEY – S1011-36-ND
15	J2, J4, J6, J11, J12	HEADER .1 " 1 x 3	DIGI-KEY – S1011-36-ND

Item	Ref. No	Description	Manufactures Part #
16	J8	HEADER .1 " 25X2	DIGI-KEY - S2011-36-ND
17	J10	HEADER .1 " 3X2	DIGI-KEY - S2011-36-ND
18	L1, L2	Inductor, 1.0UH	DIGI-KEY - PCT1187CT-ND
19	R1	RESISTOR-2.7, 5%, 1206	DIGI-KEY - P<VALUE>PCT-ND
20	R54	RESISTOR-0, 5%, 805	DIGI-KEY – P.10BCT-ND
21	R48, R49, R55, R56, R83, R84	RESISTOR-1.0, 5%, 805	DIGI-KEY - P<VALUE>BCT-ND
22	R38, R60	RESISTOR-1.0K, 5%, 805	DIGI-KEY - P<VALUE>ACT-ND
23	R34, R35, R39	RESISTOR-100, 1%, 805	DIGI-KEY - P<VALUE>CCT-ND
24	R63, R64, R95-R116	RESISTOR-150, 5%, 603	DIGI-KEY - P<VALUE>ACT-ND
25	R85, R86, R94	RESISTOR-22, 5%, 805	DIGI-KEY - P<VALUE>ACT-ND
26	R7	RESISTOR-220, 5%, 805	DIGI-KEY - P<VALUE>ACT-ND
27	R25, R46	RESISTOR-270, 5%, 805	DIGI-KEY - P<VALUE>ACT-ND
28	R37	RESISTOR-2.0K, 1%, 805	DIGI-KEY – P2.00KCCT-ND
29	R2-R6, R8, R80-R82	RESISTOR-330, 5%, 805	DIGI-KEY - P<VALUE>ACT-ND
30	R12, R13, R16-R21, R26-R33, R36, R40-R44, R47, R50-R52, R57-R59, R61, R65-R72, R74-R76, R87 R91-R93, R117-R121	RESISTOR-4.7K, 5%, 805	DIGI-KEY - P<VALUE>ACT-ND
19	R122	RESISTOR-270, 5%, 1206	DIGI-KEY - P<VALUE>PCT-ND
31	R90	RESISTOR-47, 5%, 805	DIGI-KEY - P47ACT-ND

Item	Ref. No	Description	Manufactures Part #
32	R78, R79	RESISTOR-49.9, 1%, 805	DIGI-KEY - P<VALUE>CCT-ND
33	R9-R11, R14, R15, R22-R24, R45, R53, R62	RESISTOR-47, 5%, 805	DIGI-KEY - P47ACT-ND
34	R77	RESISTOR-63.4, 1%, 805	DIGI-KEY - P<VALUE>CCT-ND
35	RN12-RN22, RN56	RES_ARRAY_4_SMD-10	DIGI-KEY - Y4<VALUE CODE>-ND
36	RN6-RN10, RN23-RN40	RES_ARRAY_4_SMD-22	DIGI-KEY - Y4<VALUE CODE>-ND
37	RN1-RN4, R11, RN41-RN55, RN57	RES_ARRAY_4_SMD-4.7K	DIGI-KEY - Y4<VALUE CODE>-ND
38	RN5	RES_ARRAY_4_SMD-47	DIGI-KEY - Y4<VALUE CODE>-ND
39	SW1	Right Angle SPST Push button	DIGI-KEY - CKN4002-ND
40	Y1	PECL Oscillator 77.76 MHz ± 20 ppm	CONNOR WINFIELD EE14-541-77.76 MHz
41	Y2	HCMOS/TTL Oscillator 77.76 MHz ± 20 ppm	MMD-MB3020H48-77.76MHz
42	U1	5V Dual TTL/PECL Translator 3.3V Dual TTL/PECL Translator	MOT - MC100ELT22 MOT - MC100LVELT22
43	U2	74HC08, Quad and gate	TOSHIBA – TC74LVX08FN
44	U3	LT1129-3.3, 3.3V Low Dropout Linear regulator	Linear Technology - LT1129CQ-3.3
45	U4	MAX811_EUS-T, Voltage Monitor with Reset	MAXIM - MAX811_EUS-T
46	U5	HP SC Duplex Single Mode Optical Transceiver	HP – HFCT-5208B
47	U6, U7	CY7B991V, Programmable skew clock buffer	CYPRESS - CY7B991V-5JC
48	U8	PMC-5313 SPECTRA-622 520 Pin SBGA	PMC - PM5313
49	U9	74FCT807, 10 bit clock Buffer	IDT – IDT74FCT807BTSO

Item	Ref. No	Description	Manufactures Part #
50	U10	MIC39150-2.5, 2.5V Low dropout Regulator	MICREL - MIC39150-2.5BT
51	U11	PMC-5363 TUPP-PLUS-622 304 Pin SBGA	PMC - PM5363
52	U12	XC4028XLA FPGA 352 Pin BG352	XILINX-XC4028XLA - 09BG352C
53	U13	NM93CS46 Serial EEPROM	NATIONAL-NM93CS46EN
54	U14	PCI9050 PCI BUS Target Interface chip 160 Pin PQFP-	PLX - PCI9050-1
55	U15	XC1701 Serial OTP EPROM	XILINX – XC1701
56	U16-U21, U23-U26	74FCT163244, 16 bit buffer	PI – PI74FCT163244V

NOTES

CONTACTING PMC-SIERRA, INC.

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Canada V5A 4V7

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Web Site: http://www.pmc-sierra.com

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