08/16/00

Errata: CS8420-CS Rev. D Performance Update

(Reference CS8420 Data Sheet revision DS245PP2 dated Aug '99)

1. On page 9 of the data sheet it is specified that in I2C mode, SCL has a maximum rise time of 1µS and a maximum fall time of 300 nS. The actual rise and fall times should be less than 25 nS.

2. On page 7 it is specified that the Serial Audio Ports are capable of receiving or transmitting data in slave mode at 27 MHz, if the necessary setup timing is observed. This is true as long as an additional condition is observed. There may be no more that 128 SCLK cycles per frame. This means a high speed burst clock can be used for SCLK, but a high speed continuous clock cannot.

3. Occasionally the CS8420 will enter an invalid mode. This can happen when an AES3 stream is first plugged into the part or when a source device interrupts the input stream. When this happens, two symptoms may be noticeable: notches occurring in the frequency response, and spurious tones being generated in response to some input frequencies. To avoid this problem, operate the part in software mode and use the micro-controller to monitor the UNLOCK bit in control register 16 (10 hex). When the part achieves lock, clear the RUN bit in register 4 and then set it again. This action clears the invalid state if it has occurred. No solution to this problem is available if the part is being used in hardware mode.

If there are any questions concerning this information,
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