19-0296; Rev 0; 8/94

EVALUATION KIT MANUAL AVAILABLE

MAXIM

500Msps, 8-Bit ADC with Track/Hold

General Description

The MAX101 ECL-compatible, 500Msps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 250MHz (Nyquist frequency). Dual monolithic converters, driven by the track/hold (T/H), operate on opposite clock edges (time interleaved). Designed with Maxim's proprietary advanced bipolar processes, the MAX101 contains a high-performance T/H amplifier and two quantizers in an 84-pin ceramic flat pack.

The innovative design of the internal T/H assures an exceptionally wide 1.2GHz input bandwidth and aperture delay uncertainty of less than 2ps, resulting in a high 7.0 effective bits at the Nyquist frequency. Special comparator output design and decoding circuitry reduce out-of-sequence code errors. The probability of erroneous codes due to metastable states is reduced to less than 1 error per 10^{15} clock cycles. And, unlike other ADCs that can have errors resulting in false full-scale or zero-scale outputs, the MAX101 keeps the error magnitude to less than 1LSB.

The analog input is designed for either differential or single-ended use with a ±270mV range. Sense pins for the reference input allow full-scale calibration of the input range or facilitate ratiometric use.

Phase adjustment is available to adjust the relative sampling of the converter halves for optimizing converter performance. Input clock phasing is also available for interleaving several MAX101s for higher effective sampling rates.

Features

- **500Msps Conversion Rate**
- **7.0 Effective Bits Typical at 250MHz**
- **1.2GHz Analog Input Bandwidth**
- **Less than ±1/2LSB INL**
- **50Ω Differential or Single-Ended Inputs**
- **±270mV Input Signal Range**
- **Ratiometric Reference Inputs**
- **Dual Latched Output Data Paths**
- **Low Error Rate, Less than 10^{-15} Metastable States**
- **84-Pin Ceramic Flat Pack**

Applications

High-Speed Digital Instrumentation

High-Speed Signal Processing

Medical Systems

Radar/Signal Processing

High-Energy Physics

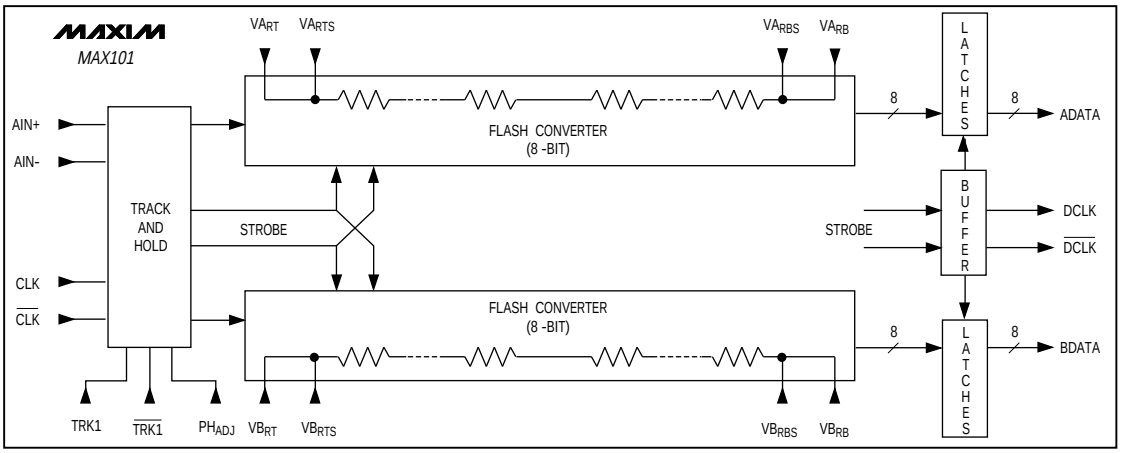
Communications

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX101CFR*	0°C to +70°C	84 Ceramic Flat Pack (with heatsink)

**Contact factory for 84-pin ceramic flat pack without heatsink.*

Functional Diagram



500Msps, 8-Bit ADC with Track/Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{CC} ..... 0V to +7V
- V_{EE} ..... -7V to 0V
- V_{CC} - V_{EE} ..... +12V

Analog Input Voltage ..... ±2V
Reference Voltage (VA_{RT}, VB_{RT}) ..... -0.3V to +1.5V
Reference Voltage (VA_{RB}, VB_{RB}) ..... -1.5V to +0.3V
Clock Input Voltage (V_{IH}, V_{IL}) ..... -2.3V to 0V
DIV10 Input Voltage (V_{IH}, V_{IL}) ..... V_{EE} to 0V
Output Current, ($I_O$max)
- T_J <100°C 14mA
- 100°C < T_J <125°C 12mA

Operating Temperature Range ..... 0°C to +70°C
Operating Junction Temperature (Note 2) ..... 0°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +250°C

Note 1: The digital control inputs are diode protected. However, limited protection is provided on other pins. Permanent damage may occur on unconnected units under high-energy electrostatic fields. Keep unused units in supplied conductive carrier or shunt the terminals together.

Note 2: Typical thermal resistance, junction-to-case $R_{\theta JC}$ = 5°C/W and thermal resistance, junction to ambient (MAX101CFR) $R_{\theta JA}$ =12°C/W, if 200 lineal ft/min airflow is provided. See *Package Information.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 100Ω to -2V, VA_{RT}, VB_{RT} = 1.02V, VA_{RB}, VB_{RB} = -1.02V, T_A = +25°C, unless otherwise noted. T_{MIN} to T_{MAX} = 0°C to +70°C. Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Integral Nonlinearity (Note 4)	INL	AData, BData	T_A = +25°C			±0.50	LSB
			T_A = T_{MIN} to T_{MAX}			±0.75	
Differential Nonlinearity	DNL	AData, BData, no missing codes	T_A = +25°C			±0.75	LSB
			T_A = T_{MIN} to T_{MAX}			±0.85	
DYNAMIC SPECIFICATIONS							
Effective Bits	ENOB	f_{CLK} = 500MHz, V_{IN} = 95% full scale (Note 5)	f_{AIN} = 10MHz		7.6		Bits
			f_{AIN} = 125MHz		7.1		
			f_{AIN} = 250MHz	6.7	7.0		
Signal-to-Noise Ratio	SNR	f_{AIN} = 125MHz, f_{CLK} = 500MHz, V_{IN} = 95% full scale (Note 6)			44.5		dB
Maximum Conversion Rate	f_{CLK}	(Note 7)		500			Msps
Analog Input Bandwidth	BW_{3dB}				1.2		GHz
Aperture Width	t_{AW}	Figure 4			270		ps
Aperture Jitter	t_{AJ}	Figure 4			2		ps
ANALOG INPUT							
Input Voltage Range	V_{IN}	AIN+ to AIN-, Table 2, T_A = T_{MIN} to T_{MAX}	Full scale	230		315	mV
			Zero scale	-305		-215	
Input Offset Voltage	V_{IO}	AIN+, AIN-, T_A = T_{MIN} to T_{MAX}		-17		32	mV
Least Significant Bit Size	LSB	T_A = T_{MIN} to T_{MAX}		1.8		2.5	mV
Input Resistance	R_I	AIN+, AIN-, to GND		49		51	Ω
Input Resistance Temperature Coefficient					0.008		Ω/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 100Ω to -2V, VA_{RT}, VB_{RT} = 1.02V, VA_{RB}, VB_{RB} = -1.02V, T_A = +25°C, unless otherwise noted. T_{MIN} to T_{MAX} = 0°C to +70°C. Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Reference String Resistance	R_{REF}	VA_{RT} to VA_{RB}		100		175	Ω
Reference String Resistance Temperature Coefficient					0.02		Ω/°C
LOGIC INPUTS							
Digital Input Low Voltage	V_{IL}	CLK, $\overline{CLK}$	$T_A = T_{MIN}$ to T_{MAX}			-1.50	V
Digital Input High Voltage	V_{IH}	CLK, $\overline{CLK}$	$T_A = T_{MIN}$ to T_{MAX}	-1.1			V
Digital Input High Current	I_{IH}	DIV10 = 0V	$T_A = T_{MIN}$ to T_{MAX}	1.1		3.1	mA
Input Bias Current	I_B	PH_{ADJ} = 0V	$T_A = T_{MIN}$ to T_{MAX}			40	µA
Clock Input Bias Current	I_{CLK}	CLK, $\overline{CLK}$ = -0.8V (no termination)	$T_A = T_{MIN}$ to T_{MAX}			50	µA
LOGIC OUTPUTS (Note 8)							
Digital Output Low Voltage	V_{OL}	AData, BData	T_A = +25°C	-1.95		-1.60	V
			$T_A = T_{MIN}$ to T_{MAX}	-1.95		-1.50	
		DCLK, $\overline{DCLK}$	T_A = +25°C	-1.3		-1.00	
			$T_A = T_{MIN}$ to T_{MAX}	-1.4		-0.9	
Digital Output High Voltage	V_{OH}	AData, BData, DCLK, $\overline{DCLK}$	T_A = +25°C	-1.02		-0.70	V
			$T_A = T_{MIN}$ to T_{MAX}	-1.10		-0.60	
Digital Output Voltage	$V_{OH} - V_{OL}$	DCLK, $\overline{DCLK}$	$T_A = T_{MIN}$ to T_{MAX}	275		445	mV
POWER REQUIREMENTS							
Positive Supply Current	I_{VCC}	V_{CC} = 5.0V	T_A = +25°C	550	765	1065	mA
			$T_A = T_{MIN}$ to T_{MAX}			1130	
Negative Supply Current	I_{VEE}	V_{EE} = -5.2V	T_A = +25°C	-935	-750	-525	mA
			$T_A = T_{MIN}$ to T_{MAX}	-975			
Common-Mode Rejection Ratio	CMRR	V_{INCM} = ±0.5V	$T_A = T_{MIN}$ to T_{MAX}	35			dB
Power-Supply Rejection Ratio	PSRR	V_{CC}(nom) = ±0.25V	$T_A = T_{MIN}$ to T_{MAX}	40			dB
		V_{EE}(nom) = ±0.25V		40			

500Msps, 8-Bit ADC with Track/Hold

TIMING CHARACTERISTICS

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 100Ω to -2V, VA_{RT}, VB_{RT} = 1.02V, VA_{RB}, VB_{RB} = -1.02V, T_A = +25°C, unless otherwise noted.)

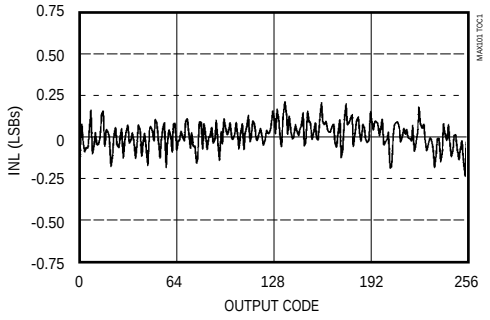
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Clock Pulse Width Low	t_{PWL}	CLK, $\overline{CLK}$		0.9		2.5	ns
Clock Pulse Width High	t_{PWH}	CLK, $\overline{CLK}$		0.9		2.5	ns
CLK to DCLK Propagation Delay	t_{PD1}	DIV10 = 0, Figures 1, 2		1.2	2.3	3.4	ns
DCLK to A/BData Propagation Delay	t_{PD2}	DIV10 = 0, Figures 1, 2		0.7	1.3	1.8	ns
Rise Time	t_R	20% to 80%	DCLK		400		ps
			DATA		850		
Fall Time	t_F	20% to 80%	DCLK		400		ps
			DATA		700		
Pipeline Delay (Latency)	t_{NPD}	See Figures 2, 3 and Table 1	Divide-by-1 mode	15		15	Clock Cycles

Note 3: All devices are 100% production tested at +25°C and are guaranteed by design for T_A = T_{MIN} to T_{MAX} as specified.
Note 4: Deviation from best-fit straight line. See *Integral Nonlinearity* section.
Note 5: See the *Signal-to-Noise Ratio and Effective Bits* section in the *Detailed Description of Specifications*.
Note 6: SNR calculated from effective bits performance using the following equation: SNR(dB) = 1.76 + 6.02 x effective bits.
Note 7: Clock pulse width minimum requirements t_{PWL} and t_{PWH} must be observed to achieve stated performance.
Note 8: Outputs terminated through 100Ω to -2.0V.

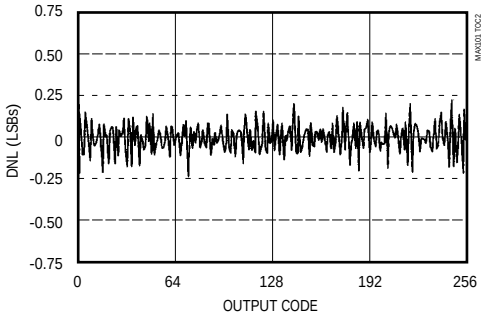
Typical Operating Characteristics

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 100Ω to -2V, VA_{RT}, VB_{RT} = 1.02V, VA_{RB}, VB_{RB} = -1.02V, T_A = +25°C, unless otherwise noted.)

INTEGRAL NONLINEARITY vs. OUTPUT CODE



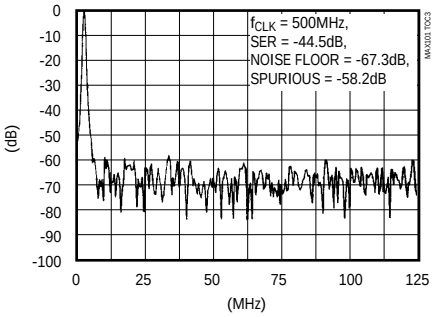
DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



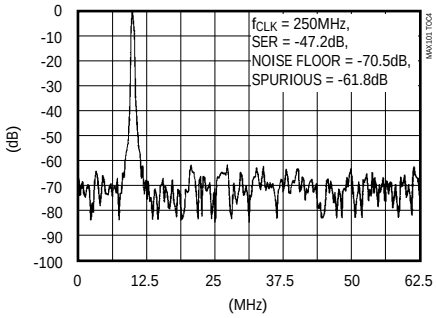
Typical Operating Characteristics (continued)

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 100Ω to -2V, VA_{RT}, VB_{RT} = 1.02V, VA_{RB}, VB_{RB} = -1.02V, T_A = +25°C, unless otherwise noted.)

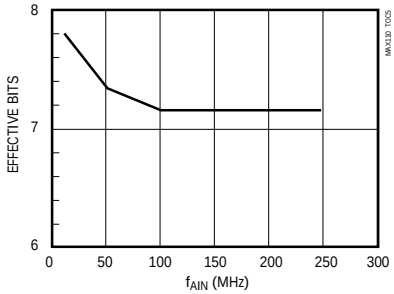
FFT PLOT
(f_{AIN} = 251.4462MHz)



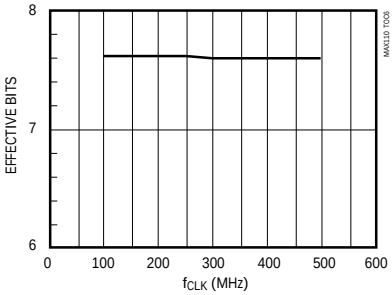
FFT PLOT
(f_{AIN} = 10.4462MHz)



EFFECTIVE BITS vs. ANALOG INPUT FREQUENCY (f_{AIN})
(f_{CLK} = 500MHz, V_{IN} = 95% FS)



EFFECTIVE BITS vs. CLOCK FREQUENCY (f_{CLK})
(f_{AIN} = 500MHz, V_{IN} = 95% FS)

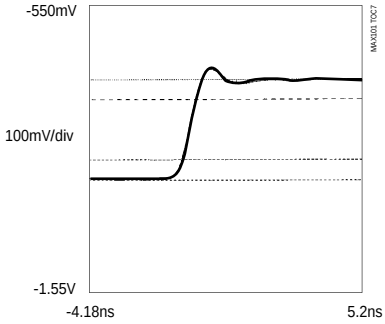


500Msps, 8-Bit ADC with Track/Hold

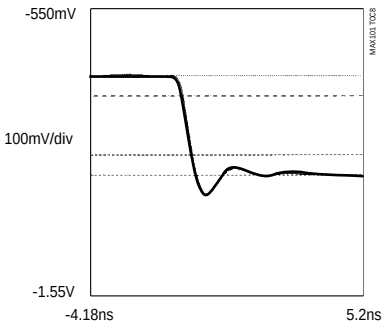
Typical Operating Characteristics (continued)

(V_{EE} = -5.2V, V_{CC} = +5V, R_L = 100Ω to -2V, VA_{RT}, VB_{RT} = 1.02V, VA_{RB}, VB_{RB} = -1.02V, T_A = +25°C, unless otherwise noted.)

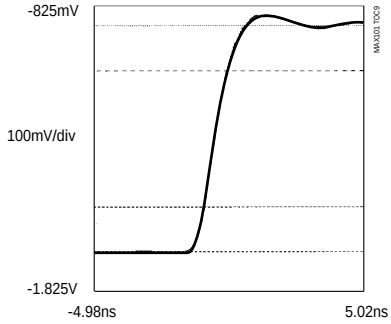
DATA CLOCK (DCLK) RISE TIME (526ps), DIV10 = OPEN



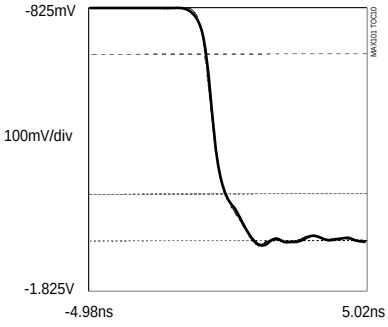
DATA CLOCK (DCLK) FALL TIME (352ps), DIV10 = OPEN



BDATA RISE TIME (855ps), DIV10 = OPEN



BDATA FALL TIME (714ps), DIV10 = OPEN



Pin Description

PIN	NAME	FUNCTION
1	PAD	Internal connection, leave open.
2, 62	CLK	Complementary Differential Clock Inputs. Can be driven from standard 10KH ECL with the following considerations: Internally, pins 2, 62 and 3, 61 are the ends of a 50Ω transmission line. Either end can be driven with the other end terminated with 50Ω to -2V. See *Typical Operating Circuit*.
3, 61	$\overline{CLK}$	
4, 7, 15, 18, 24, 27, 30, 34, 37, 40, 46, 49, 57, 60, 64, 67, 68, 70, 71, 74, 77, 78, 79, 82, 84	GND	Power-Supply Ground
5, 59	$\overline{TRK1}$	Phasing inputs (normally left open). See *Applications Information* section.
6, 58	TRK1	
8, 21, 43, 56, 81	VCC	Positive Power Supply, +5V ±5% nominal
9	VB_{RB}	"B" side negative reference voltage input (Note 9)
10	VB_{RBS}	"B" side negative reference voltage sense (Note 9)
11	TP4	Internal connection, leave pin open.
12	TP3	Internal connection, leave pin open.
13	VB_{RTS}	"B" side positive reference voltage sense (Note 9)
14	VB_{RT}	"B" side positive reference voltage input (Note 9)
16, 48, 63	N.C.	No Connect—no internal connection to these pins.
29	SUB	Circuit Substrate contact. This pin **must** be connected to V_{EE}.
31	$\overline{DCLK}$	Complementary Differential Clock Outputs. Used to synchronize following circuitry: Outputs A0–A7 are valid after DCLK's rising edge. B0–B7 output data are valid after DCLK's falling edge (see Figure 1 for output timing information).
33	DCLK	
32, 69, 80	VEE	Negative Power Supply, -5.2V ±5% nominal
35	DIV10	Divide by 10 mode. Leave open for normal operation. Selects test mode when grounded.
36, 38, 39, 41, 42, 44, 45, 47	A7–A0	AData and BData Outputs. A0 and B0 are the LSBs, and A7 and B7 are the MSBs. AData and BData outputs conform to ECL logic swings and drive 100Ω transmission lines. Terminate with 100Ω to -2V (120Ω for Tj > +100°C). See Figures 1–3.
28, 26, 25, 23, 22, 20, 19, 17	B7–B0	

Pin Description (continued)

PIN	NAME	FUNCTION
50	VA_{RT}	"A" side positive reference voltage input (Note 9)
51	VA_{RTS}	"A" side positive reference voltage sense (Note 9)
52	TP1	Internal connection, leave pin open.
53	TP2	Internal connection, leave pin open.
54	VA_{RBS}	"A" side negative reference voltage sense (Note 9)
55	VA_{RB}	"A" side negative reference voltage input (Note 9)
65	TP5	Internal connection, leave pin open.
66	TP6	Internal connection, leave pin open.
72, 73	AIN+	Analog Inputs, internally terminated with 50Ω to ground. Full-scale linear input range is approximately ±270mV. Drive AIN+ and AIN- differentially for best high-frequency performance.
75, 76	AIN-	
83	PH_{ADJ}	Phase adjustment for T/H. Normally connected to ground. A phase adjustment of approximately ±18ps can be made by varying this pin's bias point to optimize interleaving between sides A and B (Note 10).

Note 9: VA_{RT}, VA_{RB}, VB_{RT}, and VB_{RB} should be adjusted separately from a well bypassed reference circuit to ensure proper amplitude and offset matching. The sense connections to each of these terminals allows precision setting of the reference voltage. The reference ladder is similar for both converter halves (check electrical section for values). Any noise on these terminals will severely reduce overall performance.

Note 10: Good results are obtained by connecting the PH_{ADJ} input to ground. Improve performance by applying a voltage between ±1.25V to this input. The time that the "A" T/H bridge samples relative to the time that the "B" T/H bridge samples can be varied through a ±18ps range.

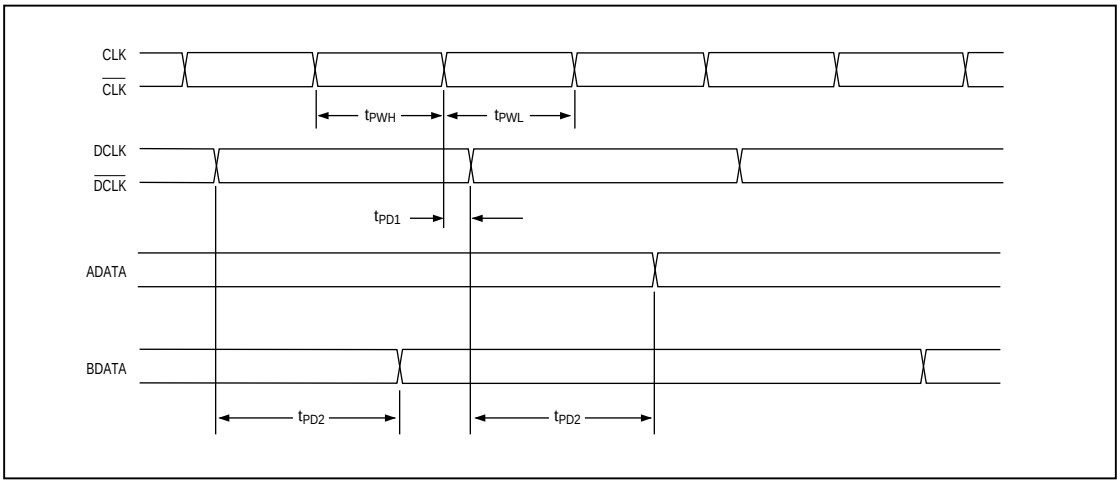


Figure 1. Output Timing, Normal Mode, DIV10 = OPEN

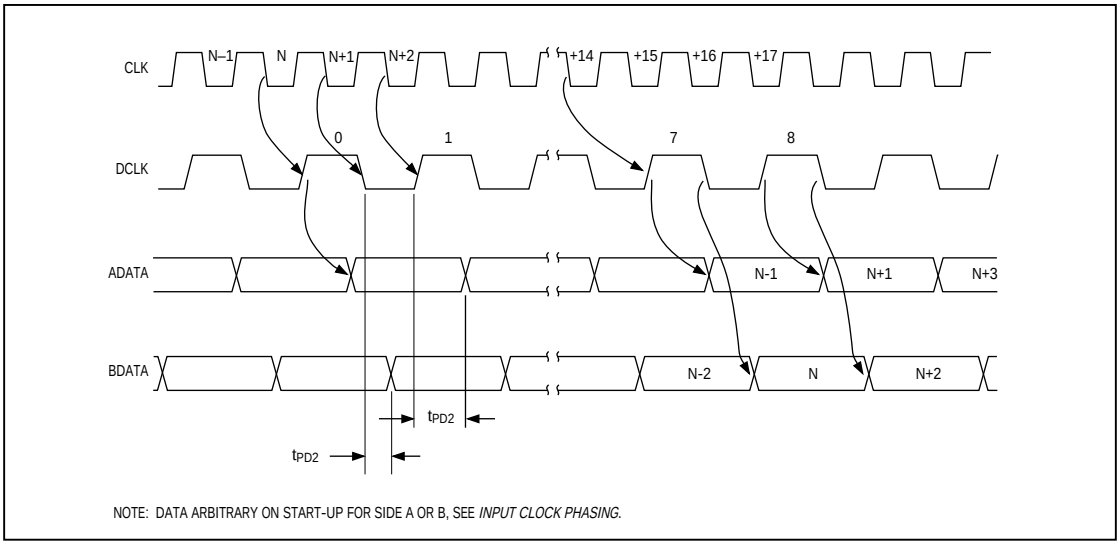


Figure 2. Output Timing, Clock to Data, Normal Mode DIV10 = OPEN

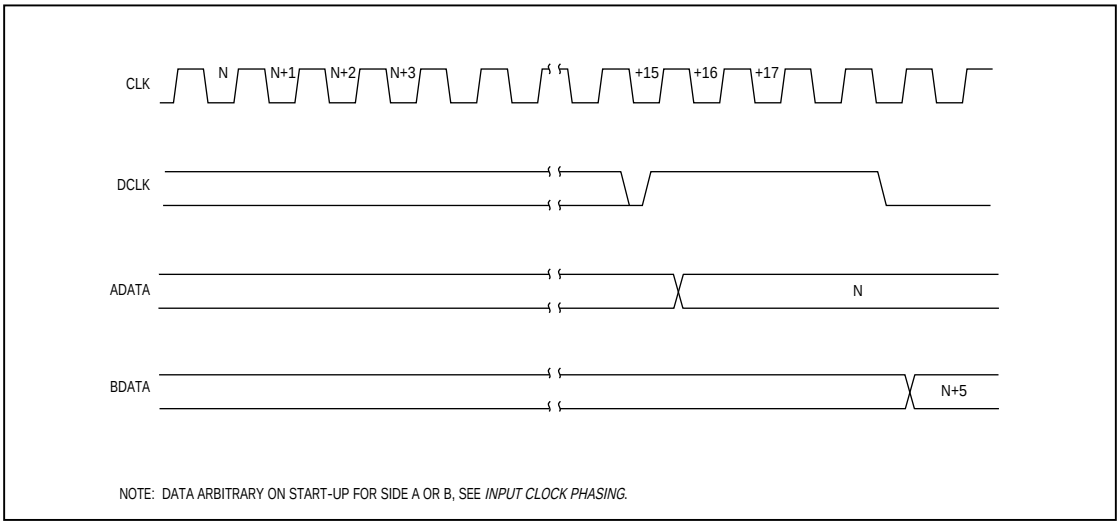


Figure 3. Output Timing, Test Mode (DIV10 = GND)

Definitions of Specifications

Signal-to Noise Ratio and Effective Bits

Signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other analog-to-digital (A/D) output signals. The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of effective bits of resolution. Therefore, a perfect 8-bit ADC can do no better than 50dB. The FFT plots in the *Typical Operating Characteristics* show the output level in various spectral bands.

Effective bits is calculated from a digital record taken from the ADC under test. The quantization error of the ideal converter equals the total error of the device. In addition to ideal quantization error, other sources of error include all DC and AC nonlinearities, clock and aperture jitter, missing output codes, and noise. Noise on references and supplies also degrades effective bits performance.

The ADC's input is a sine wave filtered with an anti-aliasing filter to remove any harmonic content. The digital record taken from this signal is compared against a mathematically generated sine wave. DC offsets, phase, and amplitudes of the mathematical model are adjusted until a best-fit sine wave is found. After subtracting this sine wave from the digital record, the residual error remains. The rms value of the error is applied in the following equation to yield the ADC's effective bits.

$$\text{Effective bits} = N - \log_2 \left(\frac{\text{measured rms error}}{\text{ideal rms error}} \right)$$

where N is the resolution of the converter. In this case, N = 8.

The worst-case error for any device will be at the converter's maximum clock rate with the analog input near the Nyquist rate (one-half the input clock rate).

Aperture Width and Jitter

Aperture width is the time the T/H circuit takes to disconnect the hold capacitor from the input circuit (i.e., to turn off the sampling bridge and put the T/H in hold mode). Aperture jitter is the sample-to-sample variation in aperture delay (Figure 4).

Error Rates

Errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for many typical converters can be incorrect, including false full- or zero-scale output. The MAX101's unique design reduces the magnitude of this type of error to 1LSB, and reduces the probability of the error occurring to less than one in every 10^{15} clock cycles. If the MAX101 were operated at 500MHz, 24 hours a day, this would translate to less than one metastable state error every 46 days.

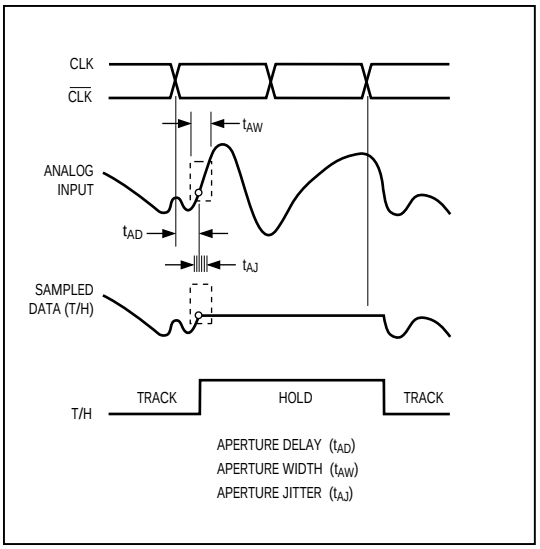


Figure 4. T/H Aperture Timing

Integral Nonlinearity

Integral nonlinearity is the deviation of the transfer function from a reference line measured in fractions of 1LSB using a "best straight line" determined by a least square curve fit.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured LSB step and an ideal LSB step size between adjacent code transitions. DNL is expressed in LSBs and is calculated using the following equation:

$$\text{DNL(LSB)} = \frac{[V_{MEAS} - (V_{MEAS - 1})] - \text{LSB}}{\text{LSB}}$$

where $V_{MEAS - 1}$ is the measured value of the previous code.

A DNL specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Detailed Description

Converter Operation

The parallel or "flash" architecture used by the MAX101 provides the fastest multibit conversion of all common integrated ADC designs. The basic element of a flash, as with all other ADC architectures, is the comparator, which has a positive input, a negative input, and an output. If the voltage at the positive input is higher than the negative input (connected to a reference), the output will be high. If the positive input voltage is lower than the reference, the output will be low. A typical n-bit flash consists of 2^n - 1 comparators with negative inputs evenly spaced at 1LSB increments from the bottom to the top of the reference ladder. For n = 8, there are 255 comparators.

For any input voltage, all the comparators with negative inputs connected to the reference ladder below the input voltage will have outputs of 1 and all comparators with negative inputs above the input voltage will have outputs of 0. Decode logic is provided to convert this information into a parallel n-bit digital word (the output) corresponding to the number of LSBs (minus 1) that the input voltage is above the bottom of the ladder.

The comparators contain latch circuitry and are clocked. This allows the comparators to function as described previously when, for example, clock is low. When clock goes high (samples) the comparator will latch and hold its state until the clock goes low again.

The MAX101 uses a monolithic dual interleaved parallel quantizer chip with two separate 8-bit converters. These converters deliver results to the A and B output latches on alternate negative edges of the input clock.

Track/Hold

As with all ADCs, if the input waveform is changing rapidly during the conversion the effective bits and SNR will decrease. The MAX101 has an internal track/hold (T/H) that increases attainable effective bits performance and allows more accurate capture of analog data at high conversion rates.

The internal T/H circuit provides two important circuit functions for the MAX101:

1) Its nominal voltage gain of 4 reduces the input driving signal to ±270mV differential (assuming a ±1.02V reference).

2) It provides a differential 50Ω input that allows easy interface to the MAX101.

Table 1. Output Mode Control

DIV10	DCLK* (MHz)	MODE	DESCRIPTION
OPEN	250	Normal Divide by 2	AData and BData valid on opposite DCLK edges (AData on rise, BData on fall).
GND	50	Test Divide by 10	AData and BData valid on opposite DCLK edges (AData on rise, BData on fall). Data sampled at input CLK rate but 4 out of every 5 samples discarded.

* Input clocks (CLK, $\overline{CLK}$) = 500MHz for all above combinations. In all modes, the output clock DCLK will be a 50% duty cycle signal.

Data Flow

The MAX101's internal T/H amplifier samples the analog input voltage for the ADC to convert. The T/H is split into two sections that operate on alternate negative clock edges. The input clock, CLK, is conditioned by the T/H and fed to the A/D section. The output clock, DCLK, used for output data timing, will be divided by 2 or 10 from the input clock, CLK (Table 1). This would result in an output data rate of 250Mbps on each output port in normal mode and 50Mbps in test mode. The differential inputs, AIN+ and AIN-, are tracked continuously between data samples. When a negative strobe edge is sensed, one-half of the T/H goes into the hold mode (Figure 4). When the strobe is low, the just-acquired sample is presented to the ADC's input comparators. Internal processing of the sampled data takes an additional 15 clock cycles before it is available at the outputs, AData and BData. See Figures 1–3 for timing.

Applications Information

Analog Input Ranges

Although the normal operating range is ±270mV, the MAX101 can be operated with up to ±500mV on each input with respect to ground. This extended input level includes the analog signal and any DC common-mode voltage.

To obtain full-scale digital output with differential input drive, a nominal +270mV must be applied between AIN+ and AIN-. That is, AIN+ = +135mV and AIN- = -135mV (with no DC offset). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero-scale digital output code, with differential -270mV drive, occurs when AIN+ = -135mV and AIN- = +135mV. Table 2 shows how the output of the converter stays at all ones (full scale) when over-ranged or all zeros (zero scale) when under-ranged.

Table 2. Input Voltage Range

INPUT	AIN+ (mV)	AIN- (mV)	OUTPUT CODE	MSB to LSB
Differential	+135	-135	1 1 1 1 1 1 1 1	full scale
	0	0	1 0 0 0 0 0 0 0	mid scale
	-135	+135	0 0 0 0 0 0 0 0	zero scale
Single Ended	+270	0	1 1 1 1 1 1 1 1	full scale
	0	0	1 0 0 0 0 0 0 0	mid scale
	-270	0	0 0 0 0 0 0 0 0	zero scale

* An offset V_{IO}, as specified in the DC electrical paramters, will be present at the input. Compensate for this offset by adjusting the reference voltage. Offsets may be different between side A and side B.

For single-ended operation:

1) Apply a DC offset to one of the analog inputs, or leave one input open. (Both AIN+ and AIN- are terminated internally with 50Ω to analog ground.)
2) Drive the other input with a ±270mV + offset to obtain either full- or zero-scale digital output. If a DC common-mode offset is used, the total voltage swing allowed is ±500mV (analog signal plus offset with respect to ground).

Reference

The ADC's reference resistor is a Kelvin-sensed, resistor string that sets the ADC's LSB size and dynamic operating range. Normally, the top and bottom of this string are driven with an external buffer amplifier. It will need to supply approximately 21mA due to the 100Ω minimum resistor string impedance. A ±1.02V reference voltage is normally applied to inputs VA_{RT}, VB_{RT}, VA_{RB}, and VB_{RB}. This reference voltage can be adjusted up to ±1.2V to accommodate extended input requirements (accuracy specifications are guaranteed with ±1.02V references). The reference inputs VA_{RTS}, VA_{RBS}, VB_{RTS}, and VB_{RBS} allow Kelvin sensing of the applied voltages to increase precision.

An RC network at the ADC's reference terminals is needed for best performance. This network consists of a 33Ω resistor connected in series with the buffer output that drives the reference. A 0.47µF capacitor must be connected near the resistor at the buffer's output (see *Typical Operating Circuit*). This resistor and capacitor combination should be located within 0.5 inches of the MAX101 package. Any noise on these pins will directly affect the code uncertainty and degrade the ADC's effective bits performance.

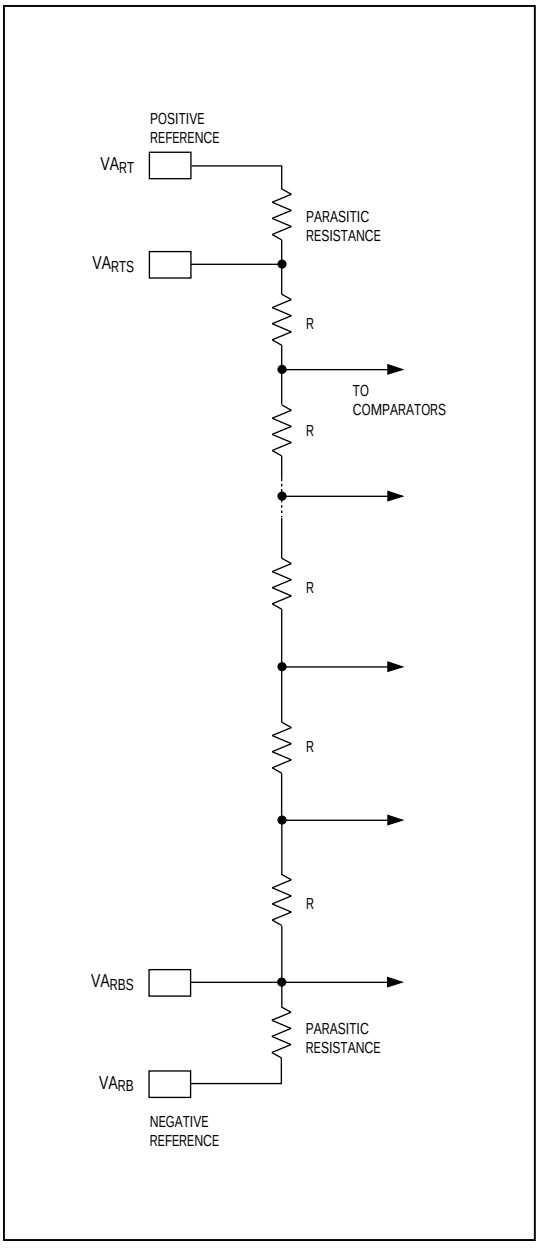


Figure 5. Reference Ladder

CLK and DCLK

All input and output clock signals are differential. The input clocks, CLK and $\overline{CLK}$, are the primary timing signals for the MAX101. CLK (pins 2, 62) and $\overline{CLK}$ (pins 3, 61) are fed to the internal circuitry through an internal 50Ω transmission line. One set of CLK, $\overline{CLK}$ inputs should be driven and the other pair terminated by 50Ω to -2V. Either set of inputs can be used as the driven inputs (input lines are balanced) for easy circuit connection. A minimum pulse width (t_{PWL}) is required for CLK and $\overline{CLK}$ (Figures 1–3).

For best performance and consistent results, use a low-phase-jitter clock source for CLK and $\overline{CLK}$. Phase jitter larger than 2ps from the input clock source reduces the converter's effective bits performance and causes inconsistent results. The clock supplied to the MAX101 is internally divided by two, reshaped, and buffered. This divided clock becomes the internal signal used as strobes for the converters.

DCLK and $\overline{DCLK}$ are output clock signals derived from the input clocks and are used for external timing of the AData and BData outputs. (AData is valid after the rising edge of DCLK and BData is valid after the falling edge.) They are fixed at one-half the rate of the input clocks in normal mode (Table 1). The MAX101 is characterized to work with 500MHz maximum input clock frequencies. See *Typical Operating Circuit*.

Output Mode Control (DIV10)

When DIV10 is grounded, it enables the test mode, where the input incoming clock is divided by ten. This reduces the output data and clock rates by a factor of 5, allowing the output clock duty cycle to remain at 50%. The clock to output phasing remains the same and four out of every five sampled input values are discarded.

When left open, this input (DIV10) is pulled low by internal circuitry and the converter functions in its normal mode.

Layout, Grounding, and Power Supplies

A +5V ±5% supply as well as a -5.2V ±5% supply is needed for proper operation. Bypass the VEE and VCC supply pins to GND with high-quality 0.1µF and 0.001µF ceramic capacitors located as close to the package as possible. Connect all ground pins to a ground plane to optimize noise immunity and highest device accuracy.

Phase Adjust

This control pin affects the point in time that one-half of the converter samples the input signal relative to the other half. PH_{ADJ} is normally connected to ground (0V), but can be adjusted over a ±1.25V range that typically provides a ±18ps adjustment between the "A" side T/H bridge strobe and the "B" side T/H bridge strobe.

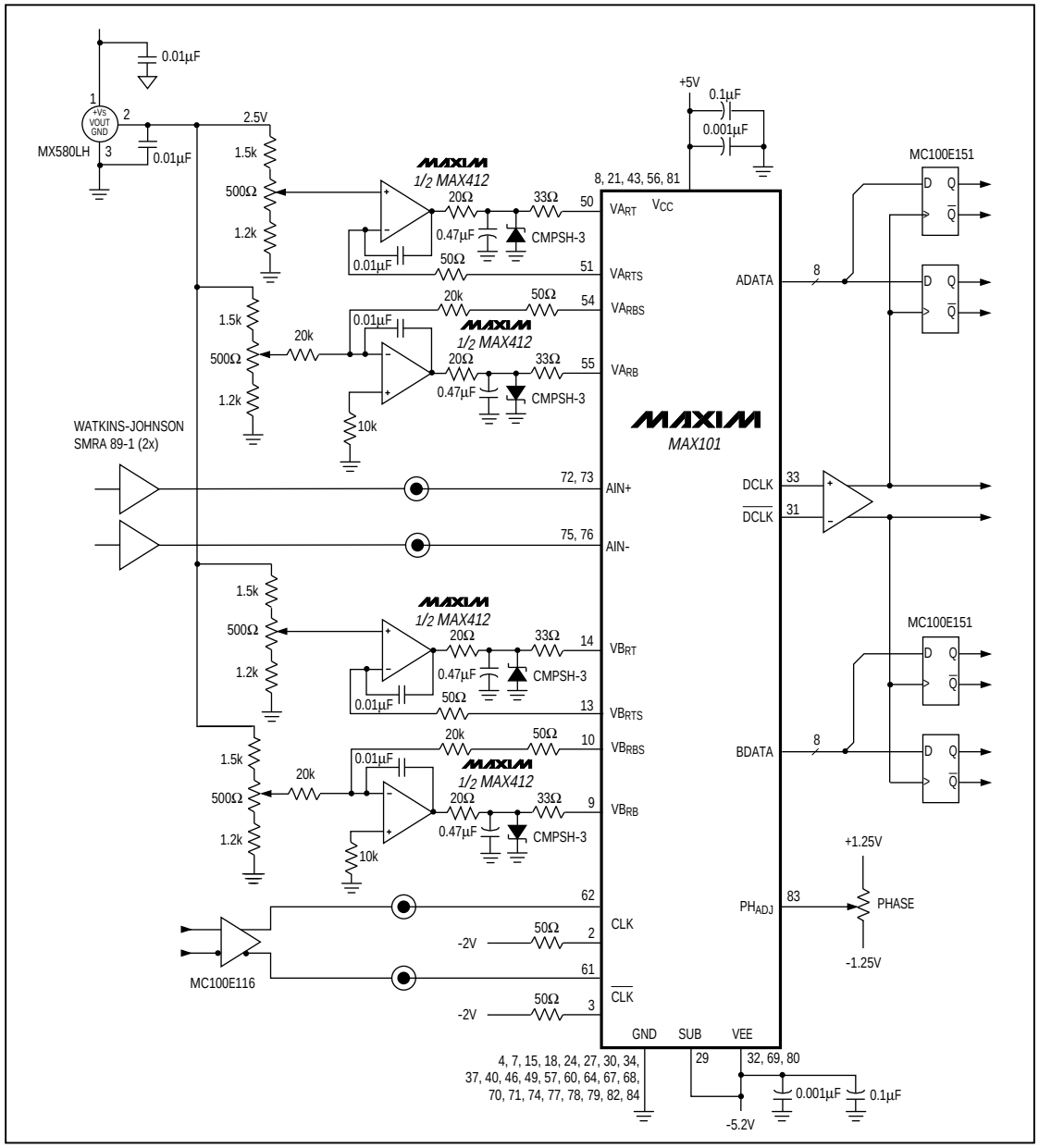
Input Clock Phasing (TRK1, $\overline{TRK1}$)

At power-up, the clock edge from which AData and BData are synchronized is undetermined. The converter can work from a specific input clock edge, as described in the following paragraph.

TRK1 and $\overline{TRK1}$ are differential inputs that are used in addition to the normal input clock (CLK) to set data phasing. A signal at one-half the input clock rate with the proper setup and hold times (setup and hold typically 300ps) is applied to these inputs. Choose AData by applying a logic "1" to TRK1 ("0" to $\overline{TRK1}$) before CLK's negative transition. Choose BData by applying a logic "0" at CLK's negative edge ("1" to $\overline{TRK1}$). In this manner, several MAX101s can be interleaved to obtain faster effective sampling rates. Voltages at the TRK1 input between ±50mV are interpreted as logic "1" and voltages between -350mV and -500mV are interpreted as logic "0".

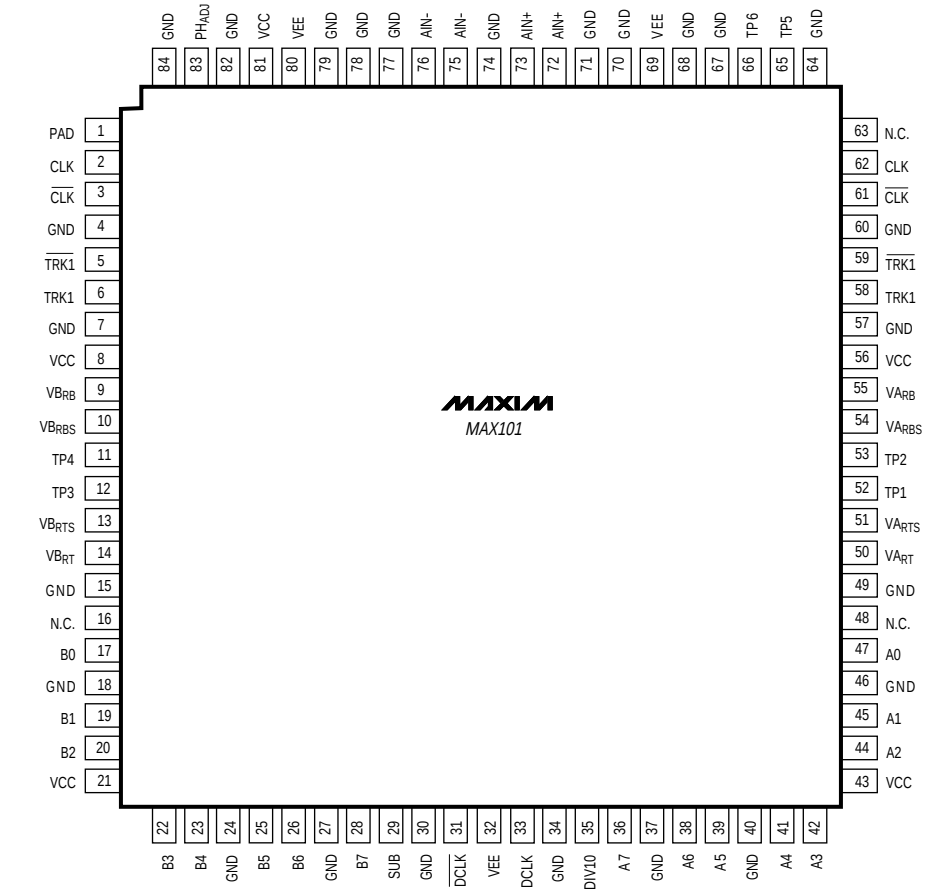
500Msps, 8-Bit ADC with Track/Hold

Typical Operating Circuit

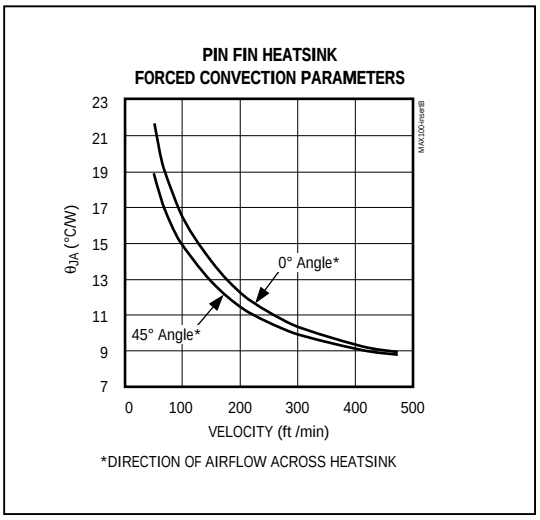


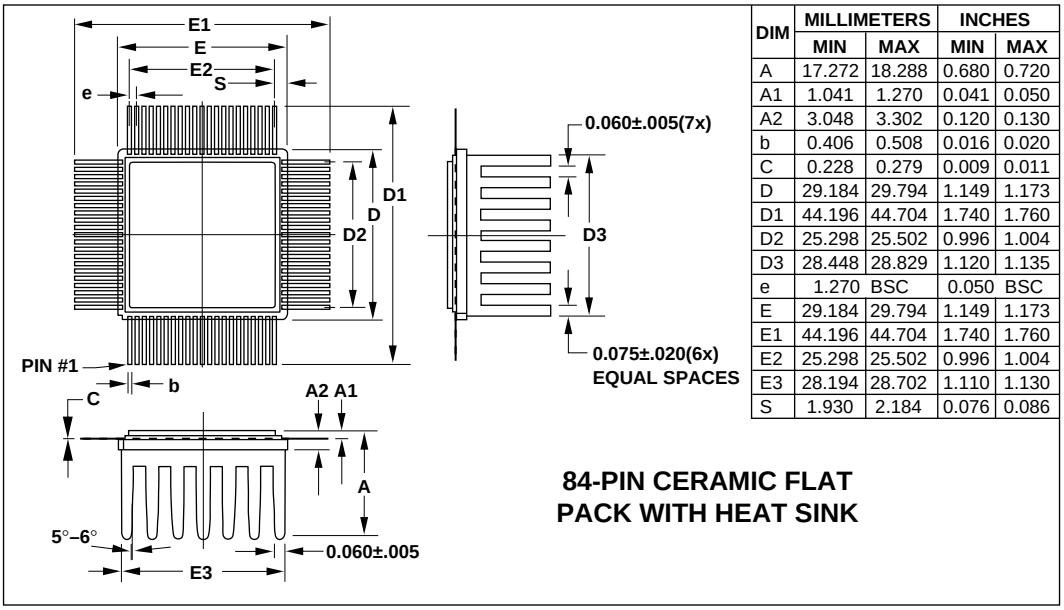
Pin Configuration

TOP VIEW



Ceramic Flat Pack





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	17.272	18.288	0.680	0.720
A1	1.041	1.270	0.041	0.050
A2	3.048	3.302	0.120	0.130
b	0.406	0.508	0.016	0.020
C	0.228	0.279	0.009	0.011
D	29.184	29.794	1.149	1.173
D1	44.196	44.704	1.740	1.760
D2	25.298	25.502	0.996	1.004
D3	28.448	28.829	1.120	1.135
e	1.270	BSC	0.050	BSC
E	29.184	29.794	1.149	1.173
E1	44.196	44.704	1.740	1.760
E2	25.298	25.502	0.996	1.004
E3	28.194	28.702	1.110	1.130
S	1.930	2.184	0.076	0.086

84-PIN CERAMIC FLAT PACK WITH HEAT SINK