MOTOROLA
Semiconductor Products Sector

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PowerPC™

Advance Information

XPC750P RISC Microprocessor Hardware Specifications

This document describes pertinent physical characteristics of the XPC750P, a process-remapped version of the MPC750. This part has been previously described jointly with the MPC750 in the MPC750 RISC Microprocessor Hardware Specifications (MPC750EC/D Rev 1); however, it is now being described separately because the MPC750 is available over much wider operating conditions (including extended temperature conditions). The XPC750P described herein will only be available at the restricted operating conditions described in Table 3.

This document describes the XPC750P; however, unless otherwise noted, all information here applies also to the XPC740P. The XPC750P and XPC740P are implementations of the PowerPC™ family of reduced instruction set computing (RISC) microprocessors. For functional characteristics of the processor, refer to the *MPC750 RISC Microprocessor User's Manual*.

The MPC750 family has been implemented in several semiconductor fabrication processes. Different processes require different supply voltages and may have other electrical differences. The implementations are, in general, functionally equivalent but may represent different revisions of the design with regard to errata. A companion document, called a Part Number Specification, is created to describe errata or specification variances that are unique to a particular revision. Part Number Specifications, if applicable, are available at the same website, http://www.mot.com/PowerPC, where this document is found.

As a designator to distinguish between MPC750 implementations in various processes, a suffix is added to the MPC750 part number as shown in Table 1.

Table 1. MPC750 Microprocessors from Motorola

Part Number	Process	Core Voltage	I/O Voltage	5-Volt Tolerant
MPC750A, MPC740A	0.29 µm CMOS, 5LM	2.6 V	3.3 V	No
XPC750P, XPC740P	0.19 µm CMOS, 5LM	1.9 V	3.3 V	No

This document will describe only the XPC750P implementation with its unique supply voltages, package (decoupling capacitors are added on the package), and unique AC timing specifications. Major subsections of this document which are identical to the MPC750 Hardware Specification are not repeated here to reduce confusion. Please refer to the MPC750 document for those unchanged subsections.

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To locate any published errata or updates for this document, refer to the website at http://www.mot.com/PowerPC/.

1.1 Overview

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.2 Features

This section is unchanged from the MPC750 Hardware Specification except as relates to supply voltage; refer to that document for feature information and to this document for applicable supply voltage.

1.3 General Parameters

The following list provides a summary of the general parameters of the XPC750P:

Technology	0.18 µm CMOS, five-layer metal
Die size	7.56 mm x 8.79 mm (67 mm^2)
Transistor count	6.35 million
Logic design	Fully-static
Packages	XPC740P: Surface mount 255 ceramic ball grid array (CBGA) without L2 interface
	XPC750P: Surface mount 360 ceramic ball grid array (CBGA) with L2 interface
Core power supply:	1.9V ± 100 mV @300 and 333MHz
	2.05V ± 50mV @366 and 400MHz
I/O power supply	3.3V ± 5% V dc

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the XPC750P.

1.4.1 DC Electrical Characteristics

The tables in this section describe the XPC750P DC electrical characteristics. Table 2 provides the absolute maximum ratings.

Table 2. Absolute Maximum Ratings

Characteristic	Symbol	XPC750P Value	Unit	Notes
Core supply voltage	Vdd	–0.3 to 2.5	V	4
PLL supply voltage	AVdd	–0.3 to 2.5	V	4
L2 DLL supply voltage	L2AVdd	–0.3 to 2.5	V	4
60x bus supply voltage	OVdd	–0.3 to 3.6	V	3,5
L2 bus supply voltage	L2OVdd	–0.3 to 3.6	V	3,5
Input voltage	V_{in}	–0.3 to 3.6	V	2
Storage temperature range	T_{stg}	–55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in Figure 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OVdd/L2OVdd by more than 0.3V at any time including during power-on reset.
3. **Caution**: OVdd/L2OVdd must not exceed Vdd/AVdd by more than 2.0V at any time including during power-on reset.
4. **Caution**: Vdd/AVdd/L2AVdd must not exceed OVdd/L2OVdd by more than 0.4V at any time including during power-on reset.
5. V_{in} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 1.

Figure 1 shows the permitted undershoot and overshoot voltage on the XPC750P.

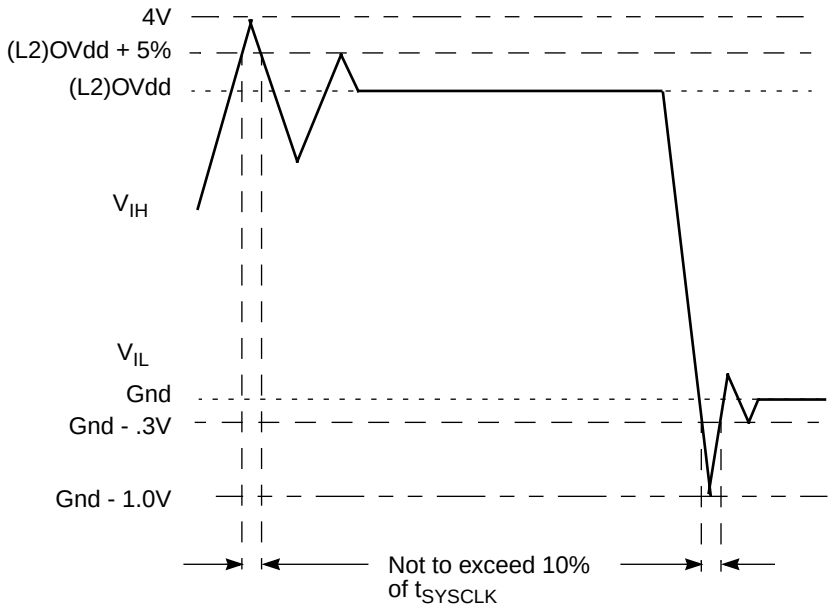


Figure 1. Overshoot/Undershoot Voltage

Table 3 provides the recommended operating conditions for the XPC750P.

Table 3. Recommended Operating Conditions

Characteristic	Symbol	300, 333MHz	366MHz	400MHz	Unit
Core supply voltage	Vdd	1.9 ± 100mv	2.05 ± 50mv	2.05 ± 50mv	V
PLL supply voltage	AVdd	1.9 ± 100mv	2.05 ± 50mv	2.05 ± 50mv	V
L2 DLL supply voltage	L2AVdd	1.9 ± 100mv	2.05 ± 50mv	2.05 ± 50mv	V
60x bus supply voltage	OVdd	3.3 ± 165mv	3.3 ± 165mv	3.3 ± 165mv	V
L2 bus supply voltage	L2OVdd	3.3 ± 165mv	3.3 ± 165mv	3.3 ± 165mv	V
Input voltage	V_{in}	GND to OVdd	GND to OVdd	GND to OVdd	V
Die-junction temperature	T_j	0 to 105	0 to 105	0 to 65	°C

Note: These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 4 provides the package thermal characteristics for the XPC750P.

Table 4. Package Thermal Characteristics

Characteristic	Symbol	Value	Rating
CBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	0.03	°C/W
CBGA package thermal resistance, die junction-to-lead thermal resistance (typical)	θ_{JB}	3.8	°C/W

Note: Refer to Section 1.8, “System Design Information,” for more details about thermal management.

The XPC750P incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). See the *MPC750 RISC Microprocessor User's Manual* for more information on the use of this feature. Specifications for the thermal sensor portion of the TAU are found in Table 5.

Table 5. Thermal Sensor Specifications

At recommended operating conditions (See Table 3.)

Characteristic	Min	Max	Unit	Notes
Temperature range	0	127	°C	1
Comparator settling time	20	—	µs	2
Resolution	4	—	°C	3

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but it must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Motorola Application Note AN1800/D, "Programming the Thermal Assist Unit in the MPC750 Microprocessor".
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Table 6 provides the DC electrical characteristics for the XPC750P.

Table 6. DC Electrical Specifications

At recommended operating conditions (See Table 3.)

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	V_{IH}	2	OVdd + 0.3	V	2,3
Input low voltage (all inputs except SYSCLK)	V_{IL}	-0.3	0.8	V	
SYSCLK input high voltage	CV_{IH}	2.4	OVdd + 0.3	V	2
SYSCLK input low voltage	CV_{IL}	-0.3	0.4	V	
Input leakage current, V_{in} = OVdd	I_{in}	—	30	µA	2,3
Hi-Z (off-state) leakage current, V_{in} = OVdd	I_{TSI}	—	30	µA	2,3,5
Output high voltage, I_{OH} = -6 mA	V_{OH}	2.4	—	V	
Output low voltage, I_{OL} = 6 mA	V_{OL}	—	0.4	V	
Capacitance, V_{in} = 0 V, f = 1 MHz	C_{in}	—	5.0	pF	3,4

Notes:
1. Nominal voltages; See Figure 3 for recommended operating conditions.
2. For 60x bus signals, the reference is OVdd while L2OVdd is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OVdd and Vdd, or both OVdd and Vdd must vary in the same direction (for example, both OVdd and Vdd vary by either +5% or -5%).

Table 7 provides the power consumption for the XPC750P.

Table 7. Power Consumption for XPC750P

	Processor (CPU) Frequency				Unit	Notes
	300 MHz	333 MHz	366MHz	400 MHz		
Full-On Mode						
Typical	3.4	4.2	4.6	5.0	W	1, 3, 4
Maximum	5.5	6.0	6.6	7.2	W	1, 2, 4
Doze Mode						
Maximum	2.5	2.65	2.85	3.0	W	1, 2
Nap Mode						
Maximum	700	4733	766	800	mW	1, 2
Sleep Mode						
Maximum	650	665	685	700	mW	1, 2
Sleep Mode—PLL and DLL Disabled						
Typical	450	450	450	450	mW	1, 3
Maximum	600	600	600	600	mW	1, 2

Notes:

1. These values apply for all valid 60x bus and L2 bus ratios. The values do not include I/O Supply Power (OVdd and L2OVdd) or PLL/DLL supply power (AVdd and L2AVdd). OVdd and L2OVdd power is system dependent, but is typically <10% of Vdd power. Worst case power consumption for AVdd = 15 mW and L2AVdd = 15 mW.
2. Maximum power is measured at Vdd = 2.0V.
3. Typical power is an average value measured at Vdd = AVdd = L2AVdd = 1.9V, OVdd = L2OVdd = 3.3V in a system executing typical applications and benchmark sequences.
4. Full-On mode is measured using worst-case instruction sequence.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the XPC750P. After fabrication, parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency. See Section 1.10, “Ordering Information.”

1.4.2.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications as defined in Figure 2.

Table 8. Clock AC Timing Specifications

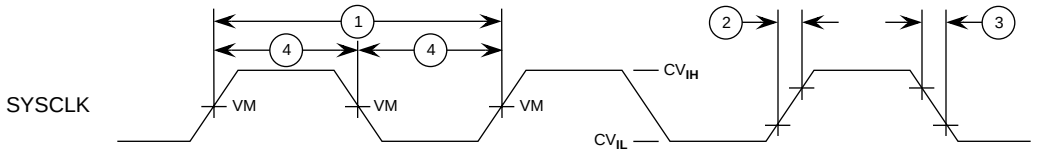
At recommended operating conditions (See Table 3.)

Num	Characteristic	300 MHz		333 MHz		366 MHz		400 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
	Processor frequency	250	300	250	333	250	366	250	400	MHz	
	VCO frequency	500	600	500	666	500	733	500	800	MHz	
	SYSCLK frequency	33	100	33	100	33	100	33	100	MHz	1
1	SYSCLK cycle time	10	30	10	30	10	30	10	30	ns	
2, 3	SYSCLK rise and fall time	—	2	—	2	—	2	—	2	ns	2
4	SYSCLK duty cycle measured at 1.4V	40	60	40	60	40	60	40	60	%	3
	SYSCLK jitter	—	±150	—	±150	—	±150	—	±150	ps	4
	Internal PLL relock time	—	100	—	100	—	100	—	100	µs	5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8.1, “PLL Configuration,” for valid PLL_CFG[0–3] settings
2. Rise and fall times for the SYSCLK input are measured from 0.4 to 2.4V.
3. Timing is guaranteed by design and characterization.
4. The total input jitter (short term and long term combined) must be under ±150 ps.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 2 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4V)

Figure 2. SYSCLK Input Timing Diagram

1.4.2.2 60x Bus Input AC Specifications

Table 9 provides the 60x bus input AC timing specifications for the XPC750P as defined in Figure 3 and Figure 4. Input timing specifications for the L2 bus are provided in Section 1.4.2.5, “L2 Bus Input AC Specifications.

Table 9. 60x Bus Input AC Timing Specifications[1]

At recommended operating conditions (See Table 3.)

Num	Characteristic	300,333,366,400 MHz		Unit	Notes
		Min	Max		
10a	Address/Data/Transfer Attribute Inputs Valid to SYSCLK (Input Setup)	2.5	—	ns	2
10b	All Other Inputs Valid to SYSCLK (Input Setup)	2.5	—	ns	3
10c	Mode select input setup to $\overline{\text{HRESET}}$ ($\overline{\text{DRTRY}}$, $\overline{\text{TLBISYNC}}$)	8	—	t_{sysclk}	4,5,6,7
11a	SYSCLK to Address/Data/Transfer Attribute Inputs Invalid (Input Hold)	0	—	ns	2
11b	SYSCLK to All Other Inputs Invalid (Input Hold)	0	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select input hold ($\overline{\text{DRTRY}}$, $\overline{\text{TLBISYNC}}$)	0	—	ns	4,6,7

Notes:

1. All input specifications are measured from the TTL level (0.8 to 2.0V) of the signal in question to the 1.4V of the rising edge of the input SYSCLK. Input and output timings are measured at the pin.
2. Address/Data/Transfer Attribute inputs are composed of the following—A[0–31], AP[0–3], TT[0–4], $\overline{\text{TBST}}$, TSIZ[0–2], $\overline{\text{GBL}}$, DH[0–31], DL[0–31], DP[0–7].
3. All other signal inputs are composed of the following—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 4.).
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Guaranteed by design and characterization.
7. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.

Figure 3 provides the input timing diagram for the XPC750P.

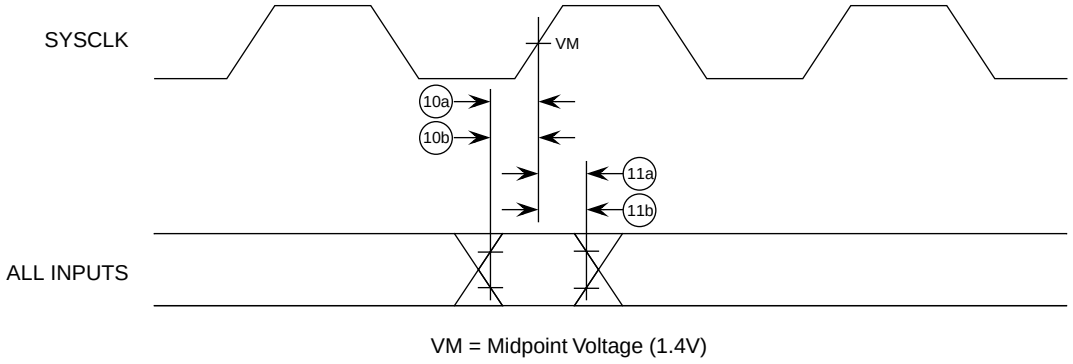


Figure 3. Input Timing Diagram

Figure 4 provides the mode select input timing diagram for the XPC750P.

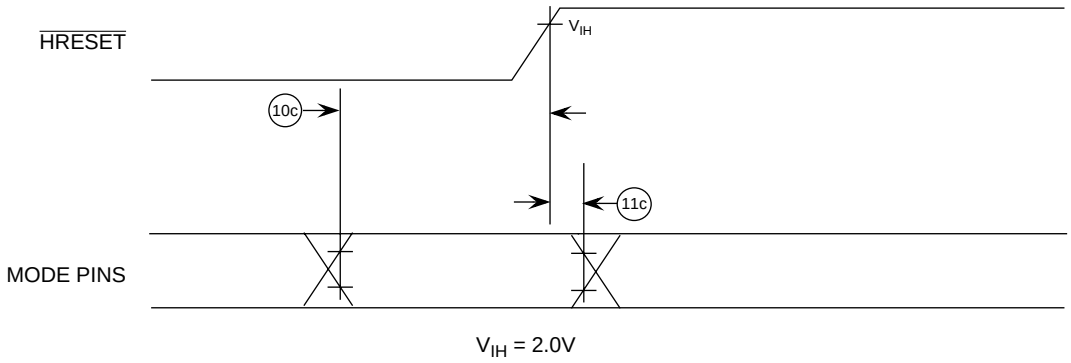


Figure 4. Mode Select Input Timing Diagram

1.4.2.3 60x Bus Output AC Specifications

Table 10 provides the 60x bus output AC timing specifications for the XPC750P as defined in Figure 5. Output timing specifications for the L2 bus are provided in Section 1.4.2.6, “L2 Bus Output AC Specifications.”

Table 10. 60x Bus Output AC Timing Specifications[1]

At recommended operating conditions (See Table 3.), C_L = 50 pF[2]

Num	Characteristic	300,333,366,400 MHz		Unit	Notes
		Min	Max		
12	SYSCLK to Output Driven (Output Enable Time)	0.5	—	ns	
13	SYSCLK to Output Valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	5.0	ns	5
14	SYSCLK to all other Outputs Valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	5.0	ns	5
15	SYSCLK to Output Invalid (Output Hold)	1.0	—	ns	3
16	SYSCLK to Output High Impedance (all except $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	6.0	ns	8
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$ High Impedance after precharge	—	1.0	t_{sysclk}	4,6,8
18	SYSCLK to $\overline{ARTRY}$ High Impedance before precharge	—	5.5	ns	8
19	SYSCLK to $\overline{ARTRY}$ Precharge Enable	$0.2*t_{sysclk}$ +1.0	—	ns	3,4,7
20	Maximum Delay to $\overline{ARTRY}$ Precharge	—	1	t_{sysclk}	4,7
21	SYSCLK to $\overline{ARTRY}$ High Impedance After Precharge	—	2	t_{sysclk}	4,7,8

Notes:

1. All output specifications are measured from the 1.4V of the rising edge of SYSCLK to TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timing are measured at the pin.
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
5. Output signal transitions from GND to 2.0V or OVdd to 0.8V.
6. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
7. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.
8. Guaranteed by design and characterization.

Figure 5 provides the output timing diagram for the XPC750P.

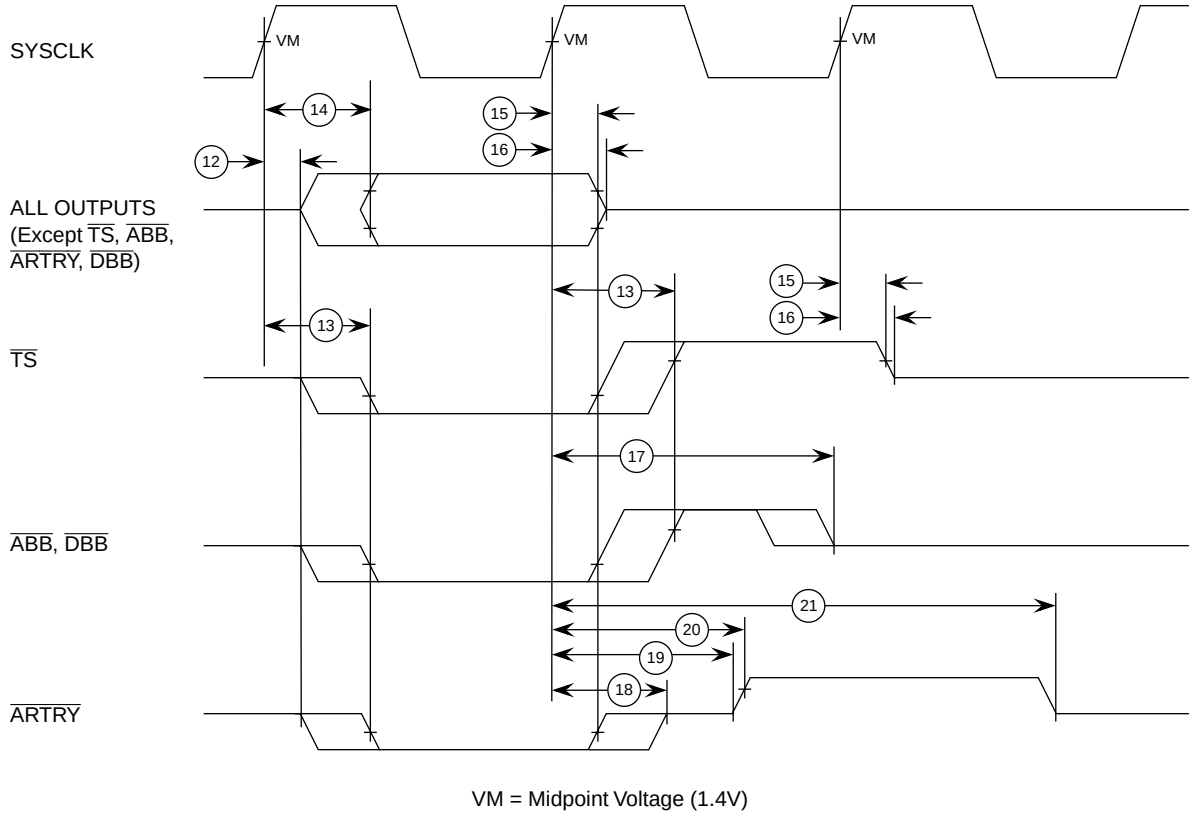


Figure 5. Output Timing Diagram

1.4.2.4 L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 15 for example core and L2 frequencies at various divisors. Table 11 provides the potential range of L2CLK output AC timing specifications as defined in Figure 6.

The minimum L2CLK frequency of Table 11 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the XPC750P core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 11 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the XPC750P will be a function of the AC timings of the XPC750P, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Motorola is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 11. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater.

L2 input and output signals are latched or enabled respectively by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC

timings of Table 12 and Table 13 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLKOUTA and L2CLKOUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Figure 12 and Table 13 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

Table 11. L2CLK Output AC Timing Specifications

At recommended operating conditions (See Table 3.)

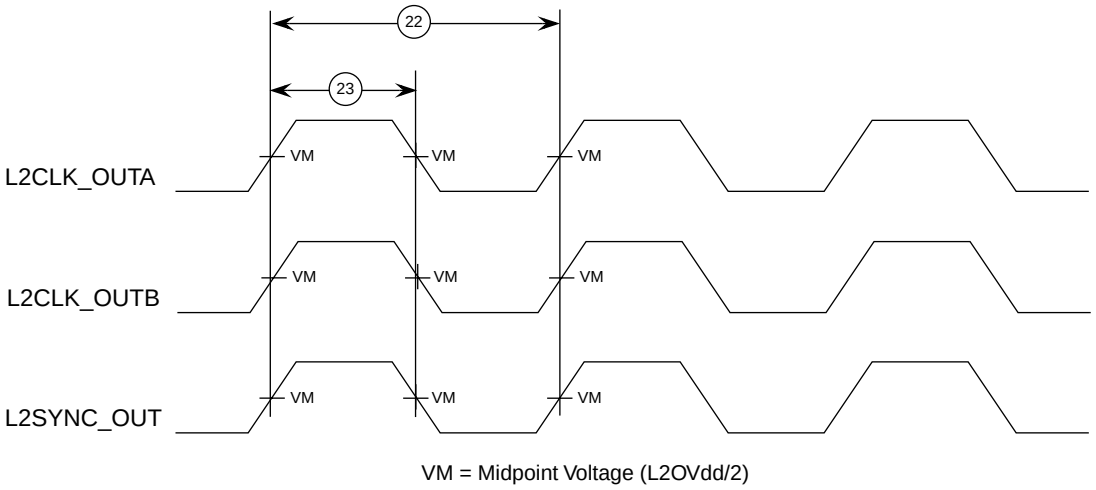
Num	Characteristic	300 MHz		333 MHz		366 MHz		400 MHz		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
	L2CLK frequency	80	300	80	333	80	366	80	400	MHz	1,4
22	L2CLK cycle time	3.3	12.5	3	12.5	2.7	12.5	2.5	12.5	ns	
23	L2CLK duty cycle	50		50		50		50		%	2
	Internal DLL-relock time	640	—	640	—	640	—	640	—	L2CLK	3
	DLL capture window	0.5	12.5	0.5	12.5	0.5	12.5	0.5	12.5	ns	5
	L2CLKOUT output-to-output skew		50		50		50		50	ps	6
	L2CLKOUT output jitter		±150		±150		±150		±150	ps	6

Notes:

1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUTC, L2CLK_OUTD, and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen such that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN. The minimum skew value allows several taps of negative adjustment without rolling over to the maximum tap. Exceptionally short paths from L2SYNC_OUT to L2SYNC_IN on the XPC750P has been observed to result in missing L2CLKOUT pulses or L2CLKOUT pulses of incorrect duty cycle.
6. Guaranteed by design and not tested. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLKOUT and the L2 address/data/control signals equally and therefore is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.

The L2CLK_OUT timing diagram is shown in Figure 6.

L2 Single-Ended Clock Mode



L2 Differential Clock Mode

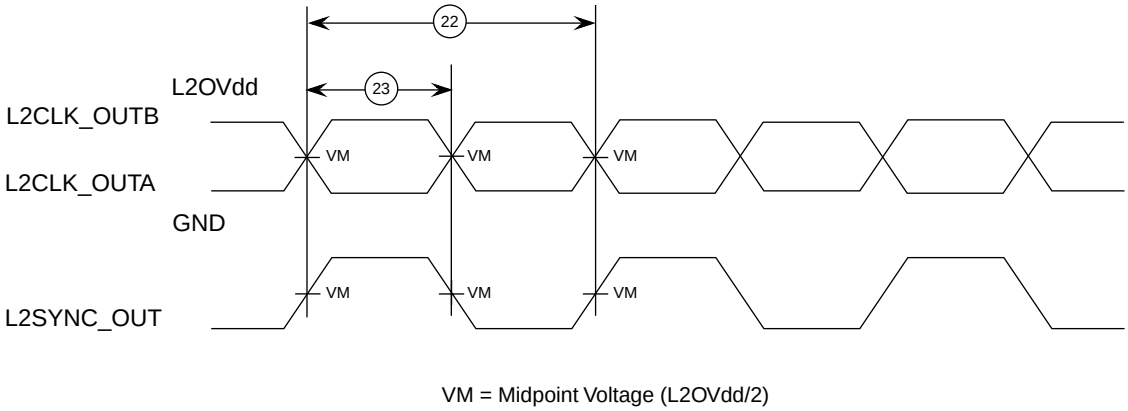


Figure 6. L2CLK_OUT Output Timing Diagram

1.4.2.5 L2 Bus Input AC Specifications

The L2 bus input interface AC timing specifications are found in Table 12.

Table 12. L2 Bus Input Interface AC Timing Specifications[1]

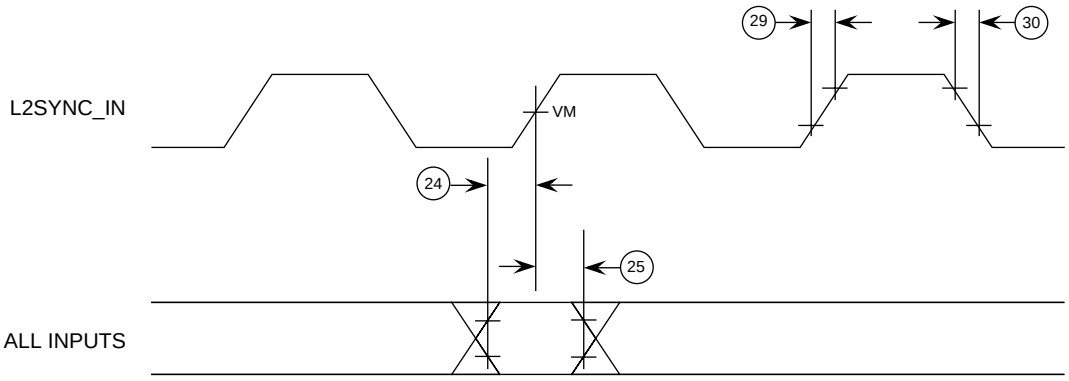
At recommended operating conditions (See Table 3.)

Num	Characteristic	Processor Frequency 300-400 MHz		Unit	Notes
		Min	Max		
29,30	L2SYNC_IN rise and fall time	—	1.0	ns	2
24	Data and parity input setup to L2SYNC_IN	1.5	—	ns	
25	L2SYNC_IN to data and parity input hold	0	—	ns	

Notes:

1. All input specifications are measured from the TTL level (0.8V or 2.0V) of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN. Input timings are measured at the pins (See Figure 7).
2. Rise and fall times for the L2SYNC_IN input are measured from 0.4 to 2.4V.

Figure 7 shows the L2 bus input timing diagrams for the XPC750P.



VM = Midpoint Voltage (1.4V)

Figure 7. L2 Bus Input Timing Diagrams

1.4.2.6 L2 Bus Output AC Specifications

Table 13 provides the L2 bus output interface AC timing specifications for the XPC750P as defined in Figure 8.

Table 13. L2 Bus Output Interface AC Timing Specifications[1]

At recommended operating conditions (See Table 3.), C_L = 20 pF[3]

Num	Characteristic	L2CR[14–15]	Core Frequency 300-400MHz		Notes
			Min	Max	
26	L2SYNC_IN to output valid	00[2]	—	4.2	
		01	—	4.7	
		10	—	4.9	
		11	—	5.2	
27	L2SYNC_IN to output hold	00[2]	0.75	—	4
		01	1.25	—	4
		10	1.45	—	4
		11	1.75	—	4
28	L2SYNC_IN to high impedance	00[2]	—	3.5	
		01	—	4.0	
		10	—	4.2	
		11	—	4.5	

Notes:

1. All outputs are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the TTL level (0.8V or 2.0V) of the signal in question. The output timings are measured at the pins.
2. The outputs are valid for both single-ended and differential L2CLK modes. For flow-thru and pipelined reg-reg synchronous burst RAMs, L2CR[14–15] = 00 is recommended. For pipelined delay-write synchronous burst SRAMs, L2CR[14–15] = 01 is recommended.
3. All maximum timing specifications assume C_L =20 pF.
4. This measurement assumes C_L = 5 pF.

Figure 8 shows the L2 bus output timing diagrams for the XPC750P.

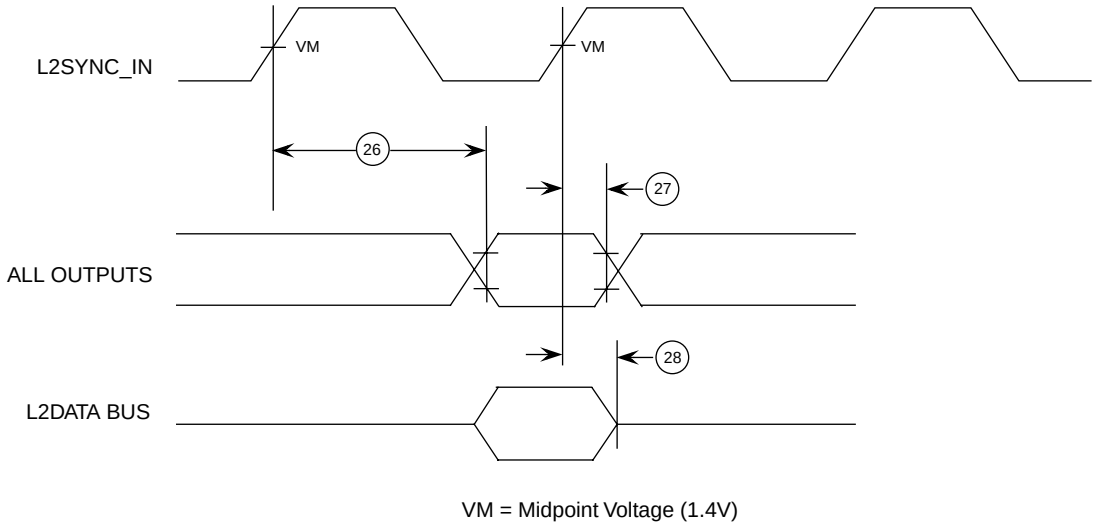


Figure 8. L2 Bus Output Timing Diagrams

1.4.3 IEEE 1149.1 AC Timing Specifications

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.5 Pin Assignments

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.6 Pinout Listings

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.7 Package Description

The following sections provide the package parameters and mechanical dimensions for the XPC740P, 255 CBGA packages.

1.7.1 Parameters for the XPC740P

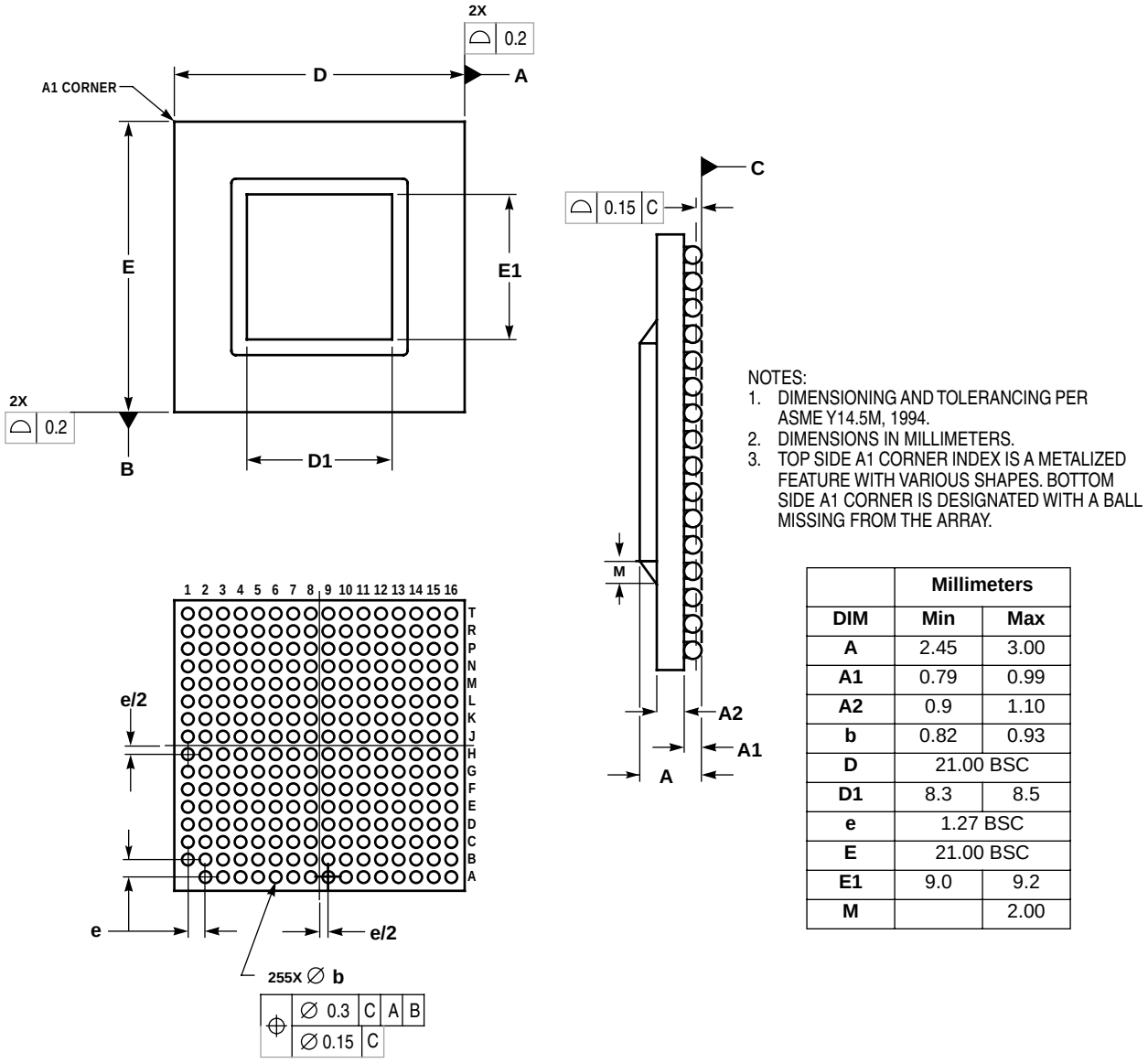
The package parameters are as provided in the following list. The package type is 21 x 21 mm, 255-lead ceramic ball grid array (CBGA).

Package outline	21 x 21 mm
Interconnects	255 (16 x 16 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.45 mm

Maximum module height	3.00 mm
Ball diameter	0.89 mm (35 mil)

1.7.2 Mechanical Dimensions of the XPC740P

Figure 9 provides the mechanical dimensions and bottom surface nomenclature of the XPC740P, 255 CBGA package.



	Millimeters	
DIM	Min	Max
A	2.45	3.00
A1	0.79	0.99
A2	0.9	1.10
b	0.82	0.93
D	21.00 BSC	
D1	8.3	8.5
e	1.27 BSC	
E	21.00 BSC	
E1	9.0	9.2
M		2.00

Figure 9. Mechanical Dimensions and Bottom Surface Nomenclature of the XPC740P

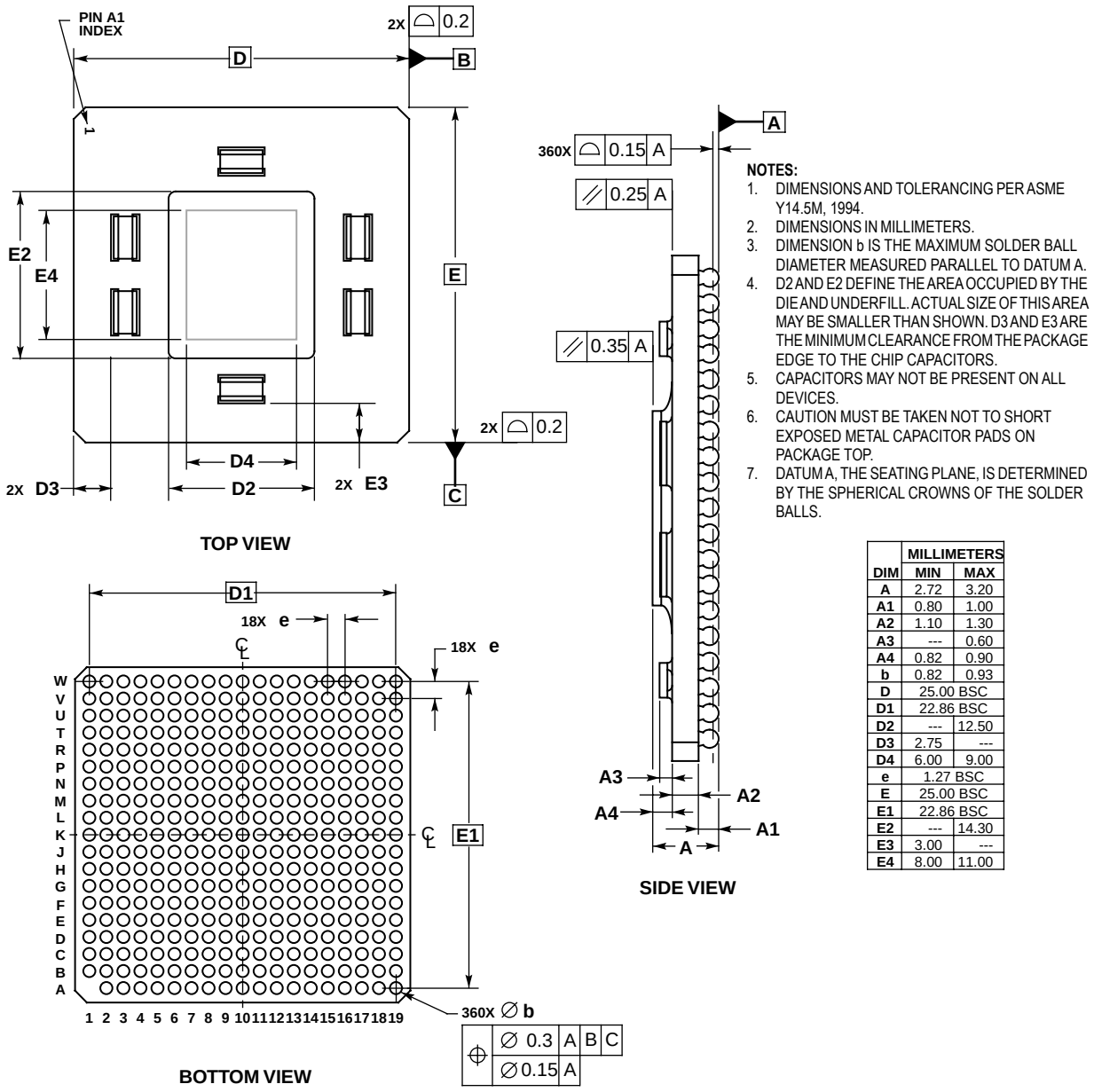
1.7.3 Parameters for the XPC750P

The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead ceramic ball grid array (CBGA).

Package outline	25 x 25 mm
Interconnects	360 (19 x 19 ball array - 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.65 mm
Maximum module height	3.20 mm
Ball diameter	0.89 mm (35 mil)

1.7.4 Mechanical Dimensions of the XPC750P

Figure 10 provides the mechanical dimensions and bottom surface nomenclature of the XPC750P, 360 CBGA package.



DIM	MILLIMETERS MIN	MAX
A	2.72	3.20
A1	0.80	1.00
A2	1.10	1.30
A3	---	0.60
A4	0.82	0.90
b	0.82	0.93
D	25.00 BSC	
D1	22.86 BSC	
D2	---	12.50
D3	2.75	---
D4	6.00	9.00
e	1.27 BSC	
E	25.00 BSC	
E1	22.86 BSC	
E2	---	14.30
E3	3.00	---
E4	8.00	11.00

Figure 10. Mechanical Dimensions and Bottom Surface Nomenclature of the XPC750P

1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the XPC750P.

1.8.1 PLL Configuration

The XPC750P's PLL is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the XPC750P is shown in Table 14 for nominal frequencies.

Table 14. XPC750P Microprocessor PLL Configuration

PLL_CFG [0–3]	Sample Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz
1000	3x	2x						250 (500)	300 (600)
1110	3.5x	2x					262 (525)	292 (594)	350 (700)
1010	4x	2x				266 (533)	300 (600)	333 (666)	400 (800)
0111	4.5x	2x				300 (600)	330 (660)	375 (750)	
1011	5x	2x			250 (500)	333 (666)	375 (750)		
1001	5.5x	2x			275 (550)	366 (733)			
1101	6x	2x			300 (600)	400 (800)			
0101	6.5x	2x		260 (520)	325 (650)				
0010	7x	2x		280 (560)	350 (700)				

Table 14. XPC750P Microprocessor PLL Configuration (Continued)

PLL_CFG [0–3]	Sample Bus-to-Core Frequency in MHz (VCO Frequency in MHz)								
	Bus-to-Core Multiplier	Core-to VCO Multiplier	Bus 33.3 MHz	Bus 40 MHz	Bus 50 MHz	Bus 66.6 MHz	Bus 75 MHz	Bus 83.3 MHz	Bus 100 MHz
0001	7.5x	2x	250 (500)	300 (600)	375 (750)				
1100	8x	2x	266 (533)	320 (640)	400 (800)				
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied						
1111	PLL off		PLL off, no core clocking occurs						

Notes:
1. PLL_CFG[0–3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the XPC750P; see Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only. **Note**: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In clock-off mode, no clocking occurs inside the XPC750P regardless of the SYSCLK input.

The XPC750P generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the XPC750P. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the XPC750P to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the XPC750P core, and the phase adjustment range that the L2 DLL supports. Table 15 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies.

Table 15. Sample Core-to-L2 Frequencies

Core Frequency in MHz	÷1	÷1.5	÷2	÷2.5	÷3
300	300	200	150	120	100
333	333	222	167	133	111
366	366	244	183	146	122
400	400	266	200	150	133

Note: The core and L2 frequencies are for reference only. Some configurations may select core or L2 frequencies which are not useful, not supported, or not tested for by the XPC750P; see Section 1.4.2.4, “L2 Clock AC Specifications,” for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

1.8.2 PLL Power Supply Filtering

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.8.3 Decoupling Recommendations

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.8.4 Connection Recommendations

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.8.5 Output Buffer DC Impedance

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.8.6 Pull-up Resistor Requirements

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.8.7 Thermal Management Information

This section is unchanged from the MPC750 Hardware Specification; refer to that document for this information.

1.9 Document Revision History

Table 16. Document Revision History

Document Revision	Substantive Changes
Rev 0	Separated XPC750P information from MPC750 Hardware Specification because of increasing diversity in operating conditions, particularly core voltage and operating temperature. Also, expanded discussion of L2CLK AC specifications to clarify and change maximum frequency of L2 operation; limited L2OVdd to 3.3V ± 5% only.; added minimum DLL skew specification; updated L2 AC timings in Table 13.
Rev 1	Changed maximum voltage for Vdd, AVdd, and L2AVdd in Table 2 to 2.5 volts.
Rev 2	Revised Figure 10.

1.10 Ordering Information

This section provides the part numbering nomenclature for the XPC750P. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office.

Figure 11 provides the Motorola part numbering nomenclature for the XPC750P. In addition to the processor frequency, the part numbering scheme also consists of a part modifier and application modifier. The part modifier indicates any enhancement(s) in the part from the original production design. The bus divider may specify special bus frequencies or application conditions. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

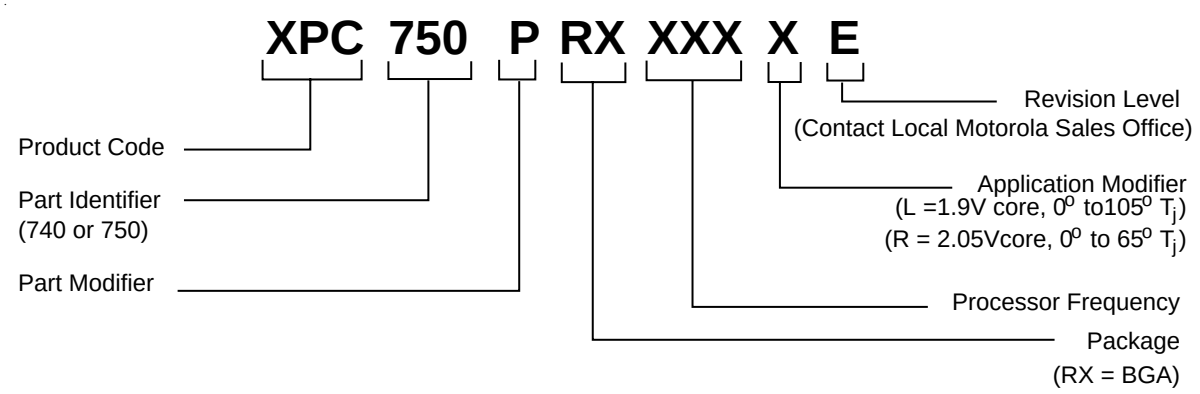


Figure 11. Motorola Part Number Key

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