Components
for Satellite Receiver Units

DCR Sat-Frontend

TUA6100B6

Gain controlled I/Q Mixer
for digital QPSK Sat signals

Preliminary Specification 01.2001 V219

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TUA6100B6
Revision History:Current Version: 01.2001 , V219

Previous version:**10.2000 , V217 -> V218**		
old Page	new Page	Subjects (major changes since last revision)
cover	**cover**	copper lead frame removed
cover	**cover**	Edition date
cover	**cover**	Spec version
20	**20**	Hysteresis of Schmitt trigger inputs, new
22	**22**	ESD note, updated
22	**22**	Ambient temperature, updated
22	**22**	Thermal resistance P-TSSOP28 + PCB board, removed
22	**22**	Detailed description of the needed thermal resistance, removed
22	**22**	Air gap package tolerances, removed
22	**22**	Thermal resistance junction case, new
22	**22**	Detailed description of the maximum junction temperature , new
23	**23**	RF input (950-2150MHz) section, definition changed to symm. balanced input, referenced to test circuit
23	**23**	Input RF level min. value corrected, test condition changed
23	**23**	Input gain control range, test condition changed
23	**23**	Quadrature error, phase + gain, test condition added
23	**23**	Quadrature error, gain, value corrected
27	**27**	Test circuit , new
27	**28**	Application circuits , updated input configuration
28	**29**	Application circuits , updated input configuration + crystal series capacitor

Previous version:**12.2000 , V218**		
old Page	new Page	Subjects (major changes since last revision)
cover	**cover**	Edition date
cover	**cover**	Spec version
2	**2**	Ordering Information, packages updated
22	**22**	Ambient temperature note, updated
23	**23**	Minimum input RF level , new description
23	**23**	Maximum input RF level , new description
27, 28	**28**, **29**	Application circuits , updated input configuration
41	**41**	Plastic Package, P-TSSOP-28-1 alloy leadframe, added

Data Classification

Maximum Ratings
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Characteristics
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Operating Range
In the operating range the functions given in the circuit description are fulfilled.
For detailed technical information about **"Processing Guidelines"** and
"Quality Assurance" for ICs, see our **"Product Overview"**.

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Gain controlled I/Q Mixer
for digital QPSK Sat signals

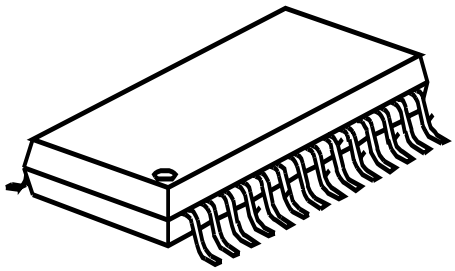
TUA6100B6

Preliminary Specification

BICMOS

1 Features

- Low impedance gain controlled RF input
- Dual matched double balanced mixer
- Digital generation of 0°/90° LO signal
- Direct down conversion from 1. IF (LNB output) to base band 0-30 MHz
- IF filter not necessary
- I / O for external baseband filter
- CMOS PLL-Synthesizer
- Active loop filter (high voltage)
- 3 high current switch outputs
- Buffered crystal oscillator output
- Low noise reference voltage
- 3-wire bus and
- I^2C bus with 4 addresses + subaddresses
- Splitting of Sat tuning range into 2/3 bands
- LO - frequency below and above input frequency possible



TSSOP-28

Package

2 General Description

The TUA 6100 is a low cost chip in the newest Infineon high speed BICMOS technology B6HFC. It is designed to implement the direct conversion receiver principle for digital QPSK-Sat receiving systems.

The DCR architecture eliminates the need for expensive RF-Filters for image rejection and IF-Frequencies for channel selection. Instead, an inexpensive base band low-pass filter is used for channel selection, and no image rejection filter is required.
These base band filter enable the possibility for an on chip integration. (not part of TUA6100)
The DCR system is the most promising architecture to lower the cost of digital set-top boxes front end.

Via a gain controlled RF preamplifier (not part of TUA6100) with approx. 30 dB gain and some selectivity, the RF signal is symmetrical fed to two low input impedance double balanced mixers .
The mixers have common inputs with internal power splitting and incorporate a new patented direct gain control in the mixer input stage and an additional gain control at the mixer output to improve S/N ratio.
The signal of the synthesizer tuning VCO is multiplied to 4 x RF input frequency via a complete internal 3.8-8.6 GHz PLL system.
To drive the mixers, this 3.8-8.6 GHz signal is split into quadrature components by a Johnson-counter $\div 4$.
The mixers are followed by 2 matched 16 dB fixed gain base band amplifiers making available the first linear DC-coupled base band outputs with approx. 224 mV_{pp} for the I and Q signal .
Two additional 16 dB fixed gain base band amplifiers with approx. 1 V_{pp} output voltage enable the possibility to use system adapted external AC-coupled base band filter and eliminate undesirable DC-components of the first amplifiers .

The TUA 6100 contains

- 2 double balanced mixer cells with new patented direct gain control,
- a digital generation of the 0°/90° local oscillator phase shifted signal to ensure minimum quadrature phase error,
- an internal synthesizer VCO with programmed band splitting and external varactor and resonator,
- 2 internal GHz VCO's and a PLL for generation of 4 x RF input frequency, (necessary for the accurate digital generation of the LO I/Q components)
- a CMOS PLL-synthesizer controlled by I^2C or 3-wire bus,
- an active synthesizer loopfilter with high voltage and high current output,
- an on chip reference oscillator (external crystal) which can be overridden by an external oscillator, and
- 4 ultra linear base band output amplifiers with approx. 16dB gain each.

The PLL-synthesizer is programmable to work with reference frequencies > 4kHz and up to 2 MHz, for more information *see Divide ratio programming on page 14*. A programmable phase detector output current makes it easy to select several transconductances controlled by bus.

A simple Windows control-program for I^2C / 3-wire bus with short description is available.

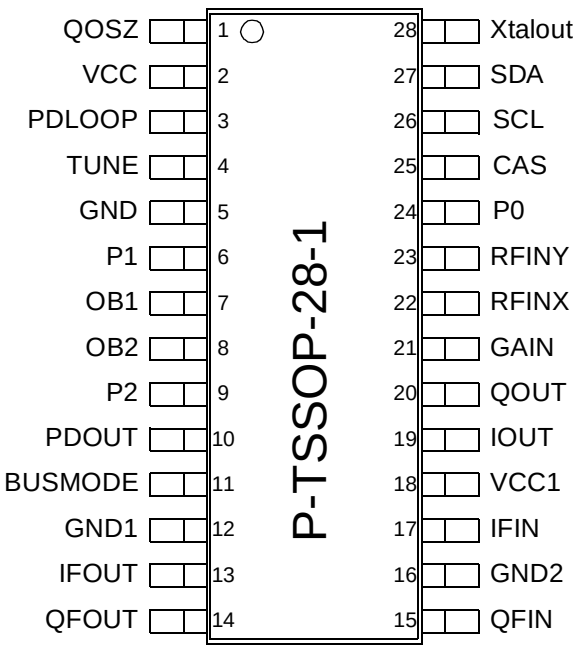
3 Ordering Information

Type	Ordering Code	Package
TUA6100B6	Q 67037-A 1034 A 701	P-TSSOP-28-1
TUA6100B6	not yet available	P-TSSOP-28-5

4 Pin Configuration

top view

2-pin synthesizer VCO configuration



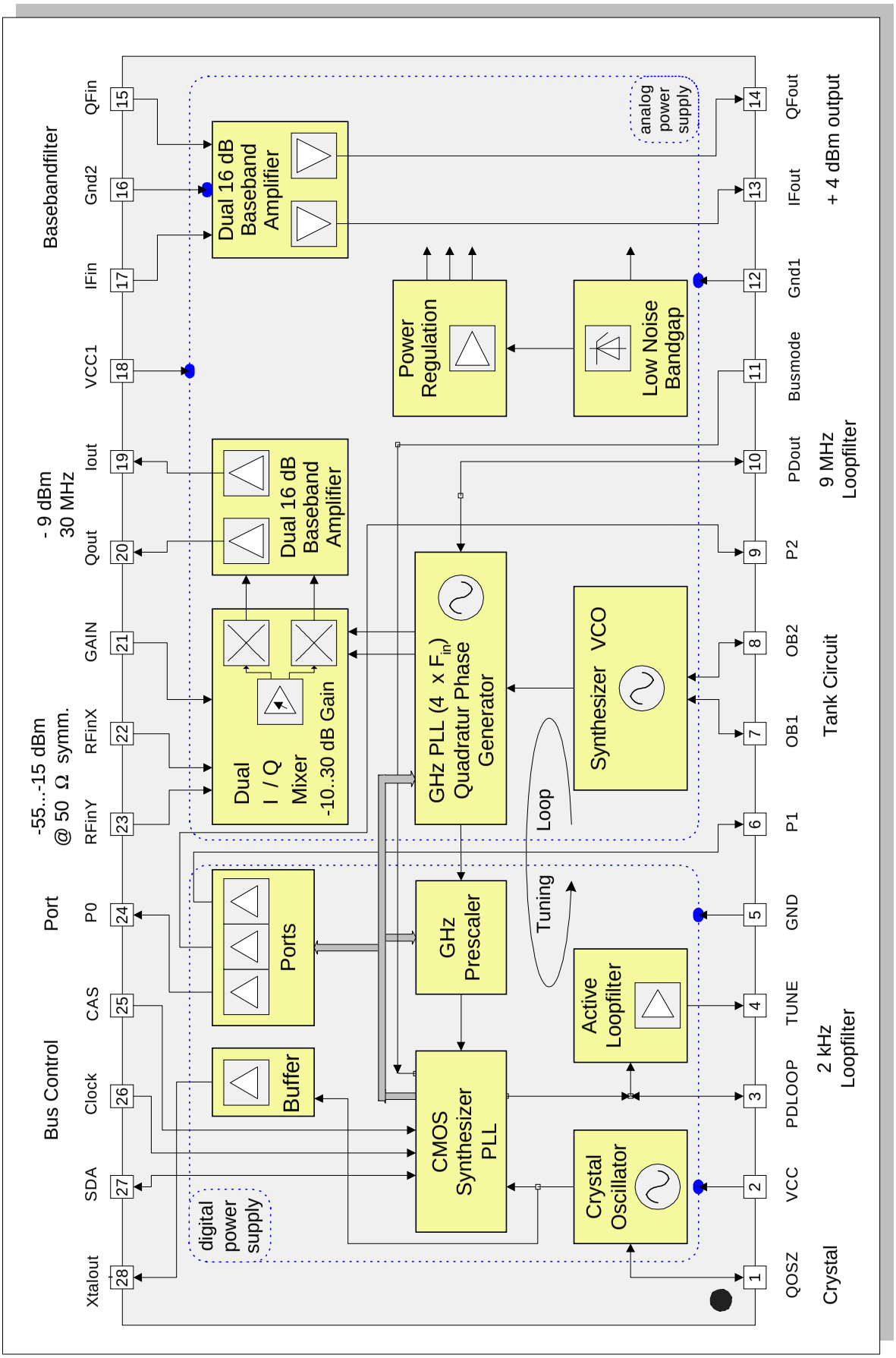
5 Pin Definitions and Functions

Pin No.	Symbol	Function
P-TSSOP-28		
1	QOSZ	Reference oscillator input / Crystal
2	VCC	Power supply voltage for I^2C / 3-wire bus and synthesizer
3	PDLOOP	Synthesizer Phase detector Charge pump output / Loop filter input
4	TUNE	Synthesizer Loop filter high voltage tuning output
5	GND	Ground for I^2C / 3-wire bus and synthesizer
6	P1	Port 1 output
7	OB1	VCO for synthesizer, stripline input 1
8	OB2	VCO for synthesizer, stripline input 2
9	P2	Port 2 output
10	PDOUT	Phase detector loop filter of internal GHz-PLL
11	BUSMODE	Selection of I^2C / 3-wire bus
12	GND1	Ground for analog part; LO and 0°/90° phase generator
13	IFOUT	Base band I output
14	QFOUT	Base band Q output
15	QFIN	Q baseband filtered input signal
16	GND2	Base band Ground
17	IFIN	I baseband filtered input signal
18	VCC1	Power supply voltage for analog part; LO and 0°/90° phase generator
19	IOUT	Base band I output for base band filter
20	QOUT	Baseband Q output for baseband filter
21	GAIN	AGC voltage input
22	RFINX	RF differential input signal (950-2150MHz)
23	RFINY	
24	P0	Port 0 output
25	CAS	CAS input for I^2C bus, Enable input for 3-Wire-bus
26	SCL	Clock input for I^2C bus, Clock input for 3-Wire-bus
27	SDA	SDA input/output for I^2C bus, Data input for 3-Wire-bus
28	Xtalout	Buffered crystal oscillator output

6 Applications

- DBS, DVB-S, DSS Set-Top Boxes,
- any I/Q Downconverter from 950 MHz - 2150 MHz to frequencies 0 - 30 MHz

7 Block Diagram



8 Circuit Description

The main function of the chip is split into bipolar analog signal processing, bipolar digital signal generation of 0°/ 90° LO-signal and a CMOS synthesizer.
Extremely symmetrical layout with matched structures promises best phase and gain balance of the inphase and quadraturephase signals.

8.1 Input Mixer

Parameter *see RF input (950-2150MHz) symm. balanced signal on page 23*
Main function is the conversion of a preselected satellite 1. IF band into the inphase and quadraturephase baseband signals.
The input stage of the mixer is directly combined with a new patented differential input gain control of 30 dB control range and a double balanced mixer with additional gain control of 15 dB in the output.
The integration of the gain control into the mixer cell results in high compression point / IP3 at full attenuation and requires low chip area .
The differential input has low impedance and is designed for 50 Ω systems with a certain mismatch.
Due to the built in gain control the mixer conversion gain varies between -10 and +35 dB.
The output is internal DC-coupled to the first base band amplifier.
For best performance the 0°/ 90° LO-signal is fed to the mixer via open collector stages with well defined output impedance and levels.
The *AGC voltage input* is positive DC-controlled, that means 0.5V - min. gain, 3V - max. gain, with MOS high impedance input.
The characteristic of the *RF gain control range* is mainly non linear .

8.2 Baseband Amplifier

Parameter *see Base band I / Q output, on page 23*
and *Base band I / Q output filtered, on page 24*
The 4 base band amplifiers are of wide-band operational type with high overshoot margin.
The DC reference voltage is internal set to 2.15 V dc .
All the amplifiers have a fixed gain of 16 dB and 30 MHz_{-0dB} bandwidth.
The distribution of the whole DC-gain into two AC-coupled 16 dB amplifiers ensures that the base band amplifiers are not overdriven by a large DC-voltage that may be caused by mixer offset or mixer LO feedback to the input.
All 4 outputs can be disabled by bus control. (*Register 02*,D14)
In this state the outputs switch to low voltage and low impedance.

8.3 Output Ports

Parameter *see Port outputs, P0, P1, P2 on page 26*
The output ports are designed with open collector transistor for high current pull down and slow switching application.

8.4 Reference Voltage

Parameter *see Power supply on page 23*
The central reference voltage is a low noise high PSSR bandgap with approx. 2.4 V DC and low temperature drift.

8.5 Reference Oscillator

Parameter *see Reference oscillator input / Crystal on page 24*
The reference oscillator input is the low impedance feedback of a cascode amplifier and uses the low series resonance of a crystal to generate an oscillation condition.
For a wide characteristic range the reference oscillator can use crystals from 1 - 16 MHz and may be used as external AC-coupled reference input if no crystal is present.

8.6 Crystal Oscillator Output

Parameter *see Crystal oscillator output on page 26*

To reduce the amount of application components in combination with a digital QPSK demodulator, the TUA 6100 offers an buffered Push-Pull output of the crystal oscillator. The frequency is the crystal frequency and is not programmable, the output signal is always on.

8.7 Synthesizer Loop filter

Parameter *see Synthesizer Loop filter high voltage tuning output on page 25*

The synthesizer active loop filter consists of a simple inverting BICMOS amplifier with MOS input and a special open collector output transistor which can handle high voltage and high output currents.
The loop filter input is internal connected to the phase detector / charge pump output.
The BICMOS amplifier output may be disabled (high Z) by bus, control register (*Register 00*,D0).

8.8 Synthesizer VCO

Parameter *see Synthesizer VCO on page 26 .*

The synthesizer VCO is a symmetrical Colpitts type oscillator with an external tank circuit.
The tank circuit consists of two microstrip lines connected to the oscillator bases and at the microstrip line ends two serial connected varicap diodes. These diodes are driven by the tuning voltage.
The synthesizer VCO oscillates at a programmed offset to the input frequency.
This guarantees minimum oscillator pulling and self-mixing with the result of undesirable DC-signal voltage.
The offset may be at low side or high side of the input signal or zero (that means $F_{vco} = F_{input}$).
The VCO tuning range is digital split into 2 or 3 bands controlled by the internal GHz PLL.
(not possible if operation $F_{vco} = F_{input}$ is desired for the hole tuning range)
Advantages :

- only one optimized VCO for the complete tuning range which is approx. 1 : 2.34 (due to the KVCO and Loop bandwidth variation it is difficult to obtain this range by one conventional VCO with constant low phase noise) .
- reduced external components
- smaller package
- lower phase noise due to the reduced tuning range of VCO
- lower synthesizer loop filter bandwidth variation
- lower maximum tuning voltage.

Detailed programming tables *see GHz PLL programming on page 9 .*

8.9 Phase Shift 0° / 90°

Parameter *see Synthesizer PLL on page 25*

To get minimum quadrature phase error, a digital generation of the 0°/90° phase shifted local oscillator signal is implemented by a 3.8-8.6 GHz Johnson-counter ÷ 4 .
This counter is designed in high speed stacked ECL bipolar technology.

8.10 GHz VCO

Two On-Chip bipolar LC-Oscillators (3.4-6.2 GHz and 6.0-8.6 GHz) controlled via On-Chip PLL .
The GHz VCO's oscillate at 4 x of the input frequency and are current controlled.
The resonant circuit is an on chip symmetrical inductor driven by differential pair amplifier whose current variable parasitic capacitance is used for frequency tuning.
The used special multi-tanh gilbert cell makes a wide tuning range possible.
The complete GHz VCO's are under control of a 3.8-8.6 GHz PLL system.
The reference frequency of this system is the output of the synthesizer VCO divided by a programmable counter; variation is 118-538 MHz(depending on the selected synthesizer tuning range).
At the same time this is the operating frequency range of the phase detector / charge pump.
The high speed charge pump is completely on chip and designed in BICMOS technology with an external loop filter bandwidth set to 9 MHz.
The GHz VCO frequency is fed to the phase detector via the high speed ECL Johnson counter ÷4 and a lower speed programmable ECL counter.

8.11 GHz PLL

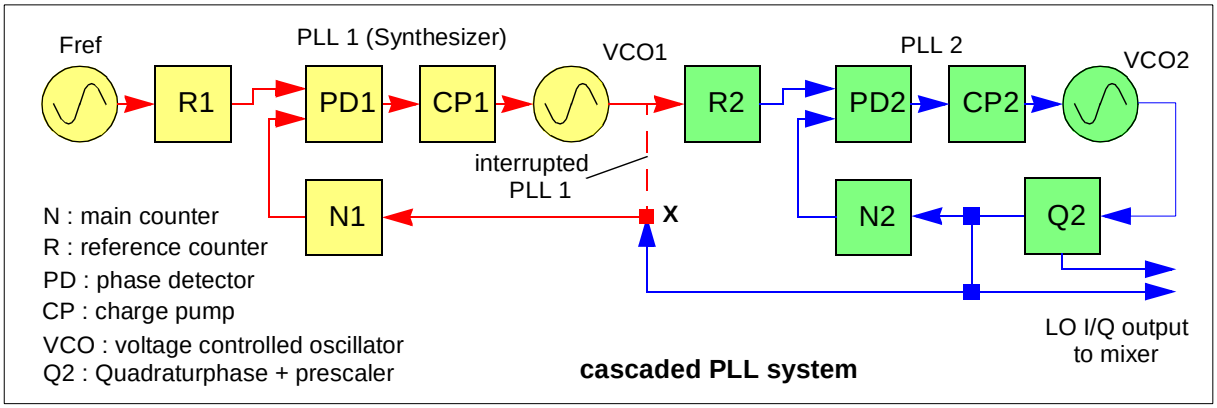
Normally in DCR systems it is necessary that the synthesizer VCO oscillates exact at the desired receiving frequency.
The following description shows a new patent pending double PLL tuning system without this requirement and enables some features that other concepts do not have.

The main benefit of this new concept is :

- the accurate 0 / 90° generation of the LO signals for the RF input mixer,
- no oscillator on input frequency,
- a programmed frequency offset of synthesizer VCO to the RF input frequency and due to that a
- very low VCO oscillator pulling and self mixing according to power crosstalk of RF input and
- the possibility of splitting the tuning range into bands.

Responsible for these advantages is a 2nd GHz PLL system with two VCO's at 4 x Fin.

This 2nd GHz PLL system is located in the broken up feedback of the synthesizer PLL 1 between the VCO1 and the programmable counter input N1. This represents a system of two cascaded PLL's.



cascaded PLL system

This location enables a shift of the synthesizer VCO1 to other frequencies, independent of the required input LO frequency of the RF mixers.

In this case the synthesizer VCO must **not** oscillate at the required LO frequency of the mixer input. Nevertheless the synthesizer PLL is referenced to the LO frequency of the mixer input which makes it easy to program the PLL because it is set exact to the receiving frequency.
Another benefit is the exact mapping of the PLL stepsize to the tuning frequency.

This is not possible in a conventional PLL tuning system with the feedback of the VCO1 direct to the programmable counters N1, if the VCO1 is not running on the RF input frequency.
This may become clear in the above concept, if the interrupted PLL 1 is closed and the LO I/Q output is cut off from node x.
In this case step size and tuning frequency have additional terms of calculation. Depending on the system concept. they do not fit to the programmed values of the synthesizer PLL 1, because it is referenced to the VCO1 and no longer to the LO I/Q output.
(following dependencies will become valid, $F_{tune} = (N2 / R2) * F_{vco1}$ and $F_{step} = (N2 / R2) * PLL1_{step}$).

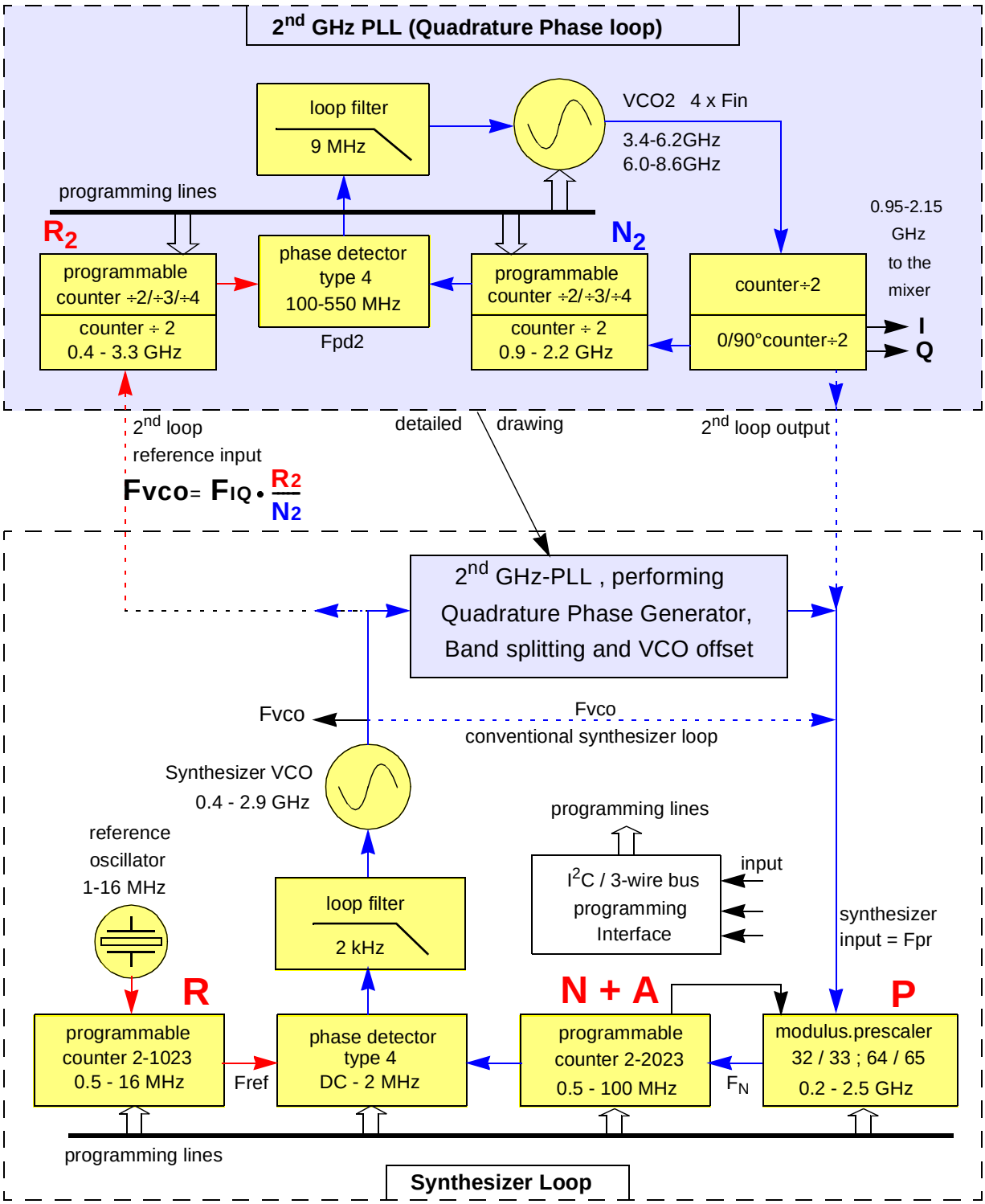
The R2 and N2 counters of the GHz PLL enable a programmable frequency offset of the synthesizer VCO to the RF input as well as a splitting of the required RF tuning range.

For the band splitting feature the counters R2 and N2 of the GHz PLL must be used with 2 different values (e.g. 4/2 and 4/3). As a result VCO1 will pass his range twice, while the LO I/Q output to mixer will have a tuning range which is split into 2 bands.

In the feedback of the GHz PLL is located the high speed Johnson-counter $\div 4$ (Q2) which acts as prescaler for the two 3.4 - 8.6 GHz VCO's and accurate 0 / 90° LO generator.

The complete GHz PLL is designed in high speed ECL cascoded technology which enables counter frequencies up to 15 GHz , oscillator frequencies up to 10 GHz and phase detector / charge pump signal slopes of less then 100 ps.

8.11.1 Functional GHz PLL Block Diagram



8.11.2 GHz PLL programming

programmable tuning ranges of the synthesizer VCO controlled by GHz PLL for Fin = 950 - 2150 MHz

$\frac{F_{VCO}}{F_{Input}}$	0.5	0.66	0.75	1	1	1	1.33	1.5	2		GHz-PLL
	$\frac{2}{4}$	$\frac{2}{3}$	$\frac{3}{4}$	$\frac{2}{2}$	$\frac{3}{3}$	$\frac{4}{4}$	$\frac{4}{3}$	$\frac{3}{2}$	$\frac{4}{2}$		$\frac{R2}{N2}$ R-Counter N-Counter
	Possibilities of 2 band splitting without VCO at input frequency										**1:1.51 tuning range**
$Fvco_{min}$ $Fvco_{max}$	712 1076	<- + ->	712 1076				1900 2870	<- + ->	1900 2870	MHz	$F_{vco} = \frac{R2}{N2} \times F_{in}$
Fin_{min} Fin_{max}	1424 2152	<- + ->	949 1434				1425 2152	<- + ->	950 1435	MHz	band switching at 1430 MHz
	Possibilities of 3 band splitting without VCO at input frequency										**1:1.53 tuning range**
$Fvco_{min}$ $Fvco_{max}$	700 1075	830 934	712 934				2173 2867	2182 2445	1900 2910	MHz	$F_{vco} = \frac{R2}{N2} \times F_{in}$
Fin_{min} Fin_{max}	1400 2150	1245 1400	949 1245				1630 2150	1455 1630	950 1455	MHz	band switching at 1455, 1630 1245, 1400 MHz
	low side VCO			**VCO at Fin**			**high side VCO**				

Note: the maximum operating frequency of the synthesizer VCO is 2.9 GHz
for the low side VCO mode and VCO at Fin application is not yet available.

8.11.3 Synthesizer VCO band switching

Programming tables of the synthesizer VCO band switching controlled by the GHz-PLL

Register 01 Subaddress 01H	
D23	GHz VCO Switch
0	3.4-6.2 GHz
1	6-8.6 GHz

Register 01 Subaddress 01H		
$N1_2$ D21	$N0_2$ D20	N-Counter GHz-PLL
0	0	: 3
0	1	: 4
1	0	: 2
1	1	: 3

Register 02 Subaddress 02H		
$R1_2$ D13	$R0_2$ D12	R-Counter GHz-PLL
0	0	: 3
0	1	: 4
1	0	: 2
1	1	: 3

recommended switching at 1525 MHz

RFin below 1525 MHz	
0	3.4-6.2 GHz
RFin above 1525 MHz	
1	6-8.6 GHz

recommended switching for band splitting (high side VCO), Fvco = 1900 - 2870 MHz

						RFin 2 band	RFin 3 band
1	0	: 2	0	1	: 4	< 1430 MHz	< 1455 MHz
1	0	: 2	0	0	: 3	not used	1455-1620 MHz
0	0	: 3	0	1	: 4	> 1430 MHz	> 1620 MHz

(low side VCO), Fvco = 712 - 1076 MHz

0	1	: 4	0	0	: 3	< 1430 MHz	< 1245 MHz
0	0	: 3	1	0	: 2	not used	1245-1400 MHz
0	1	: 4	1	0	: 2	> 1430 MHz	> 1400 MHz

The GHz VCO must be switched in any case at RFin =1525 MHz if a tuning range including frequencies below and above 1525 MHz is used.

8.12 Synthesizer PLL

Parameter see *Synthesizer Phase detector Charge pump output / Loop filter input* and *Synthesizer PLL* (*page 25*).
The PLL block forms a digitally programmable **p**hase **l**ocked **l**oop (PLL) with a serial bus control. The circuit consists of a serial control logic, a high frequency dual modulus prescaler, an A- and a N-counter with dual modulus control logic, a reference- (R-) counter, and a phase detector with lock detector and charge pump output.

8.12.1 Serial Bus Control Logic

For TUA6100 the combi-bus is selectable between I^2C and 3-wire-busmode by pin BUSMODE (I^2C = low, 3W = high).
All bus pins (CLOCK, DATA, ENABLE and BUSMODE) are Schmitt-triggered with input buffer for 3V or 5V µC.
Programming of the IC is done by a serial data protocol with sub addressing. The contents of the message is assigned to the functional units according to the preceded sub addresses.
Before programming the counters the control register (sub address 00_{Hex}) should be set.
The data bit stream starts with the most significant bit (MSB) and is shifted in on the low to high transition of the clock signal.

- **I^2C bus mode**

  In this mode four different chip addresses can be set by appropriate DC level at pin ENABLE which has in this case the function of a **c**hip **a**ddress **s**elect (CAS). The pin DATA is a bidirectional input/output pin for **s**erial **da**ta (SDA) from and the acknowledge bit (ACK) to the microcontroller (µC).

Data Transition:

Data transition on the pin DATA must only occur when the **s**erial **cl**ock (SCL) is low.
SDA transitions while SCL is high will be interpreted as start or stop condition.

Start Condition (STA):

A start condition is defined by a high to low transition of the SDA line while SCL is at a stable high level.This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):

A stop condition is defined by a low to high transition of the SDA while the SCL line is at a stable high level. This condition terminate the communication between the devices and forces the bus interface into the initial conditions.

Acknowledge (ACK):

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will pull the SDA line to low level to indicate it has received the 8 bits of data correctly.

Data Transfer Write Mode:

To start the communication, the bus master must initiate a start condition, followed by the 8bit chip address (write). The chip address for the TUA 6100 is fixed as ”11000xyz” (MSB at first).
The last significant bit (LSB=z) of the chip address byte defines the type of operation to be performed: z=1 means, a read operation is selected and z=0 means, a write operation is selected.
After the successful comparison of the transmitted chip address with the fixed one include the hard-switched chip address select bits CAS2=x and CAS1=y, the serial control logic of the TUA6100 will generate an ACK. Otherwise the processor must break off the data transfer.
After this device addressing the desired subaddress byte and data bytes must be followed. The subaddresses determines which one of the data bytes (00H...03H) is transmitted first.
At the end of the data transition the master must generate the stop condition.

Data Transfer Read Mode:

To start the communication in the read mode, the bus master must initiate a start condition, followed by the 8bit chip address (write: z=0) and by the subaddress (80H) of the read register. Then followed by the chip address (read: z=1). After that procedure the 8bit data register 80H is read out. When the first byte(s) read out the µC mandatory send LOW during the ACK-clock, but after the last byte is read out the µC mandatory send HIGH (neg. ACK) during the ACK-clock. At the end of data transition the master must be generate the stop condition.

- **3-wire bus mode**

Pin DATA is in this mode only data input. There is no data output. Pin ENABLE is used to activate the bus interface and to allow the transfer of data to the device. When ENABLE is in an inactive high state, shifting is inhibited.

Data Transition:

Data transition on the pin DATA must only occur when the clock SCL is low. To transfer data to the device, ENABLE (which must start inactive high) is taken low. A serial data transfer is made via DATA and CLOCK when ENABLE is taken back high. The bit stream doesn't need a chip address.

Data Transfer Write Mode:

To start the communication, the signal ENABLE is taken low. The desired subaddress byte and data bytes must be followed. The subaddresses determines which one of the data bytes (00H...03H) is transmitted first. At the end of the data transition the bus ENABLE must be high.

Data Transfer Read Mode:

To start the communication in the read mode, the ENABLE is taken low, followed by the subaddress read (xxH). After that the device is ready to read out the xbit data register xxH. At the end of the data transition the ENABLE must be high.

- **Dual Modulus Prescaler**

The dual modulus prescaler up to 2.5 GHz is switchable between divide ratio 32/33 and 64/65 by the bit D22 in the A/N-counter subaddress (01H). Input frequency of the prescaler is the divided GHz-VCO-frequency ÷ 4 with the range of 950 MHz .. 2150 MHz.

- **R-Counter and A- / N-Counter**

The TUA 6100 has a 10-bit counter for the R-path and a 7-bit and 11-bit counter for the A-/N-path. The input frequency for the R-counter is the buffered XTAL-frequency (1-16 MHz). Tuning steps can be selected by the programmable R-counter from f_R = 31.25 kHz ..1 MHz (f_{XTAL}=16MHz).
The output frequency of the prescaler (14 MHz..70 MHz) passes the programmable dual modulus A-/N-counter which switches the prescaler and make available the comparison frequency f_V for the digital frequency / phase detector.

- **Phase Comparator (Frequency/Phase Detector)**

The digital phase and frequency sensitive phase detector generates a phase error signal UP or DOWN according to the phase difference between f_R (R-counter output) and f_V (N-counter output).
This phase error signal drives the charge pump current generator.
Polarity is changeable via bus (bit D4 of the control register), it must be negative for TUA6100 application note.
If the positive edge of the divided VCO signal appears prior to the positive edge of the reference signal, the DOWN-output pulses for the duration of the phase difference.
In the reverse case the UP-output pulses.
If the two signals are in phase (PLL is locked), the phase detector produces an output signal with fixed anti-backlash impulses in order to prevent a dead zone for very small phase deviations.
Therefore phase differences of less than 100 ps can be resolved.
In general the shortest anti-backlash pulse gives the best system performance.

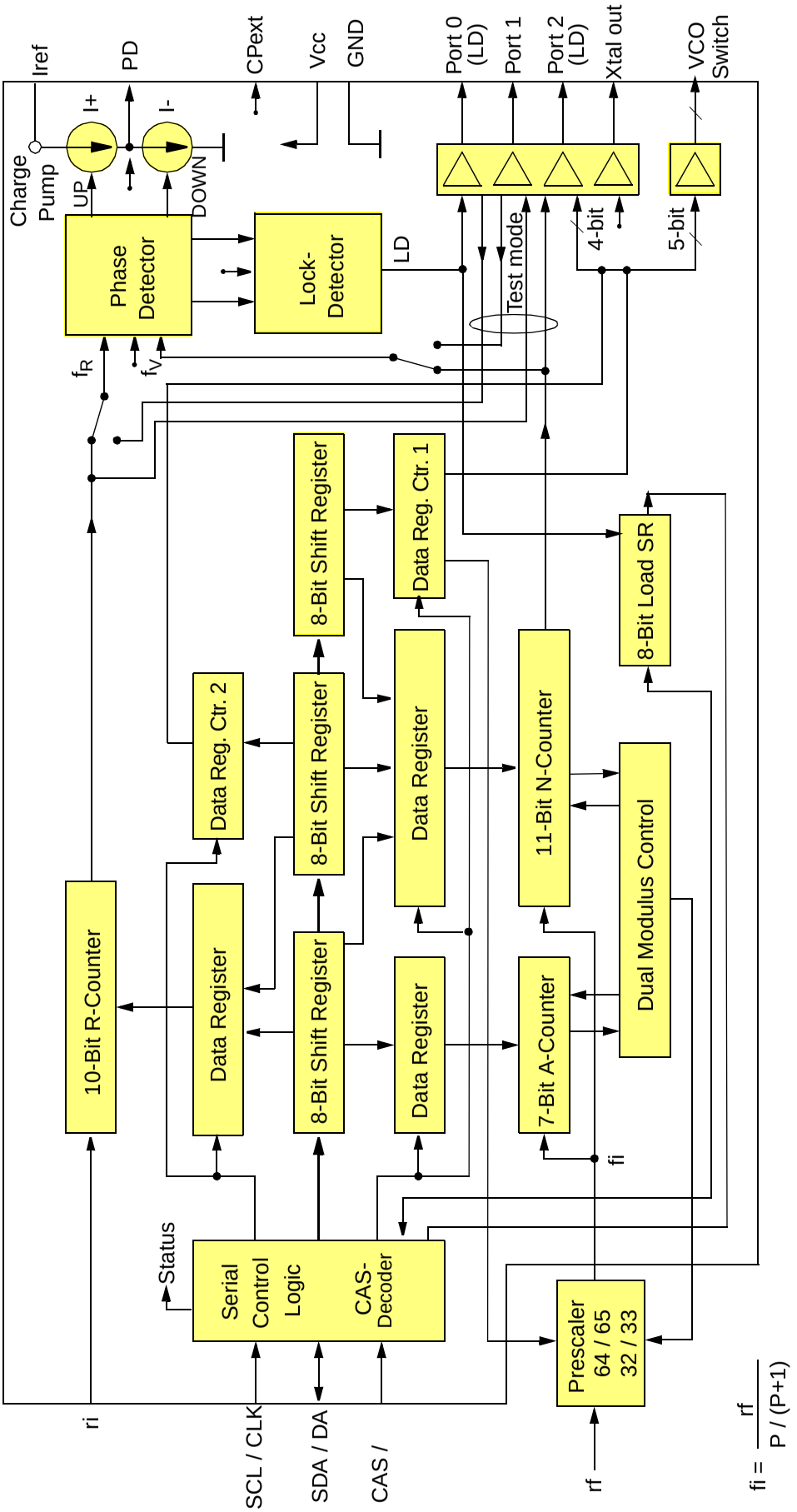
- **Charge Pump**

  The charge pump generates defined pulses of current (I+ and I-) by the phase detector UP- and DOWN signals. If the PLL is locked and the bit D1 of the control register is LOW, the charge pump output (pin 3: PDLOOP) goes into the high-impedance state.
  There are four current values selectable by bit D2 and D3 of the control register (subaddress 00H).
  Note : only 100µA and 1mA are optimized.
  The synthesizer charge pump output may be disabled (high Z) by bus, control register(Register 00, D1).

- **Lock Detector**

  The lock detector indicates when the PLL is locked (lock_in: LD_out = high).
  It is possible to put out the lock detect signal to the ports P0 or P2, by the control register bits D5 and D6.
  In this case the content of the respective control register bit for port P0 or P2 (D18 of subaddress 01H or D10 of subaddress 02H) is not active.
  Parallel the lock detector information may be read out by bus (D7 of subaddress 80H).

8.12.2 Functional Synthesizer PLL Block Diagram



8.12.3 Divide ratio programming

Because of DCR concept the tuning frequency of the RF input controlled by the PLL is given below:

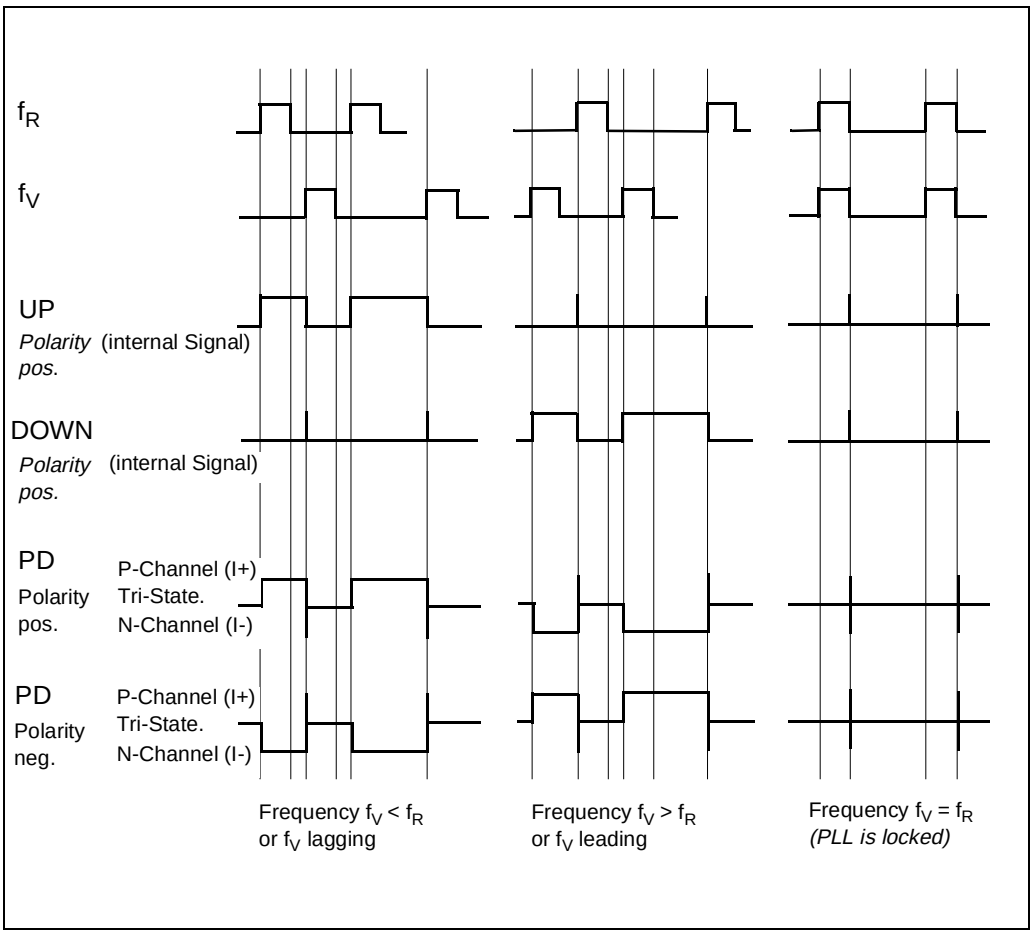
$$rf = [(P \cdot N) + A] \cdot \frac{ri}{R} = \frac{M}{R} \cdot ri \qquad \text{with} \qquad A \leq N$$

rf :	frequency of RF_{input}
ri :	reference frequency input (crystal oscillator)
P :	divide ratio of the prescaler [P/(P+1) = (32/33) or (64/65)]
A :	divide ratio of the A-counter (max. 7 bit)
N :	divide ratio of the N-counter (max. 11 bit)
R :	divide ratio of the R-counter (max. 10 bit)
M = (P∗N)+A :	total divide ratio of the PLL (with A<N)

Note : for continuous frequency steps following condition is necessary

$$[(P \cdot N) + A] \geq P \cdot [P - 1]$$

8.12.4 Phase detector outputs



8.13 Bus Interface

Pin Function

Pin name	BUSMODE	Data	Clock	Enable
Function	Bus-Mode-Select	Serial data	Clock	Enable (3W) / Chip-Address-Select (I2C)
I^2C-mode (I2C)	Low	Data in / out	Clock in	Four Chip-Addresses (see below)
3Wire mode (3W)	High	Data in / out		High=Inactive, Low=Active

8.13.1 Chipaddress Organisation

(only I^2C-Mode)

Chip Address

MSB							LSB	Function
1	1	0	0	0	CAS2	CAS1	0	Chip Address Write
1	1	0	0	0	CAS2	CAS1	1	Chip Address Read

Chip-Address-Select (CAS)

Voltage on Pin CAS[1)]	How to do?	CAS2	CAS1	Chip-Address	
				Hex	Dec
0...0,5 V	Pin CAS external on GND	0	0	C0	192
open circuit	Pin CAS = 1,25 V (intern)	0	1	C2	194
2,0..3,0 V	R_{ext} = 68 kOhm external on Vcc , tolerance for R_{ext} +-20%	1	0	C4	196
> 4,5	Pin CAS external on Vcc	1	1	C6	198

1) Vcc = 5V, voltage is a function of resistor divider from Vcc

8.13.2 Subaddress Organisation

Sub Addresses of Write Data Registers									
MSB							LSB	Hex	Function
0	0	0	0	0	0	0	0	00	Control-Register
0	0	0	0	0	0	0	1	01	A/N-Counter
0	0	0	0	0	0	1	0	02	R-Counter
0	0	0	0	0	0	1	1	03	for future use
1	0	0	0	0	0	0	0	80	Status-Register

8.13.3 Bus Data Format

I²C-bus write mode

Bit	Function
STA	
1	MSB
1	**CHIP ADDRESS** (WRITE)
0	
0	
0	
CAS2	
CAS1	
0	LSB
ACK	
S7	MSB
S6	**SUB ADDRESS** (WRITE) 00H...03H
S5	
S4	
S3	
S2	
S1	
S0	LSB
ACK	
DX	MSB
...	**DATA_IN** X...0 (X=7, 15 or 23)
D5	
D4	
D3	
D2	
D1	
D0	LSB
ACK	
STO	

I²C-bus read mode

Bit	Function
STA	
1	MSB
1	**CHIP ADDRESS** (WRITE)
0	
0	
0	
CAS2	
CAS1	
0	LSB
ACK	
1	MSB
0	**SUB ADDRESS** (READ) 80H
0	
0	
0	
0	
0	
0	LSB
ACK	
STA	restart
1	MSB
1	**CHIP ADDRESS** (READ)
0	
0	
0	
CAS2	
CAS1	
1	LSB
ACK	
DX	MSB
...	**DATA_OUT FROM SUB ADD** X...0 (X=7)
D5	
D4	
D3	
D2	
D1	
D0	LSB
1	
STO	

3W-bus write mode

Bit	Function
S7	MSB
S6	**SUB ADDRESS** (WRITE) 00H...03H
S5	
S4	
S3	
S2	
S1	
S0	LSB
DX	MSB
...	**DATA_IN** X...0 (X=7, 15 or 23)
D5	
D4	
D3	
D2	
D1	
D0	LSB

3W-bus read mode

Bit	Function
S7	MSB
S6	**SUB ADDRESS** (READ) 80H
S5	
S4	
S3	
S2	
S1	
S0	LSB
DX	MSB
...	**DATA_OUT FROM SUB ADD** X...0 (X=7)
D5	
D4	
D3	
D2	
D1	
D0	LSB

8.13.4 Data Byte Specification

Register 00 Subaddress 00H Control - Register	
Bit	Function
MSB D7	Test-Mode / Normal-Mode
D6	Test-Modes (in/out) LockDetect (on/off)
D5	LockDetect-Out on Port 0 / 2
D4	Phase Detector polarity (+/-)
D3	ChargePump current 100/500µA ,1/2mA
D2	
D1	Charge Pump (on/off)
D0 LSB	Loop filter OP (on/off)

Register 01 Subaddress 01H A/N-Counter,Ports,VCO		
Bit	Function	
MSB D23	GHz VCO Switch	
D22	Prescaler Switch 32/33 <--> 64/65	
D21	$N1_2$	N-Counter GHz-PLL
D20	$N0_2$	
D19	Port 1	
D18	Port 0	
D17	2^{10}	divide ratio of the synthesizer N-Counter 2 2047
D16	2^9	
D15	2^8	
D14	2^7	
D13	2^6	
D12	2^5	
D11	2^4	
D10	2^3	
D9	2^2	
D8	2^1	
D7	2^0	
D6	2^6	divide ratio of the synthesizer A-Counter 0 127
D5	2^5	
D4	2^4	
D3	2^3	
D2	2^2	
D1	2^1	
D0 LSB	2^0	

Register 02 Subaddress 02H R-Counter,Ports,VCO		
Bit	Function	
MSB D15	not used (must be=0)	
D14	Base band amplifier disable	
D13	$R1_2$	R-Counter GHz-PLL
D12	$R0_2$	
D11	not used	
D10	Port 2	
D9	2^9	divide ratio of the synthesizer R-Counter 2 1023
D8	2^8	
D7	2^7	
D6	2^6	
D5	2^5	
D4	2^4	
D3	2^3	
D2	2^2	
D1	2^1	
D0 LSB	2^0	

Register 03 Subaddress 03H for future use	
Bit	Function
MSB D7	-
D6	-
D5	-
D4	-
D3	-
D2	-
D1	-
D0 LSB	-

Register 80 Subaddress 80H Status - Register (READ)	
Bit	Function
MSB D7	LockDetect-Out
D6	for future use all bits high
D5	
D4	
D3	
D2	
D1	
D0 LSB	

Control-Register (Register 00) ---> Subaddress 00H			
Bit			Function
MSB D7	0		Normal-Mode
	1		Test-Mode
D6	D7 must be = 1 (Test-Mode)		
	0		R-counter / 2 -> output to Port P0 N-counter / 2 -> output to Port P1
	1		Port P0 -> input to R-counter Port P1 -> input to N-counter
	D7 must be = 0 (Normal-Mode)		
	0		Bit D5 not active
	1		Bit D5 active
D5	D5 is only active for D6 = 1, D7 = 0		
	0		LockDetect output on Port 0
	1		LockDetect output on Port 2
D4	0		PhaseDetector polarity negative
	1		PhaseDetector polarity positive
D3 D2	D3	D2	Synthesizer ChargePump current
	0	0	100µA
	0	1	500µA
	1	0	1mA
	1	1	2mA
D1	0		Synthesizer ChargePump disabled
	1		Synthesizer ChargePump enabled
D0 LSB	0		Synthesizer Loopfilter OP disabled
	1		Synthesizer Loopfilter OP enabled

Test-Mode:

It is possible to switch into an internal chip test mode by bit D7 of the control register (subaddress 00H). If test mode is activated there are two test options available by bit D6 of the control register:

D6 = 0 --> Test-Mode1:
In this case the output frequencies of the counters divided by 2 (!) are put out to the Ports P0 (R-counter output frequency / 2) and P1 (N-counter output frequency / 2) Nevertheless the phase detector and the charge pump are in function (lock detector = OFF).

D6 = 1 --> Test-Mode2:
In this case the phase detector, charge pump and lock detector (= ON) can be tested by external frequencies which are applied to the Ports P0 (path of the R-counter frequency) and P1 (path of the N-counter frequency). (Note: LD_out only on port P2 visible!)

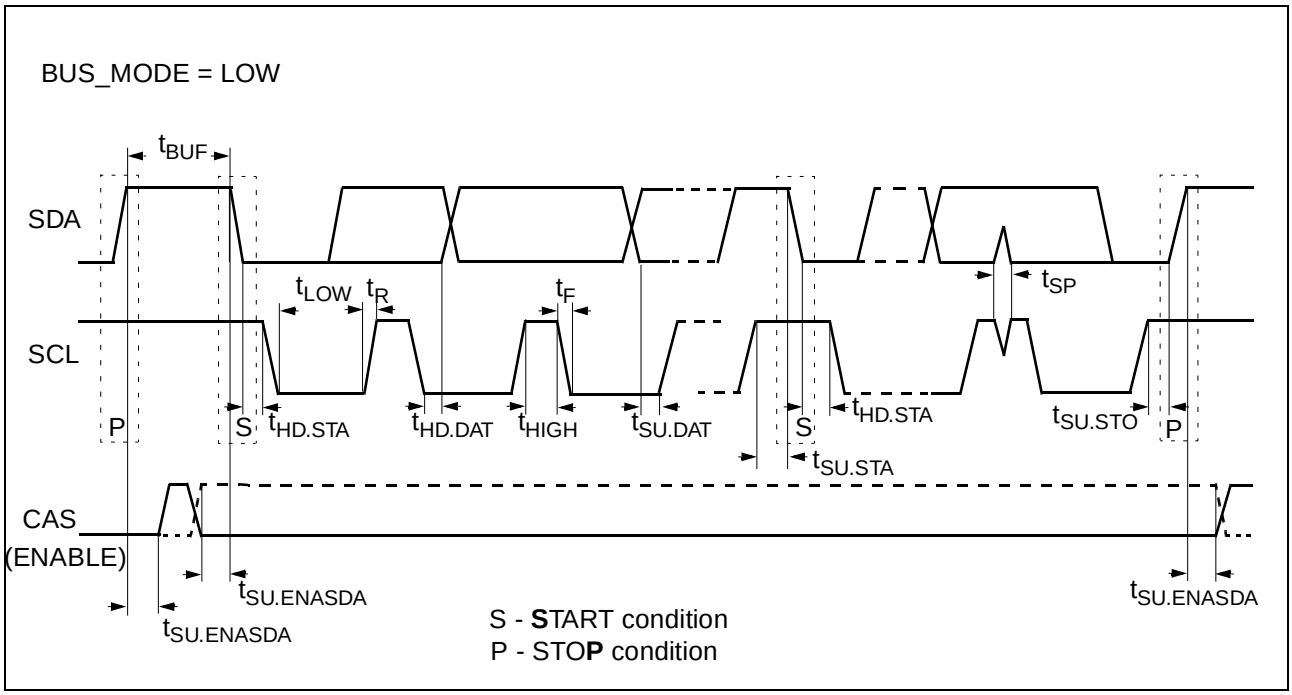
Status-Register (READ) (Register 128) ---> Subaddress 80H		
Bit		Function
MSB D7	0	synthesizer PLL unlocked
	1	synthesizer PLL locked
D6	1	for future use, all bits = 1
.....	1	
D0 LSB	1	

Prescaler, Ports, GHz-PLL (Register 01) ---> Subaddress 01H			
Bit			Function
MSB D23	0		GHz VCO = 3.4-6.2 GHz
	1		GHz VCO = 6-8.6 GHz
D22	0		Prescaler divide ratio 32/33
	1		Prescaler divide ratio 64/65
D21 D20	D21	D20	N-Counter GHz-PLL
	0	0	: 3
	0	1	: 4
	1	0	: 2
	1	1	: 3
D19	0		Port_1 output = low level
	1		Port_1 output = high level
D18	0		Port_0 output = low level
	1		Port_0 output = high level

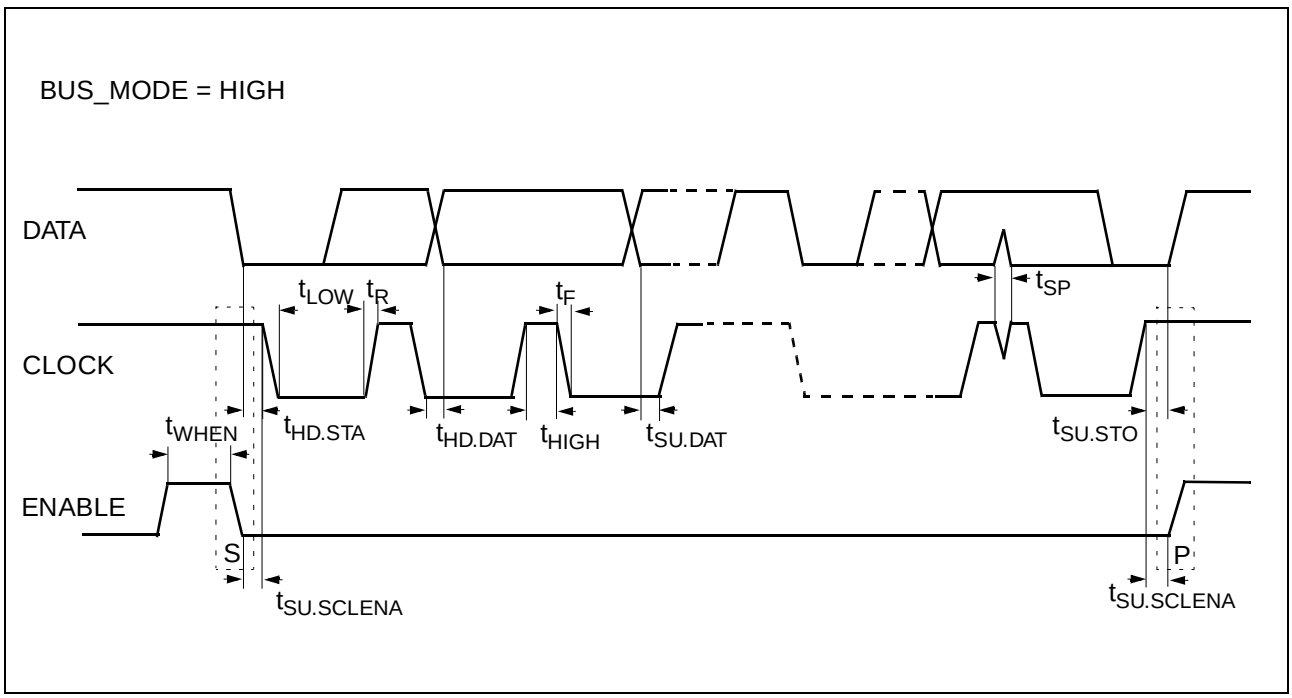
Ports, GHz-PLL (Register 02) ---> Subaddress 02H			
Bit			Function
MSB D15	0		not used (must be=0)
D14	0		base band amplifier enabled
	1		base band amplifier disabled
D13 D12	D13	D12	R-Counter GHz-PLL
	0	0	: 3
	0	1	: 4
	1	0	: 2
	1	1	: 3
D11	0		-
	1		-
D10	0		Port_2 output = low level
	1		Port_2 output = high level

8.13.5 Bus Timing

I²C Bus



3W-Bus



Parameter see also *I²C and 3-Wire-bus on page 26*	Symbol	Limit Values		Unit
		min.	max.	
LOW level input voltage (DATA, CLOCK, ENABLE, BUS_MODE)	V_{IL}	-0.5	0.96	V
HIGH level input voltage (DATA, CLOCK, ENABLE, BUS_MODE)	V_{IH}	2.24	5.5	V
Hysteresis of Schmitt trigger inputs	V_{Hys}		1.12	V
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
LOW level output voltage (DATA), only I2C-bus at 3mA sink current at 6mA sink current	V_{OL}	0	0.4 0.6	V
Output fall time from $V_{IH\ min}$ to $V_{IL\ max}$ with a bus capacitance from 10pF to 400pF with up to 3mA sink current at V_{OL}	t_{OF}	$20+0.1C_b$ 1)	250	ns
SCL clock frequency	f_{SCL}	0	400	kHz
Bus free time between a STOP and START condition 2)	t_{BUF}	1.3	--	µs
Hold time (repeated) START condition. After this period, the first clock pulse is generated. 2)	$t_{HD.STA}$	0.6	--	µs
LOW period of the SCL clock	t_{LOW}	1.3	--	µs
HIGH period of the SCL clock	t_{HIGH}	0.6	--	µs
Set-up time for a repeated START condition 2)	$t_{SU.STA}$	0.6	--	µs
Data hold time	$t_{HD.DAT}$	0		ns
Data set-up time	$t_{SU.DAT}$	100	--	ns
Rise time, fall time of SDA and SCL signals	t_R, t_F	$20+0.1C_b$1)	300	ns
Set-up time for STOP condition 2)	$t_{SU.STO}$	0.6	--	µs
Setup time BUS_ENA to SDA 2)	$t_{SU.ENASDA}$	0.6	--	µs
Setup time CLOCK to BUS_ENA 3)	$t_{SU.SCLENA}$	0.6	--	µs
H-pulse width (BUS_ENA) for new data protocol 3)	t_{WHEN}	0.6	--	µs
Capacitive load for each bus line	C_b	--	400	pF

1) C_b= capacitance of one bus line in pF
Note that the maximum t_F for the SDA and SCL bus lines quoted in table above (300ns) is longer than the specified maximum t_{OF} for the output stages (250ns).This allows series protection resistors to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_F.

2) only for I²C bus mode

3) only for I²C bus mode

9 Electrical Characteristics

9.1 Absolute Maximum Ratings

The maximal ratings may not be exceeded under any circumstances, not even momentary and individual, as permanent damage to the IC will result.

Parameter	Symbol	Limit Values		Units
		min.	max.	
Supply voltage	V_{VCC}	- 0.3	5.5	V
Supply voltage 1	V_{VCC1}	- 0.3	5.5	V
Crystal oscillator	V_{QOSZ}	V_{VCC}-3 > 0	V_{VCC}-1 > 0	V
Crystal oscillator buffered output	$V_{XTALOUT}$	0	V_{VCC}	V
Synthesizer Charge pump out Loop filter in	V_{PDLOOP}	0	V_{VCC}	V
Synthesizer Loop filter tuning output	V_{TUNE}	- 0.3	35	V
VCO inputs	V_{OB1},V_{OB2}	0	V_{VCC}	V
Port outputs	$V_{P0,P1,P2}$	0	V_{VCC}	V
	$I_{P0,P1,P2}$		15	mA
	Σ $I_{P0,P1,P2}$		30	mA
Port outputs , $V_{P0,P1,P2} = V_{VCC}$, I=max	t $_{Imax}$		1	ms
GHz-PLL Charge pump out	V_{PDOUT}	0	V_{VCC}	V
Baseband outputs I / Q	$V_{IOUT\ ,\ QOUT}$	0	V_{VCC1}	V
	$I_{IOUT\ ,\ QOUT}$		4	mA
Baseband filtered inputs I / Q	V_{IFIN},V_{QFIN}	0	V_{VCC1}	V
Baseband filtered Output I / Q	$V_{IFOUT\ ,\ QFOUT}$	0	V_{VCC1}	V
	$I_{IFOUT\ ,\ QFOUT}$		4	mA
AGC voltage	V_{AGC}	0	V_{VCC1}	V
RF input	$V_{RFINX\ ,\ RFINY}$	0	1.5 < V_{VCC1}	V
I^2C / 3-Wire-Bus	SCL, SDA,CAS BUSMODE	- 0.3	V_{VCC}+0.3	V

All values are referred to ground (pin), unless stated otherwise.
All currents are designated according to the source and sink principle, i.e. if the device pin is to be regarded as a sink (the current flows into the stated pin to internal ground), it has a negative sign,
and if it is a source (the current flows from Vs across the designated pin), it has a positive sign.

Parameter	Symbol	Limit Values		Units
		min.	max.	
Absolute Maximum Ratings continued				
ESD-Protection pin 4, Tune[1)]	V_{ESD}	- 500	500	V
ESD-Protection all other bipolar pins 1)	V_{ESD}	- 1	1	kV
ESD-Protection all CMOS pins 1)	V_{ESD}	- 1	1	kV
Total power dissipation	P_{tot}		687.5	mW
Ambient temperature	T_A	- 20	see note	°C [2)]
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	- 40	150	°C
Thermal resistance junction case	R_{th}		2	K/W

1) all ESD tests done according to EIA/JESD22-A114-B (HBM incircuit test), as a single device incircuit contact discharge test.

2) The maximum ambient temperature dependends on the mounting conditions of the package.
Any application mounting must guarantee not to exceed the maximum junction temperature of 125 °C.
As reference the thermal resistance junction to case is given.

To reach a high ambient temperature, a good solution is a 2-layer PCB board with complete GND plane under the chip body and a 2nd complete layer ground plane. Additional the area under the chip body should be equipped with as many via holes as possible, solded to the 2nd layer. Not used pins should be solded to GND if possible (e.g. unused ports).

9.2 Operating Range

Within the operational range the IC operates as described in the circuit description.
The AC / DC characteristic limits are not guaranteed.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min	max		
Supply voltage	V_{VCC}	4.5	5.5	V	
Supply voltage 1	V_{VCC1}	4.5	5.5	V	
Difference between VCC...VCC1 and between GND...GND1	Δ V	-0.3	0.3	V	
Current consumption	$I_{vcc+vcc1}$		125	mA	
Input frequency range of mixer	f_{RFIN}	950	2150	MHz	
VCO frequency range	f_{VCO}	0.7	3	GHz	
Synthesizer Loop filter tuning output	V_{TUNE}	0.5	33	V	
Ambient temperature	T_A	- 20	see note	°C 2)	

9.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Parameter T_A = 25 °C,V_{VCC}, V_{VCC1} = 5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Power supply						
Total current consumption	I_{VCC}+I_{VCC1}		110	125	mA	R_L>1MΩ,C_L<1.5pf
RF input (950-2150MHz) symm. balanced signal (*see Input Mixer on page 5*) RF source impedance 50 Ω, balanced input, test circuit **see page 27**						
Input frequency	f_{RFIN}	950		2150	MHz	balanced
minimum input RF level	V_{RFIN}		-55	-50	dBm	balanced 1100 MHz
maximum input RF level	V_{RFIN}			-15	dBm	balanced 1100 MHz
Input impedance differential without any application	R_{RFIN}		15		Ω	f = 0.9 - 2.2 GHz see diagrams ***13.5*** and **page 38**
	L_{RFIN}		1.3		nH	
Input gain control range	Δ A	40	43	45	dB	V_{GAIN}=0.4...2.6V see diagrams ***13.4***
Internal mixer gain	Δ A	-10		30	dB	
VCO power present at RF input			- 60	- 50	dBm	f = R_2 / N_2 x f_{in}
LO power present at RF input			- 74	- 70	dBm	f = f_{in}
input compression point -1 dB		- 7	- 5		dBm	minimum gain
output compression point -1 dB		+ 13	+ 15		dBm	minimum gain,Vcc=5V
Input IP2		+ 28	+ 32		dBm	minimum gain
Input IP3		+ 1	+ 5		dBm	minimum gain
Output IP3		+ 21	+ 25		dBm	minimum gain
Noise Figure @1400 MHz	F		15	16	dB	maximum gain, SSB
Base band I / Q output, IOUT, QOUT, pin 19, 20 (*see Baseband Amplifier on page 5*)						
DC voltage	V_{IOUT} V_{QOUT}		2.15		V	R_L>1MΩ
DC quiescent current	I_{IOUT},I_{QOUT}		2.7		mA	R_L>1MΩ
Baseband I/Q output voltage	V_{IOUT} V_{QOUT}		225	1000	mV_{pp}	R_L>1MΩ
Baseband I/Q output bandwidth both amplifiers in series see diagrams ***13.1*** and ***13.3***	$f_{-0.1\ dB}$	25	35		MHz	no filter, IOUT-IFIN 47nF QOUT-QFIN 47nF
	$f_{-1\ dB}$		70		MHz	
Baseband I/Q output flatness	Δ A		0.05	0.1	dB	up to 25 MHz
Quadrature error, phase	Δ Φ		1	3	deg	balanced @ 1100 MHz RFin= -35 dBm, test circuit **see page 27**
Quadrature error, gain	Δ A		1	2.5	dB	
Internal amplifier gain	A		16		dB	internal from mixer output to I / Q OUT
Baseband I/Q output impedance	R_{IOUT}, R_{QOUT}			50	Ω	dynamic resistance

Parameter T_A = 25 °C, V_{VCC}, V_{VCC1} = 5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
I / Q base band filtered input signal IFIN, QFIN, pin 15, 17 (*see Baseband Amplifier on page 5*)						
DC voltage	V_{IFIN},V_{QFIN}		2.1		V	see filter on *page 33*
Baseband I/Q input impedance	$R_{IFIN,QFIN}$		18		kΩ	see diagrams ***13.8***
Base band I / Q output filtered, IFOUT, QFOUT, pin 13, 14 (*see Baseband Amplifier on page 5*), symm. balanced input application						
DC voltage	V_{IFOUT} V_{QFOUT}		2.1		V	R_L>1MΩ
DC quiescent current	I_{IFOUT} I_{QFOUT}		2.7		mA	R_L>1MΩ
Baseband I/Q output voltage	V_{IFOUT} V_{QFOUT}		1	3.5	V_{pp}	R_L>1MΩ
Base band I/Q output bandwidth both amplifiers in series see diagrams ***13.1*** and ***13.3***	$f_{-0.5\,dB}$	20	22		MHz	no filter,15pf/1kΩ load IOUT-IFIN 47nF QOUT-QFIN 47nF
	$f_{-1\,dB}$	27	30		MHz	
Amplifier gain	A		16		dB	$V_{I,QFOUT}$ / $V_{I,QFIN}$
Group delay variation, see ***13.2*** both amplifiers in series	Δ t	-250		250	ps	100kHz 100MHz
Baseband I/Q output impedance	R_{IFOUT}, R_{QFOUT}			50	Ω	dynamic resistance
S/N @ 45 Mbaud	IFOUT,QFOUT	24	26		dB	maximum gain, 1Vpp
S/N @ 45 Mbaud	IFOUT,QFOUT	30	32		dB	minimum gain, 1Vpp
AGC voltage input (*see Input Mixer on page 5*)						
Gain control range	ΔV_{GAIN}	0.4		2.6	V	see diagrams ***13.4***
Gain control input impedance	R_{GAIN}	100	100e6		MΩ	
Gain control input clamp voltage	$V_{GAINmax}$		3.75		V	protected by resistor
Gain control input clamp current	$I_{GAINmax}$		180	500	µA	V_{GAIN} = Vcc1
Synthesizer Phase detector Charge pump output / Loop filter input (*see Synthesizer Loop filter on page 6*)						
DC voltage	V_{PDLOOP}		1.8		V	locked
DC current	I_{PDLOOP}	0.1		2	mA	see *Control-Register*
Tristate output current	I_{PDLOOP}		0.1	1	nA	V_{PDLOOP} = 2 V , guaranteed by design
Reference oscillator input / Crystal (*see Reference Oscillator on page 5*)						
DC voltage	V_{QOSZ}		3.4		V	
Crystal frequency	f	1	4	16	MHz	series resonance
Crystal resistance	f	10		100	Ω	series resonance
negative input impedance	Z_{QOSZ}	- 500	- 700	- 900	Ω	f = 4 MHz
Drive current	I_{QOSZ}		135		$µA_{rms}$	f = 16 MHz, Cs=18pF

Parameter T_A = 25 °C, V_{VCC}, V_{VCC1} = 5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Synthesizer Loop filter high voltage tuning output (*see Synthesizer Loop filter on page 6*)						
LOW output voltage	V_{TUNE}	0		0.5	V	I_{TUNE} = 1.5 mA
HIGH output current	I_{TUNE}	0		10	µA	V_{TUNE} = 33V
Synthesizer PLL (*see Synthesizer PLL on page 10*)						
N-counter divide ratio	N	2		2047		11-Bit, CMOS
A-counter divide ratio	A	0		127		7- Bit, CMOS
R-counter divide ratio	R	2		1023		10-Bit, CMOS
P-counter divide ratio	P	32/33		64/65		5/6-Bit, Bipolar
Equivalent phase noise at phase detector input, @ 1 kHz offset, within loop band width, 6 kHz loop BW, SSB			-164		$^{dBc}/_{Hz}$	Fref = 30 kHz
			-159		$^{dBc}/_{Hz}$	Fref = 100 kHz
			-158		$^{dBc}/_{Hz}$	Fref = 125 kHz
			-155		$^{dBc}/_{Hz}$	Fref = 250 kHz
			-149		$^{dBc}/_{Hz}$	Fref = 1000 kHz
Quadrature phase mismatch	$\Delta\Phi$		1	3	deg	
Total divide ratio [1)] see *see 8.12.3 on page 14*	M	992 4032		65.631 131.135		P=32/33 P=64/65
PLL tuning step size (programmable via R-counter) see *Register 02*	f_{ref}	0.9775 3.91 15.650	125	500 2000 8000 [2)]	kHz	$f_{crystal}$ = 1 MHz $f_{crystal}$ = 4 MHz $f_{crystal}$ = 16 MHz
Continuous step size see ***8.12.3*** (programmable via R-counter)	f_{ref}	32.759		957.66	kHz	P = 32/33 f_{in} = 950 - 2150 MHz
Continuous step size see ***8.12.3*** (programmable via R-counter)	f_{ref}	16.395		235.61	kHz	P = 64/65 f_{in} = 950 - 2150 MHz
Frequency range with continuous step size for P = 32/33	f	950 950 950 992 1984		1025 2050 2150 2150 2150	MHz	f_{ref} = 15.625 kHz f_{ref} = 31.250 kHz f_{ref} = 62.5 ...500 kHz f_{ref} = 1.000 MHz f_{ref} = 2.000 MHz
Frequency range with continuous step size for P = 64/65 [3)]	f	950 950 1008 2016		2048 2150 2150 2150	MHz	f_{ref} = 15.625 kHz f_{ref} = 31.25...166.7 kHz f_{ref} = 250 kHz f_{ref} = 500 kHz
R-counter values for 166.666 kHz step size	R		6 24 96			$f_{crystal}$ = 1 MHz $f_{crystal}$ = 4 MHz $f_{crystal}$ = 16 MHz

1) The minimum total divide ratio is only important for continuous frequency step size, if lower divide ratios are used not all frequencies are possible. To find out the missing frequencies our Windows control program for I^2C / 3-wire bus may be used.
2) Step sizes > 2 MHz are not guaranteed, 1 MHz continuous step size is only possible for RFin > 992 MHz
3) For low power dissipation the use of the 64/65 prescaler should be preferred if the desired step size fits

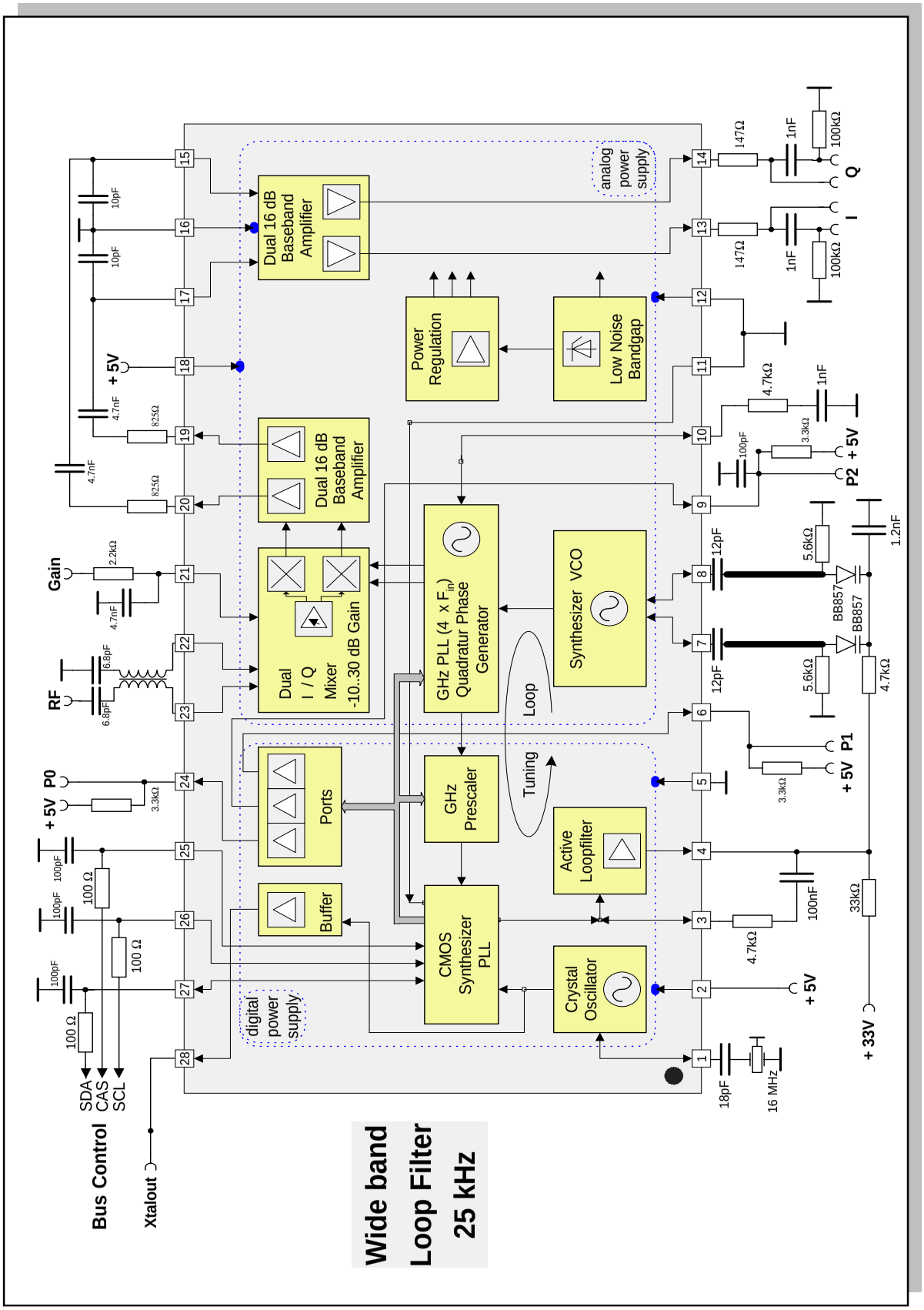
Parameter T_A = 25 °C, V_{VCC}, V_{VCC1} = 5V	Symbol	Limit Values			Unit	Test conditions
		min	typ	max		
Synthesizer VCO (*see Synthesizer VCO on page 6*)						
DC voltage	V_{OB1},V_{OB2}		1.9		V	
high side VCO frequency range	f_{VCO}	1900		2870	MHz	2 band split, *page 32*
high side VCO frequency range	f_{VCO}	1900		2910	MHz	3 band split, *page 32*
low side VCO frequency range	f_{VCO}	712		1076	MHz	2 band split, *page 32*
low side VCO frequency range	f_{VCO}	700		1075	MHz	3 band split, *page 32*
high side VCO frequency range	f_{VCO}	1424		2151	MHz	+VCO at f_{in}, band split
low side VCO frequency range	f_{VCO}	950		1434	MHz	+VCO at f_{in}, band split
Phase noise high side VCO[1)]		- 53	- 56	- 60	dBc	1 kHz offset, SSB
Phase noise high side VCO[1)]		- 73	- 76	- 80	dBc	10 kHz offset, SSB
Phase noise high side VCO[1)]		- 93	- 96	- 100	dBc	100 kHz offset, SSB

1) Note : This is the phase noise of the free running VCO, not for the overall system performance at baseband output. For detailed system phase noise information see diagrams *page 30* and *page 31* and our separate application note.

Port outputs, P0, P1, P2 (*see Output Ports on page 5*)						
Supply voltage	V_P	0		5.5	V	max. Vcc
LOW output voltage	V_P	0		0.5	V	I_P = 15 mA
LOW output current	I_P			15	mA	
HIGH output current	I_P	0		10	µA	V_P = 5 V
Port outputs, I=max	t_{Imax}			1	ms	$V_{P0,P1,P2}$=V_{VCC}
Crystal oscillator output (*see Crystal Oscillator Output on page 6*)						
Buffer output voltage [1)]	$V_{Xtalout}$		1.1		V_{pp}	R_L>1MΩ, Vcc=5V, C_L = 10 pF, f = 16 MHz
Buffer output current	$I_{Xtalout}$			1	mA	
Buffer output impedance	$R_{Xtalout}$		350		Ω	
I^2C and 3-Wire-bus Clock, Data, Enable, BUS_MODE (see *Bus Data Format on page 16* and *8.13.5 Bus Timing on page 19*)						
HIGH level input voltage	V_{IH}	2.24		V_{VCC}	V	
LOW level input voltage	V_{IL}	-0.5		0.96	V	
LOW level output voltage (DATA), only I2C-bus	V_{OL}	0		0.4 0.6	V	3mA sink current 6mA sink current
Hysteresis of Schmitt trigger inputs	V_{hys}	0.2	1		V	
H-input current	I_H			10	µA	V_I = V_{VCC} = 5.5V
L-input current	I_L	-60			µA	V_I = GND
Input capacity	C_I			5	pF	

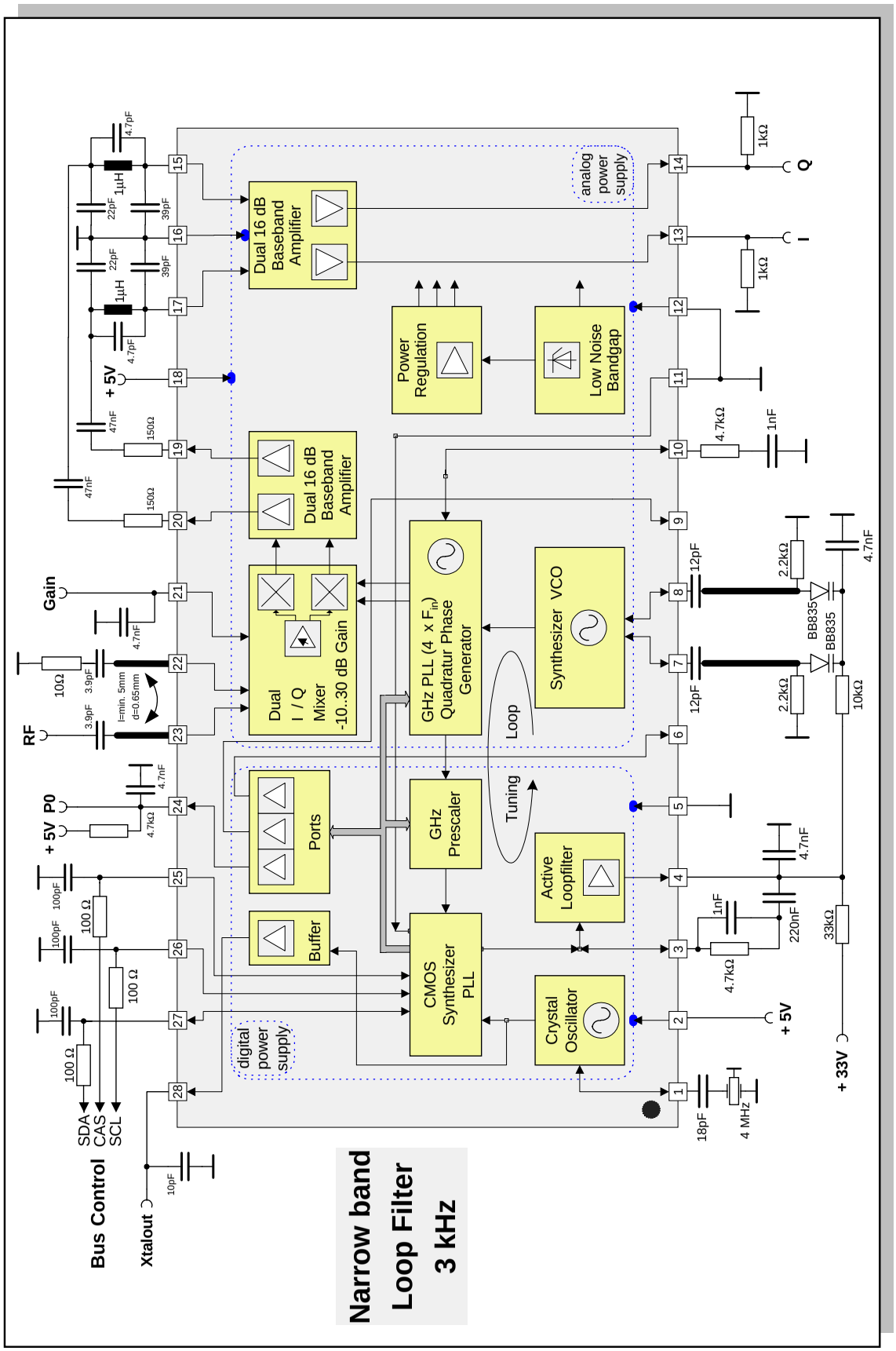
1) output voltage is dependant on Vcc

10 Test circuit

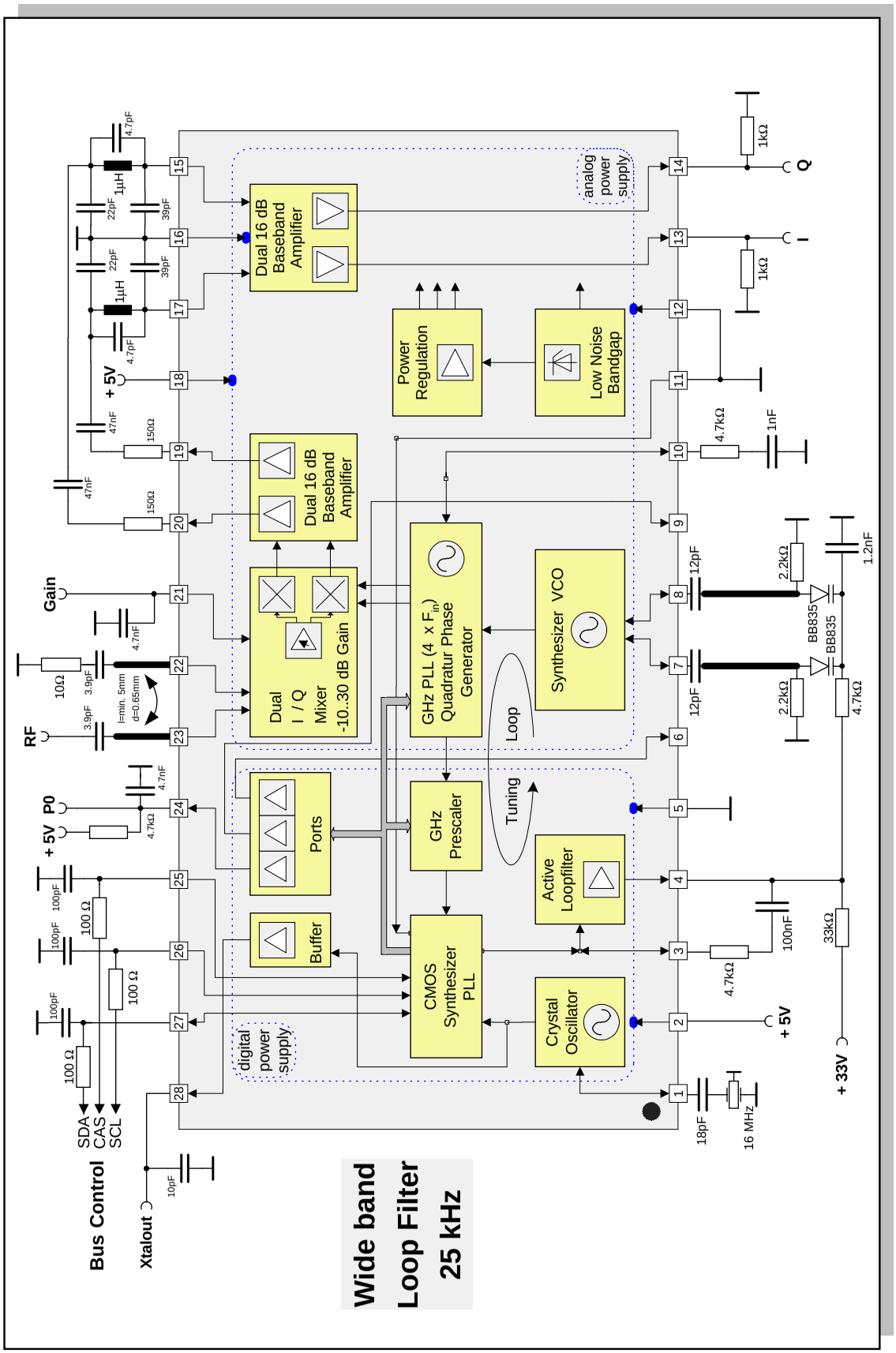


11 Application circuits

- **high side synthesizer VCO narrow band loop filter example**
  3 kHz typ.



- **high side synthesizer VCO wide band loop filter example**
  25 kHz typ.



- **Phase noise performance of application**

The over all system phase noise at base band of the TUA 6100 is strongly dependent on several parameter :
1.programming of the 2nd PLL (GHz-PLL setting of the R_2 and N_2 counter)
2.programming of the 1st synthesizer PLL
- receiving frequency (variation of the VCO steepness due to non linearity of the varicap),
- phase detector current,
- crystal frequency,
- step size = Fref,
- loop filter parameter. (bandwidth)

A well balanced phase noise over the whole tuning range requires an optimized parameter programming of the synthesizer PLL for each receiving frequency

- 1st you have to decide for the optimum loop filter bandwidth for your application.
Narrow band loop filter :
achieves better PLL outband phase noise at high frequencies offset but lower PLL inband phase noise at low frequency offset.
Wide band loop filter :
achieves better PLL inband phase noise at low frequencies offset but lower PLL outband phase noise at high frequency offset.

- 2nd you have to decide for the crystal frequency for your application.
Higher crystal frequency achieves better PLL inband phase noise.

- 3rd you have to decide for the varicap for your application.
Linear varicaps achieves better balanced phase noise than non linear varicaps.

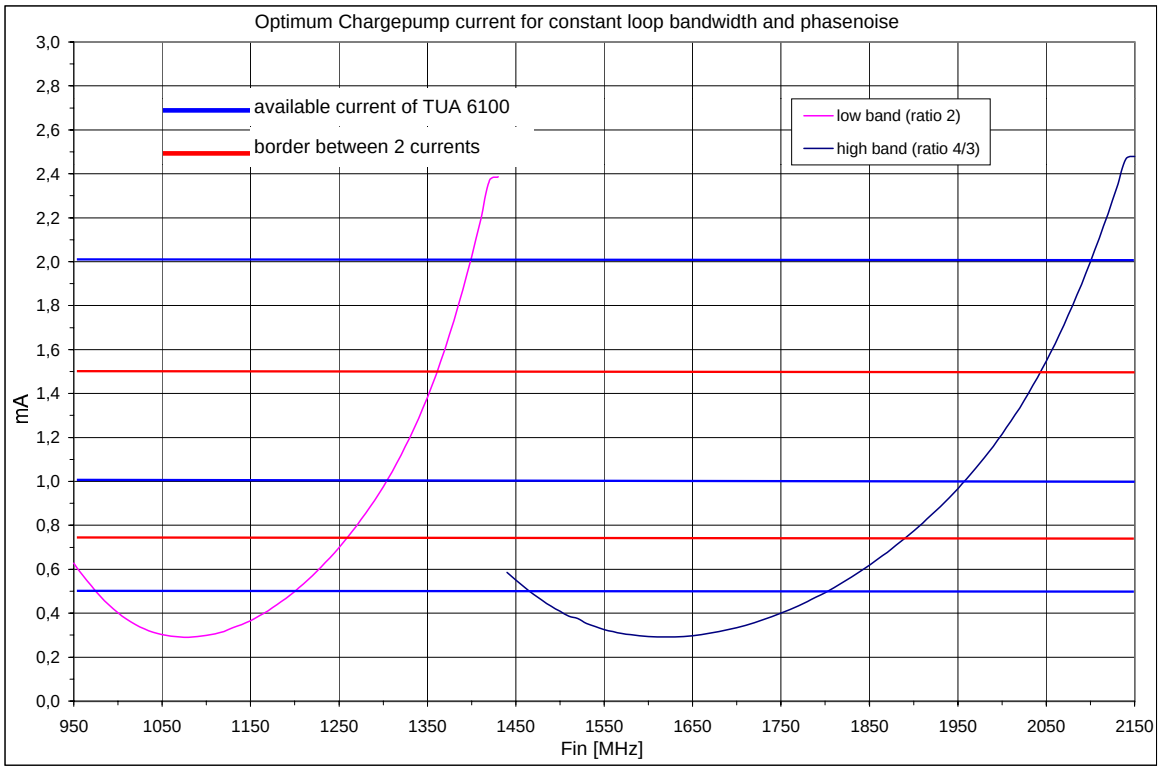
- 4th you have to decide for the main stepsize for your application.
Higher step size achieve better PLL inband phase noise.

- 5th during programming the desired receiving frequency you have to set step size and phase detector output current for each frequency. This is necessary to compensate the non linearity of the varicap.

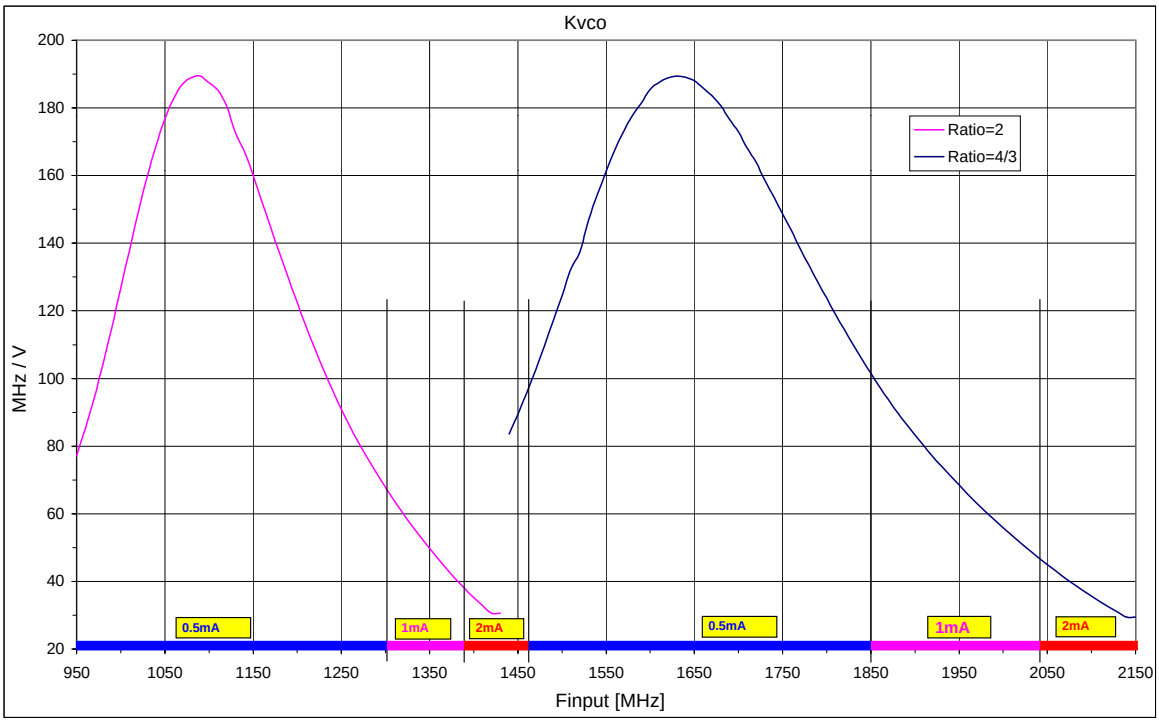
All this is done in our separate application note with the above two application circuits which obtain the following worst case phase noise values :					
Narrow band loop filter	3	3	3	3	kHz
Offset Frequency	1	10	100	1000	kHz
Measured phase noise at base band	- 55	- 76	- 98	- 100	dBc/Hz
Wide band loop filter	30	30	30	30	kHz
Offset Frequency	1	10	100	1000	kHz
Measured phase noise at base band	- 75	- 77	- 91	- 100	dBc/Hz

For detailed information see our separate application note version B5.

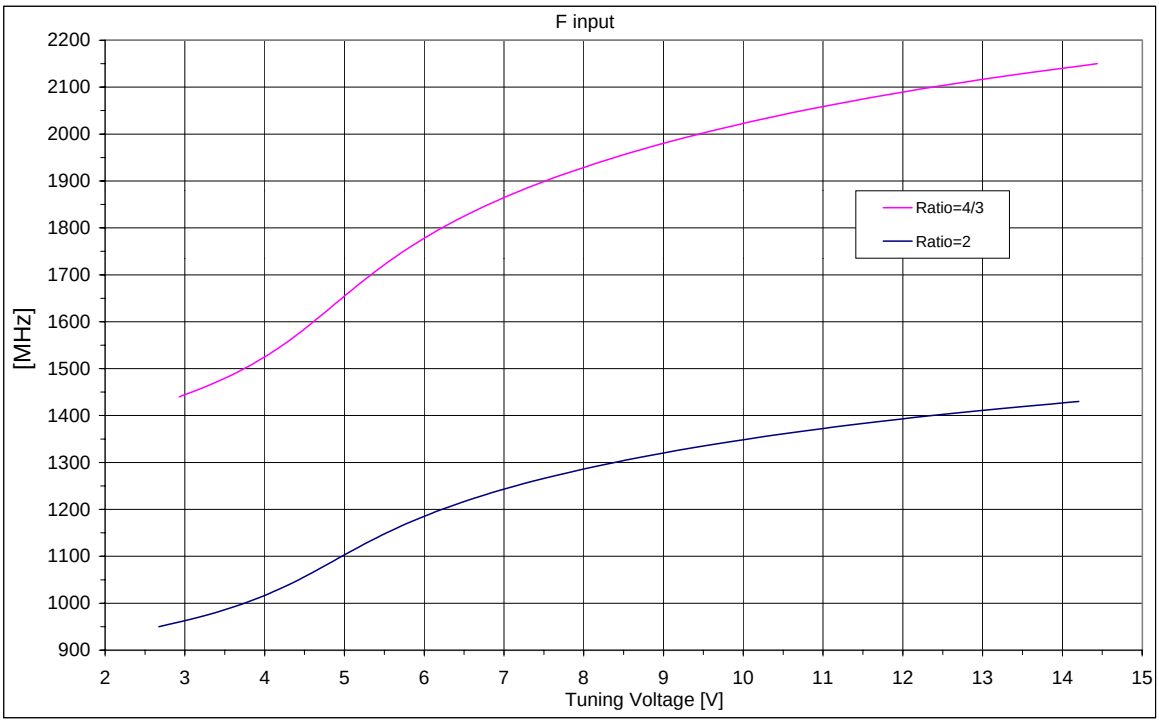
- **Optimum phase detector current**
  valid for the two applications above, band splitting into 2 ranges



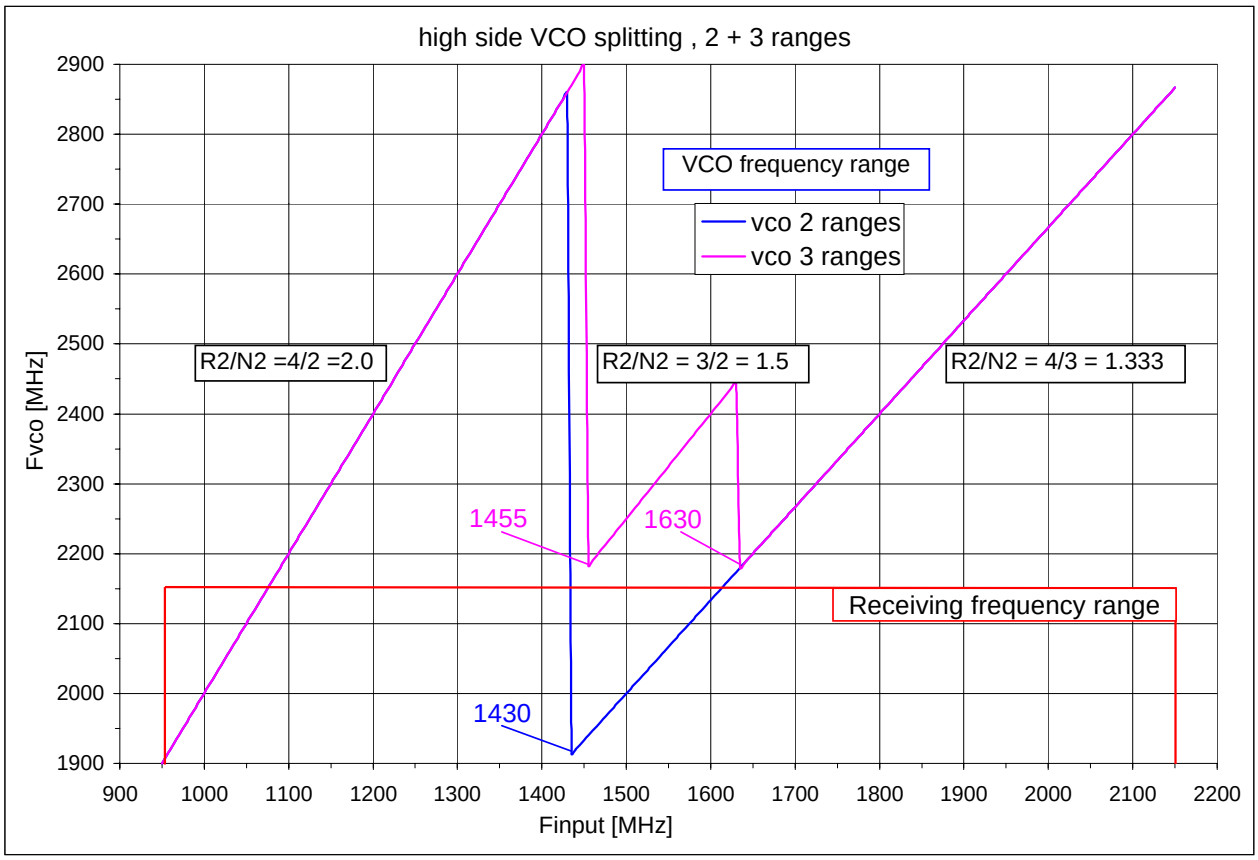
- **VCO steepness + phase detector current ranges**
  valid for the two applications above, band splitting into 2 ranges



- **VCO tuning voltage**
  valid for the two applications above, band splitting into 2 ranges

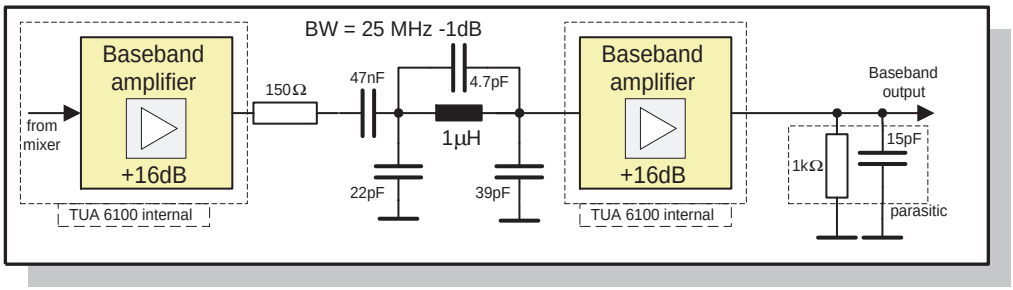


- **Receiving frequency band splitting into 2 or 3 ranges**
  3 band programming reduces the VCO pulling in the frequency range from 1430 to 1630 MHz

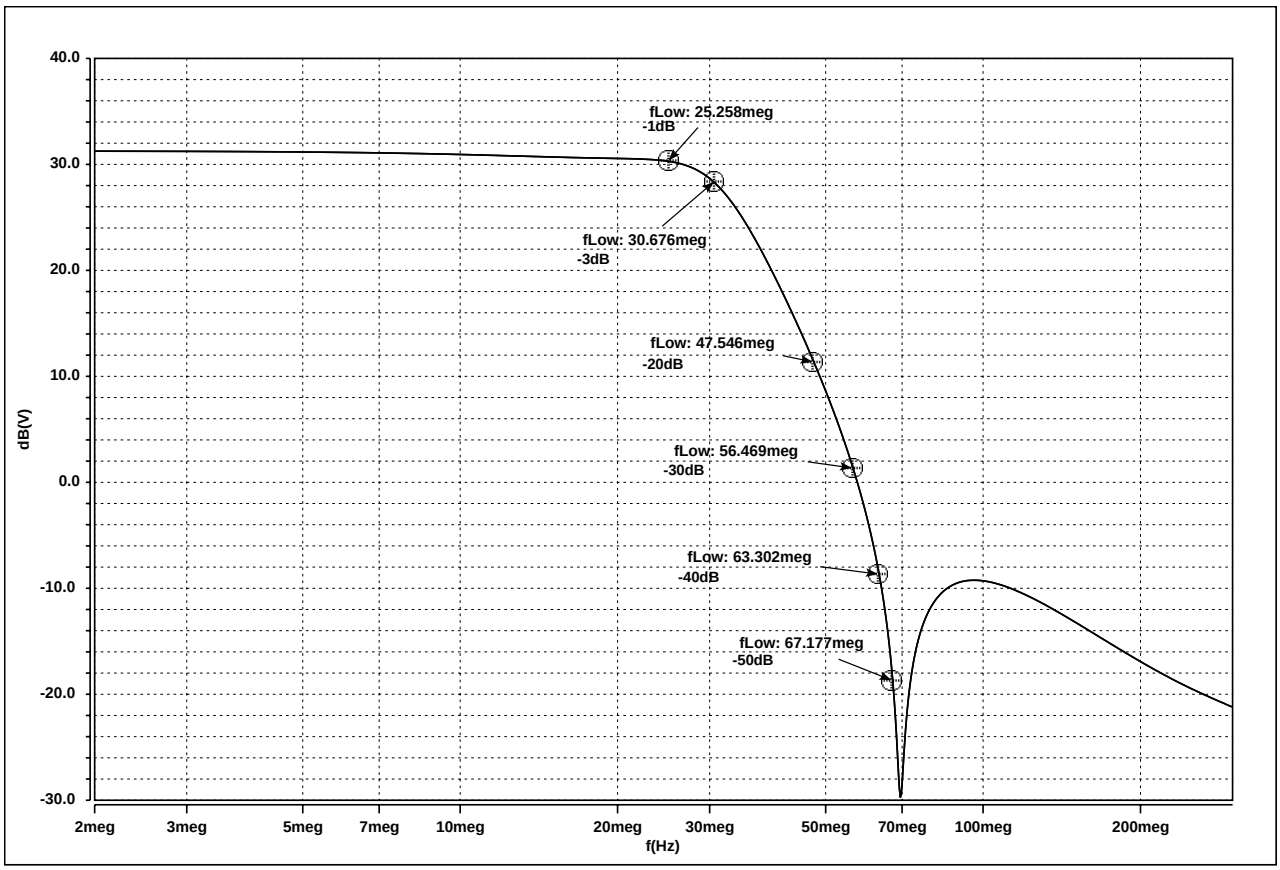


12 Base band filter

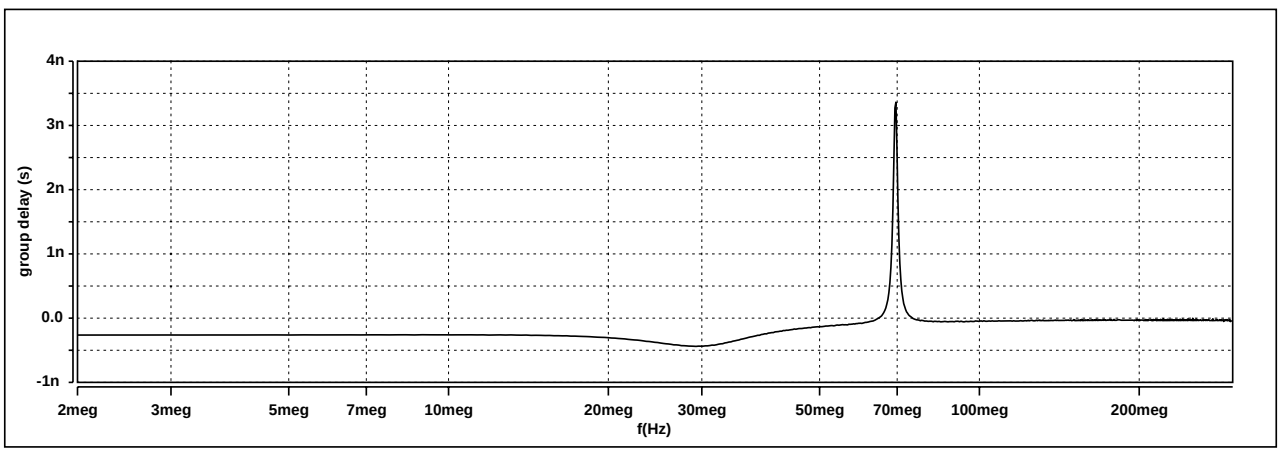
for 45 MBaud signals



- **Frequency response incl. the two base band amplifiers + output load**



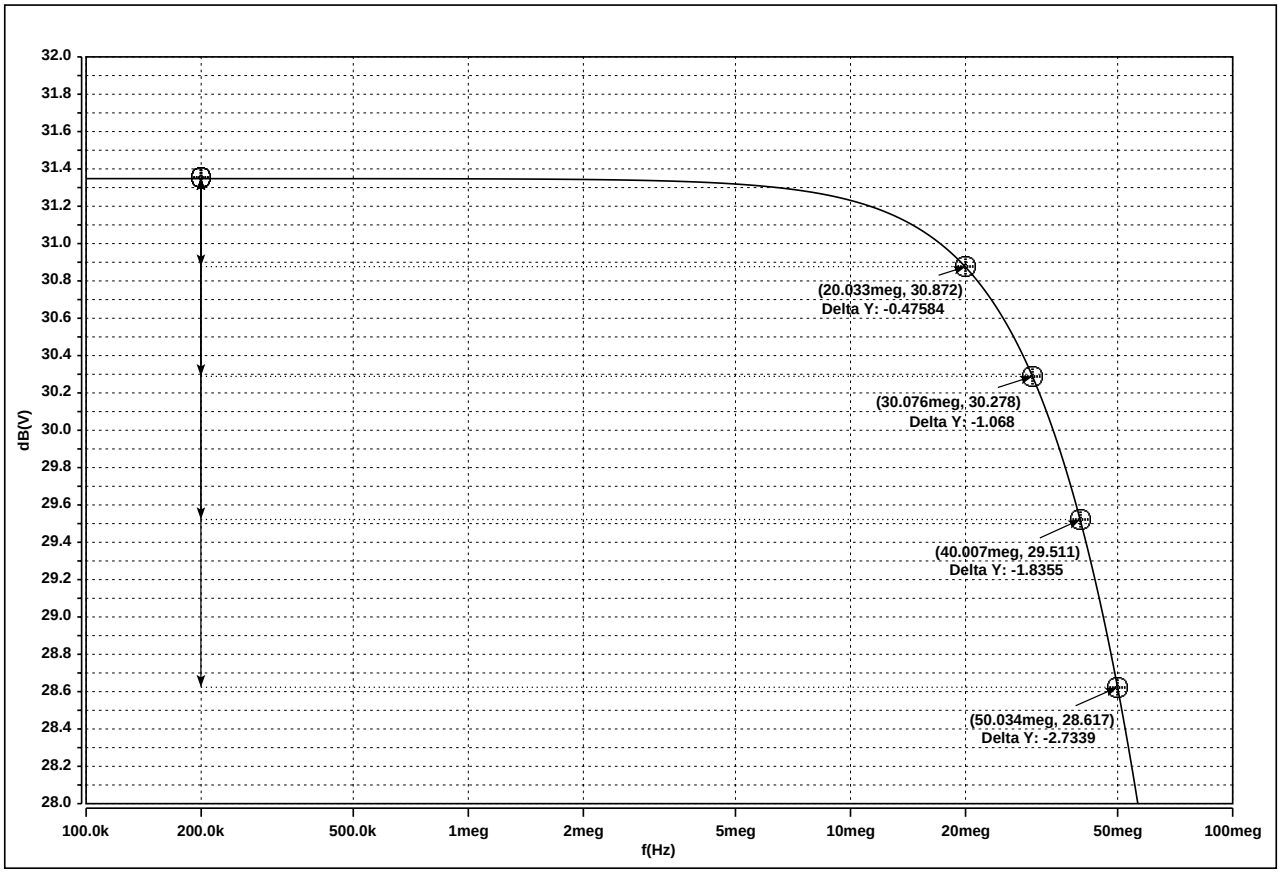
- **Group delay incl. the two +16 dB base band amplifiers + output load**



13 Electrical Diagrams

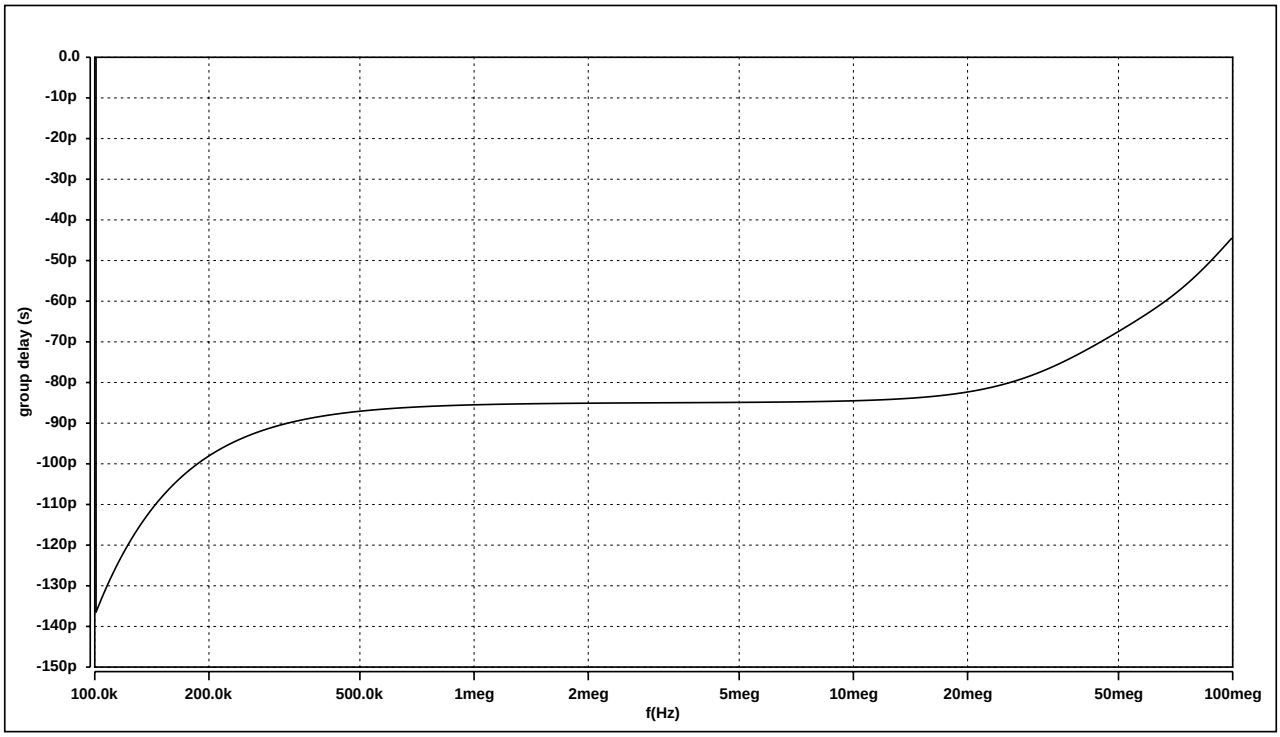
13.1 Frequency flatness of base band outputs

without base band filter, both base band amplifiers in series, coupling capacitor 47nF



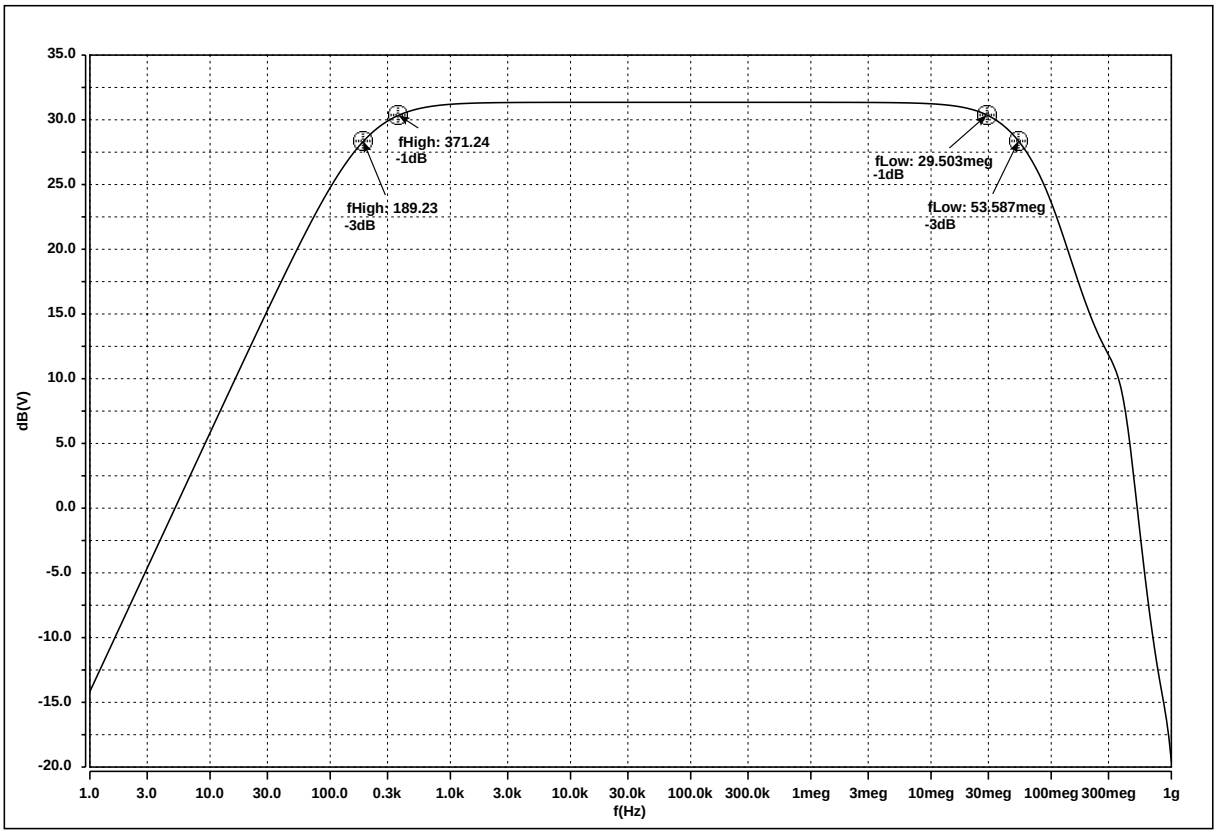
13.2 Group delay of base band outputs

without base band filter, both base band amplifiers in series, coupling capacitor 47nF

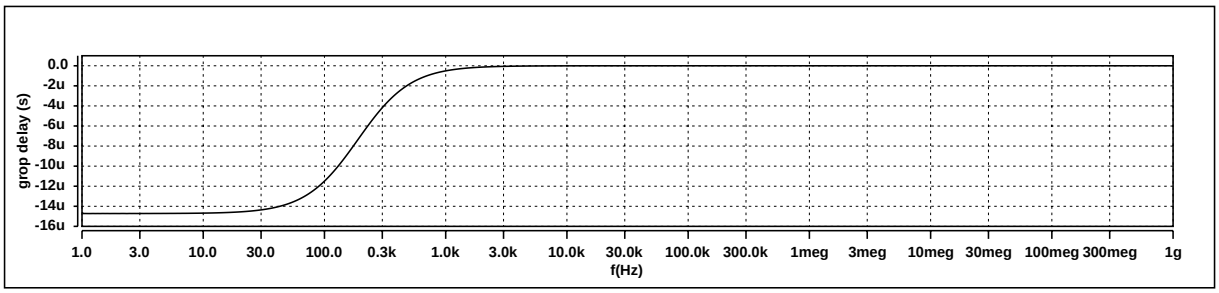


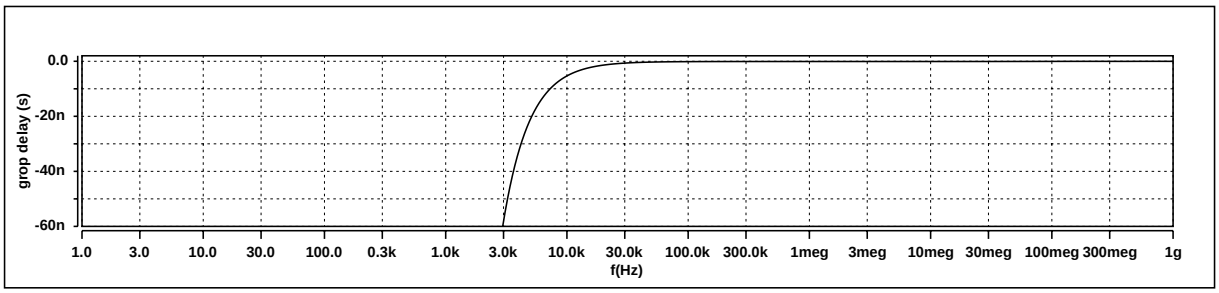
13.3 Frequency response of base band outputs

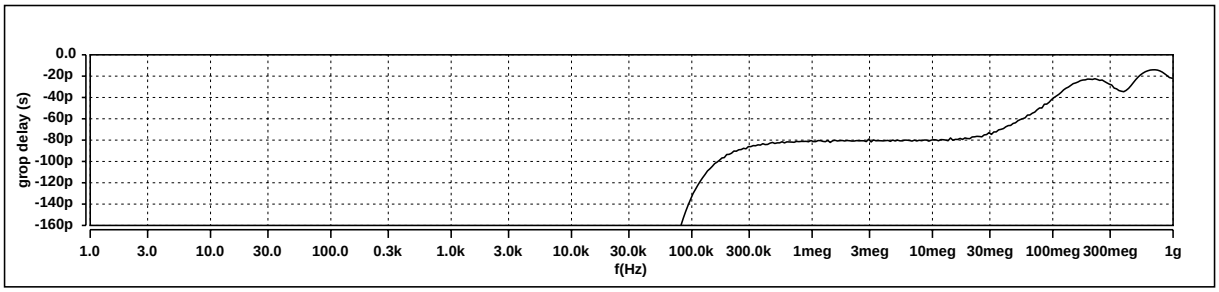
without base band filter, both base band amplifiers in series, coupling capacitor 47nF



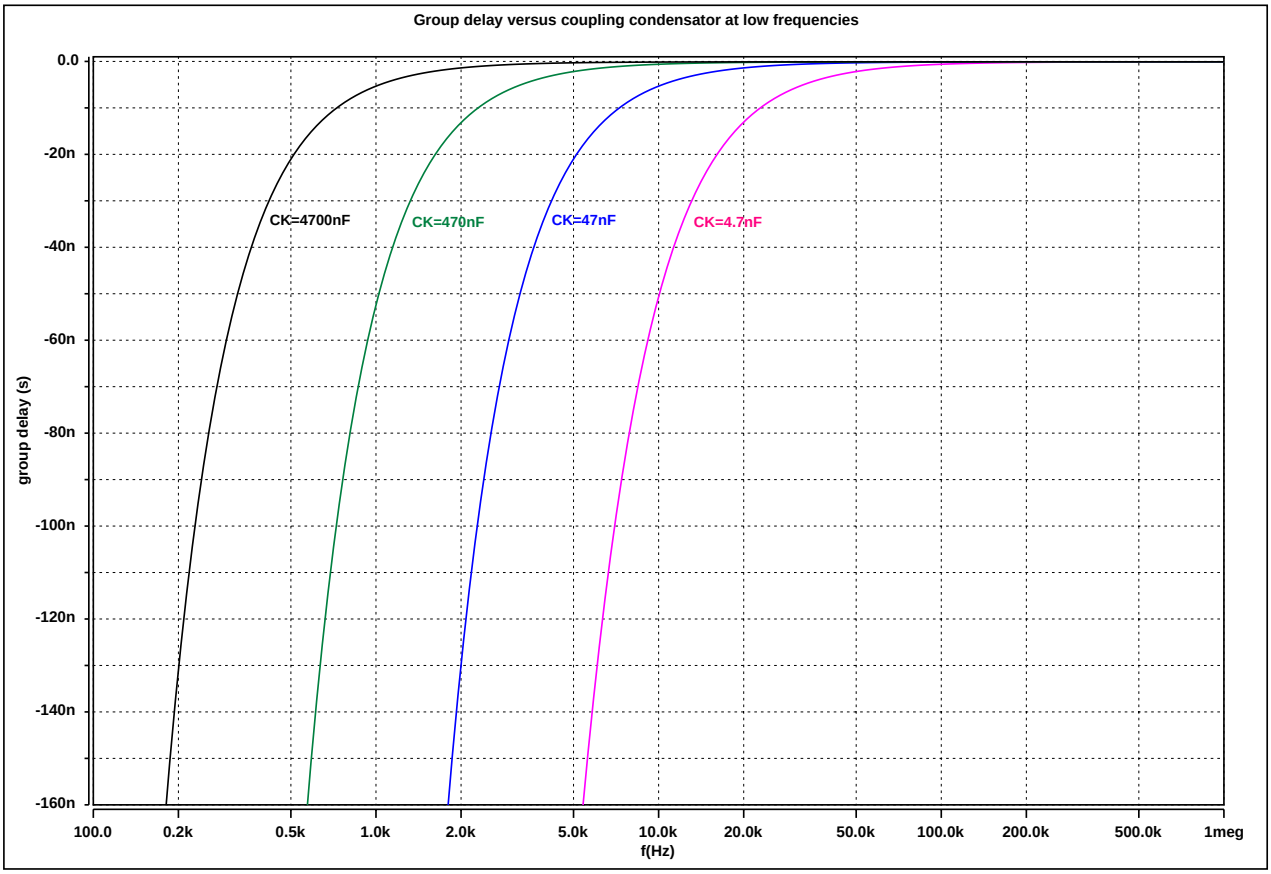
Group delay (coupling capacitor 47nF, low frequencies response is dependent on coupling capacitor**)**



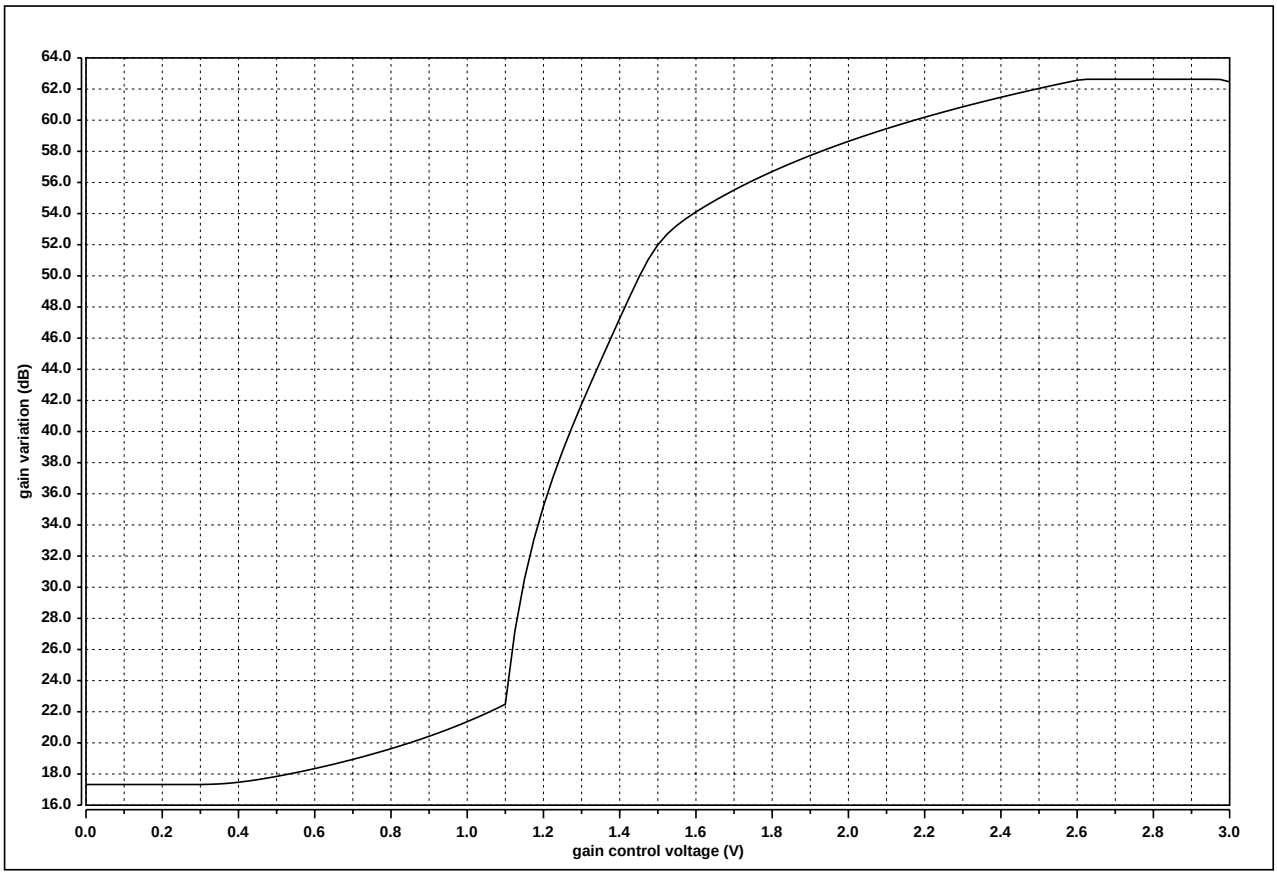




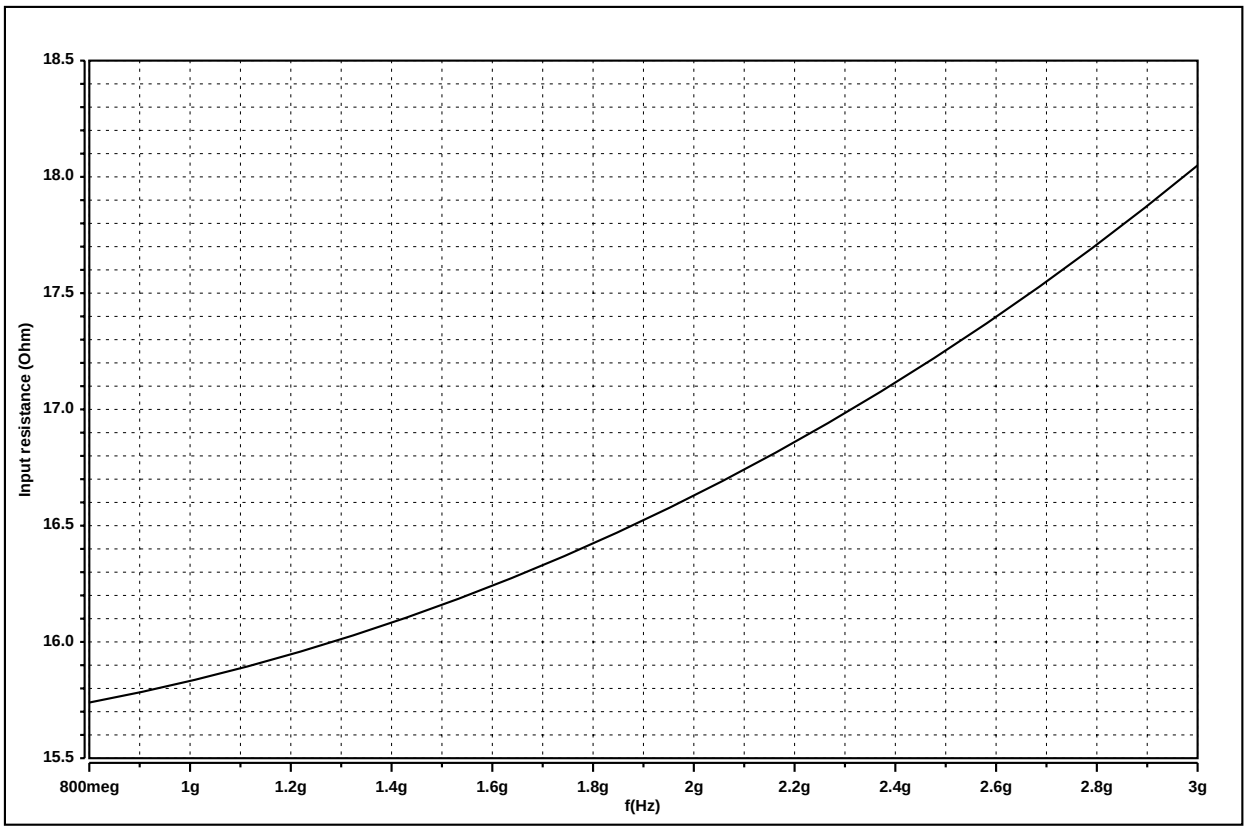
- **Group delay at low frequencies, dependent on coupling capacitor**

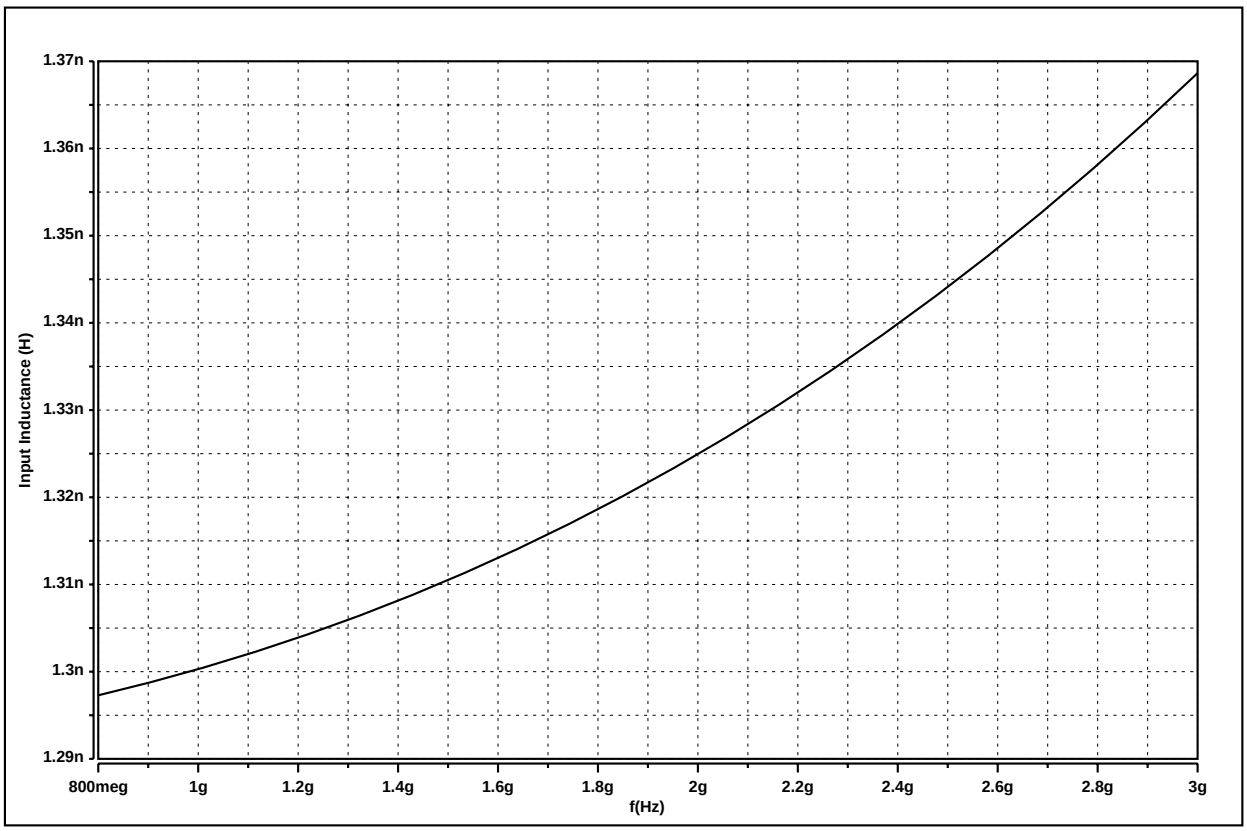


13.4 RF gain control range

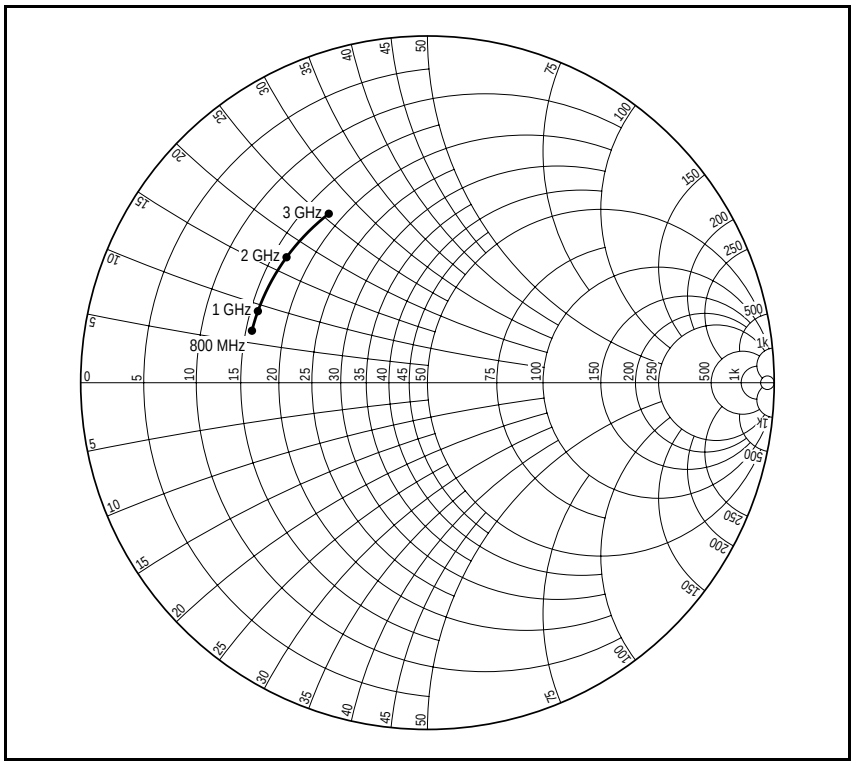


13.5 RF input impedance



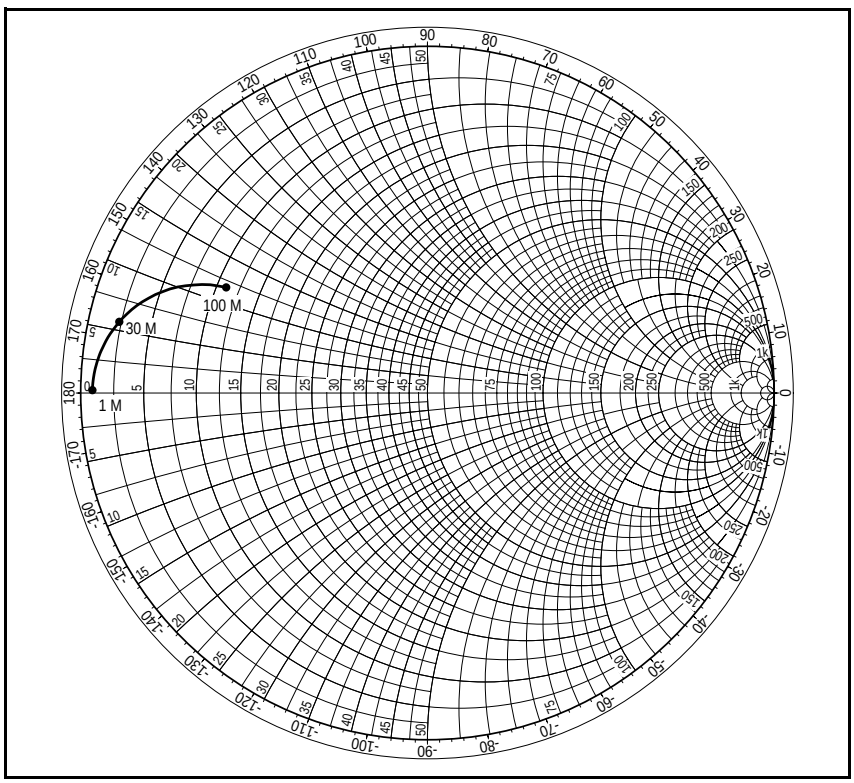


- **RF input impedance continued, Smith diagram**

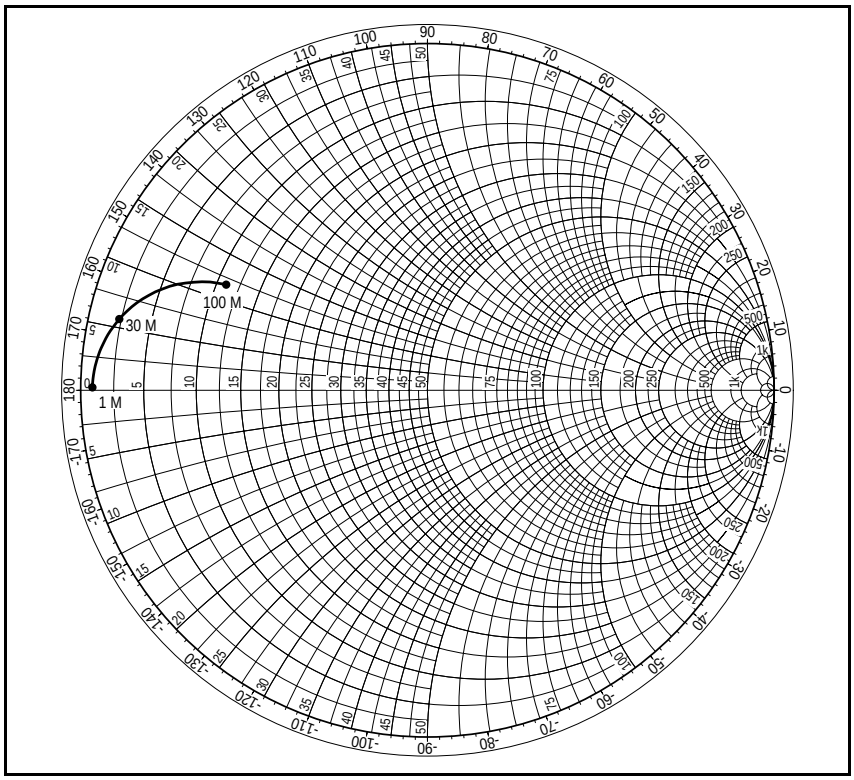


13.6 Base band output impedance pin 13, 14 (filtered), Smith diagram

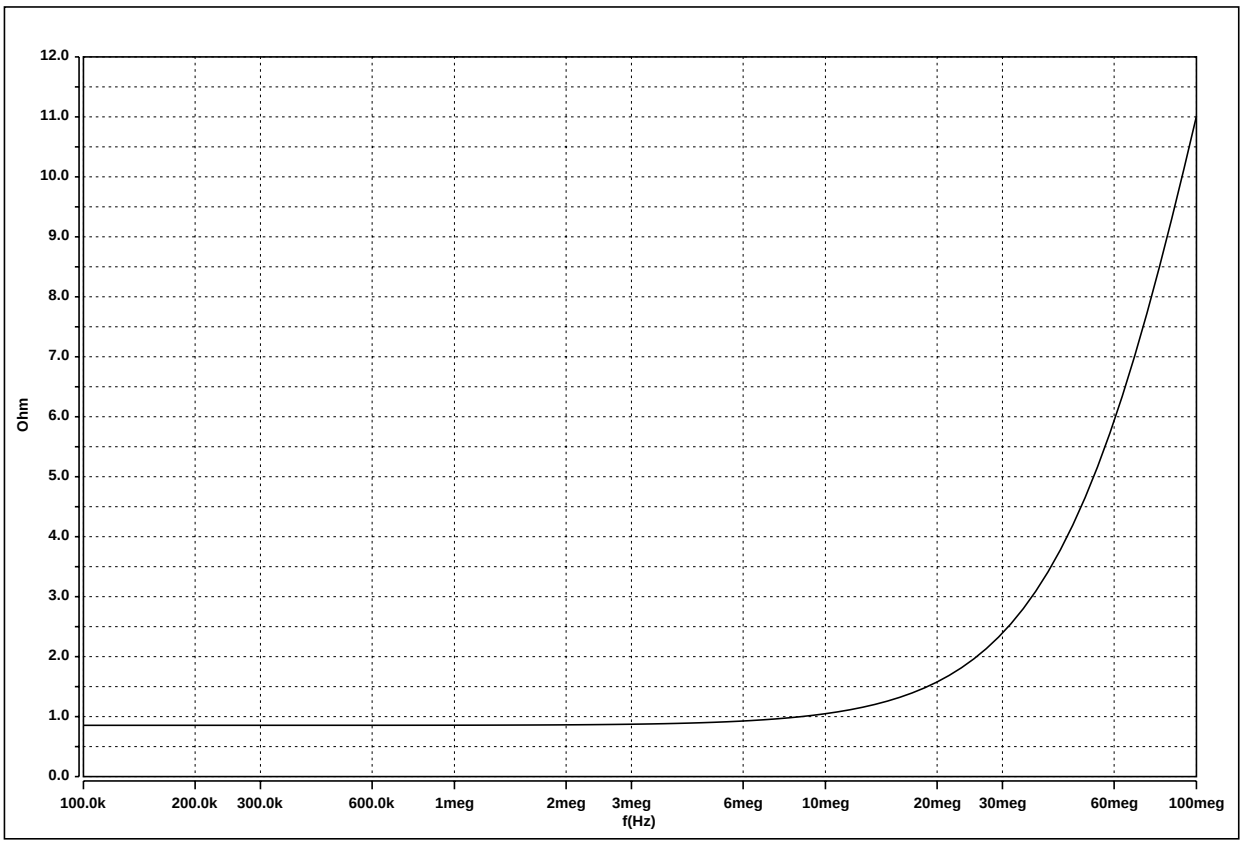
identical to pin 19, 20



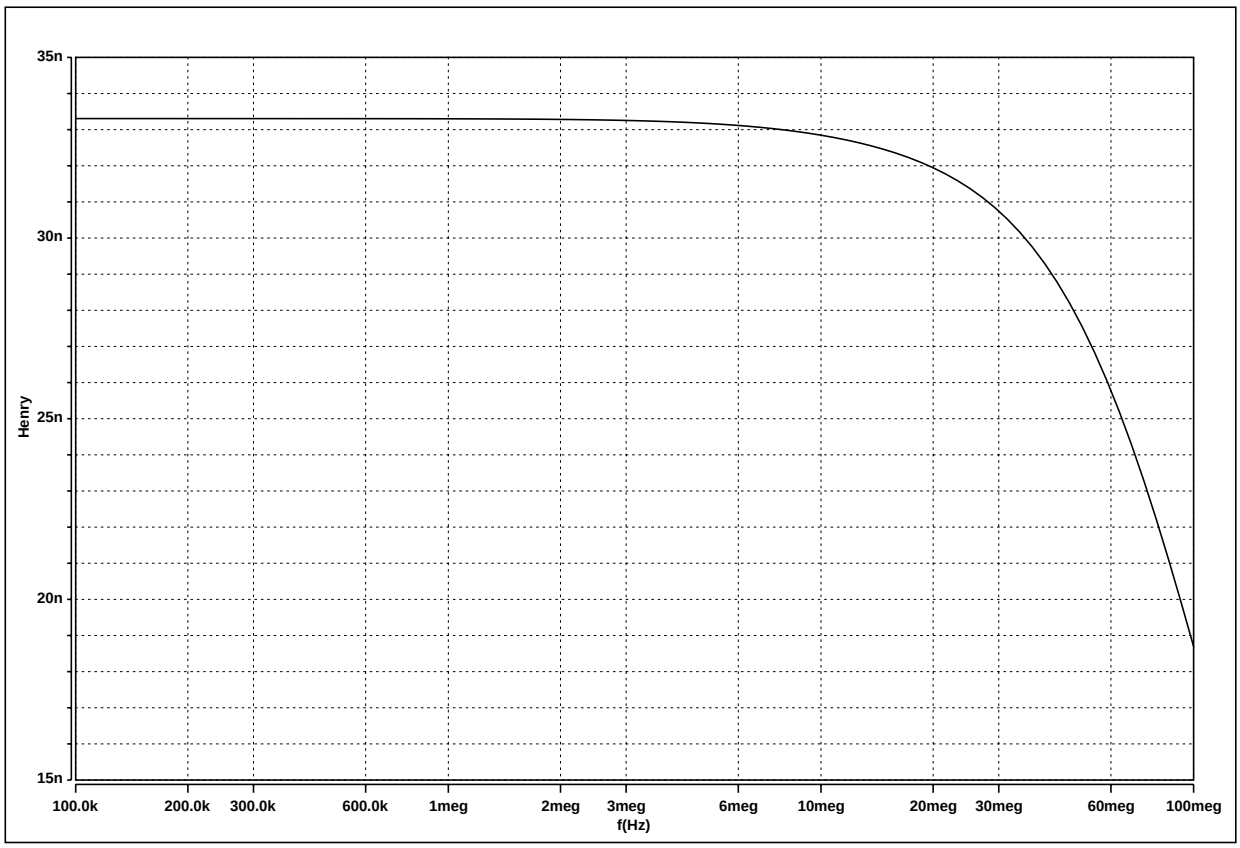
13.7 Base band output impedance pin 19, 20 , Smith diagram



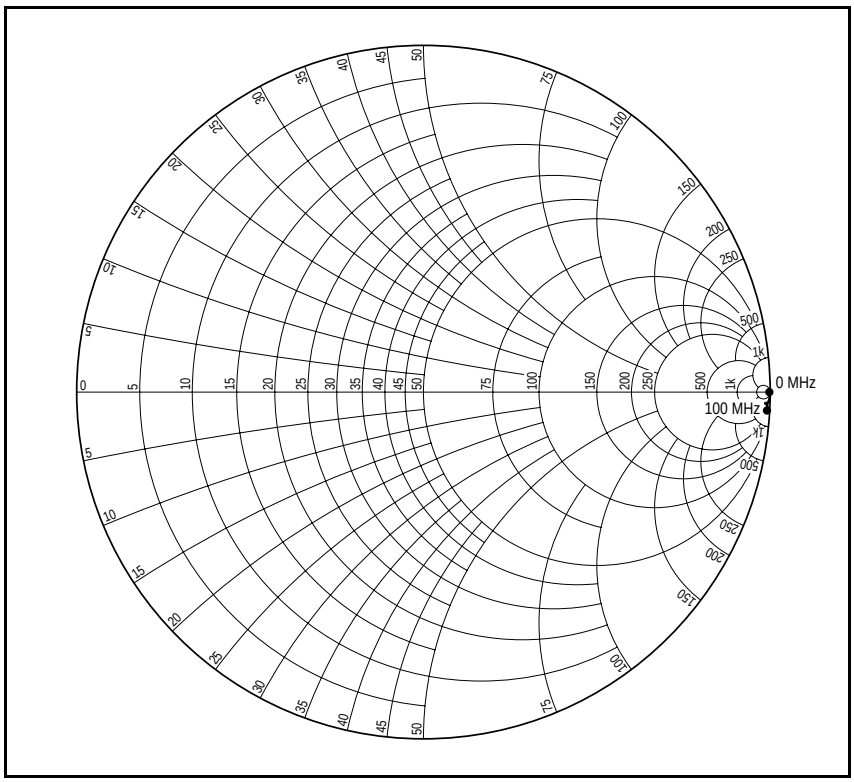
- **Base band output impedance Pin 19, 20 (Ohm)**



- **Base band output inductance Pin 19, 20 (Henry)**

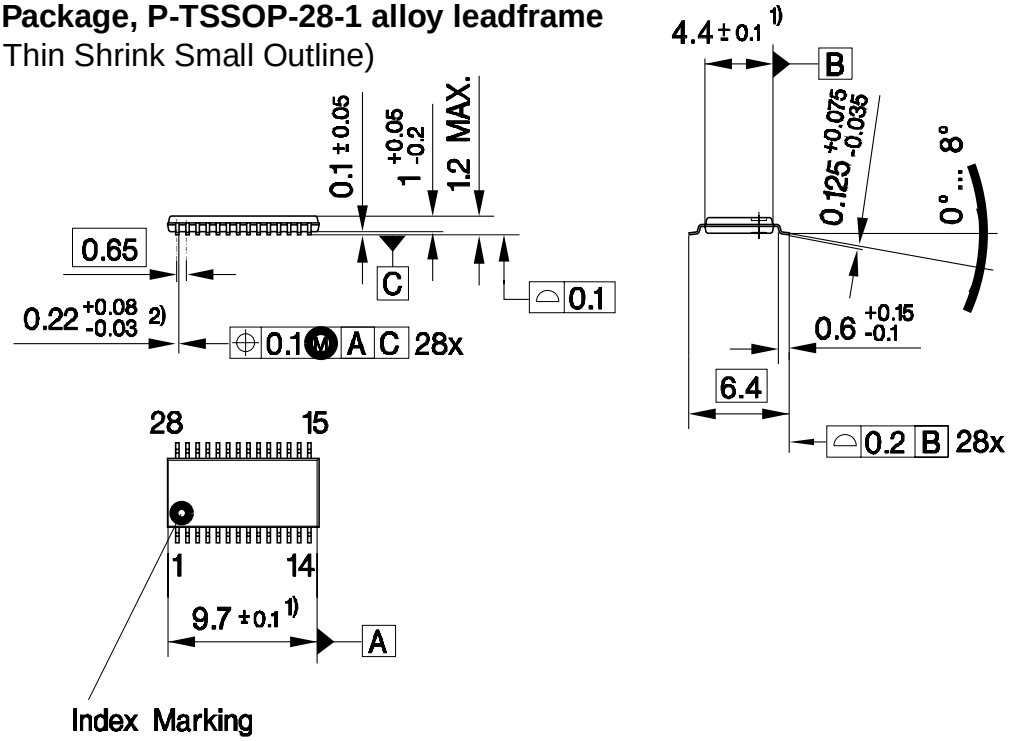


13.8 Base band Input Impedance (filtered)



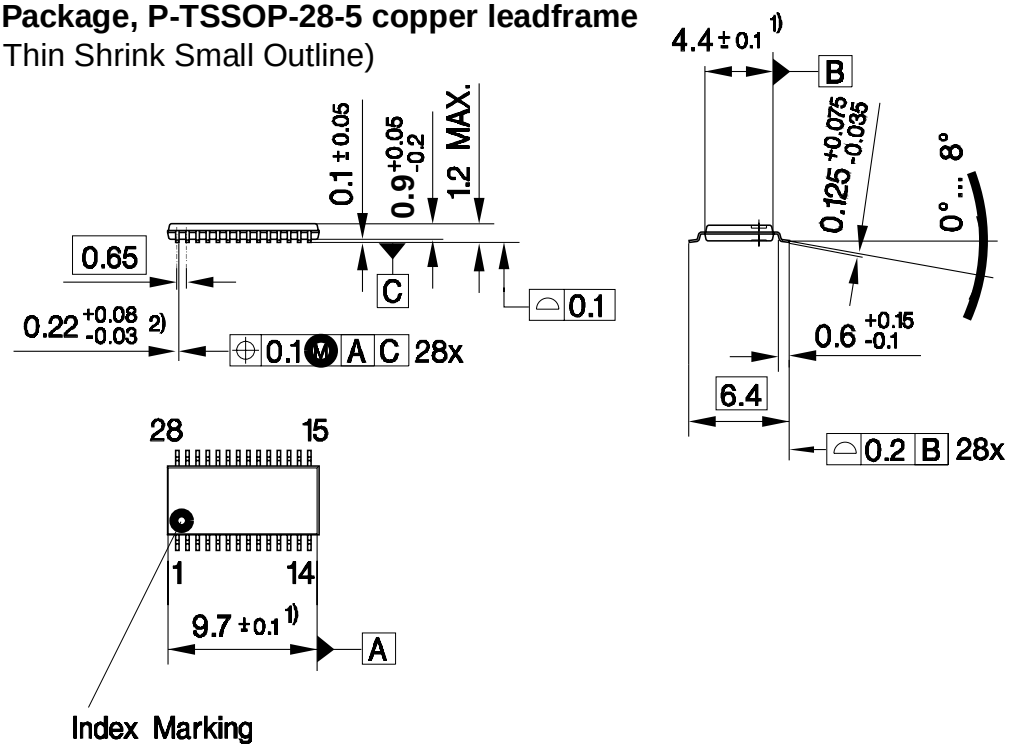
14 Package Outlines

Plastic Package, P-TSSOP-28-1 alloy leadframe
(Plastic Thin Shrink Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Plastic Package, P-TSSOP-28-5 copper leadframe
(Plastic Thin Shrink Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion