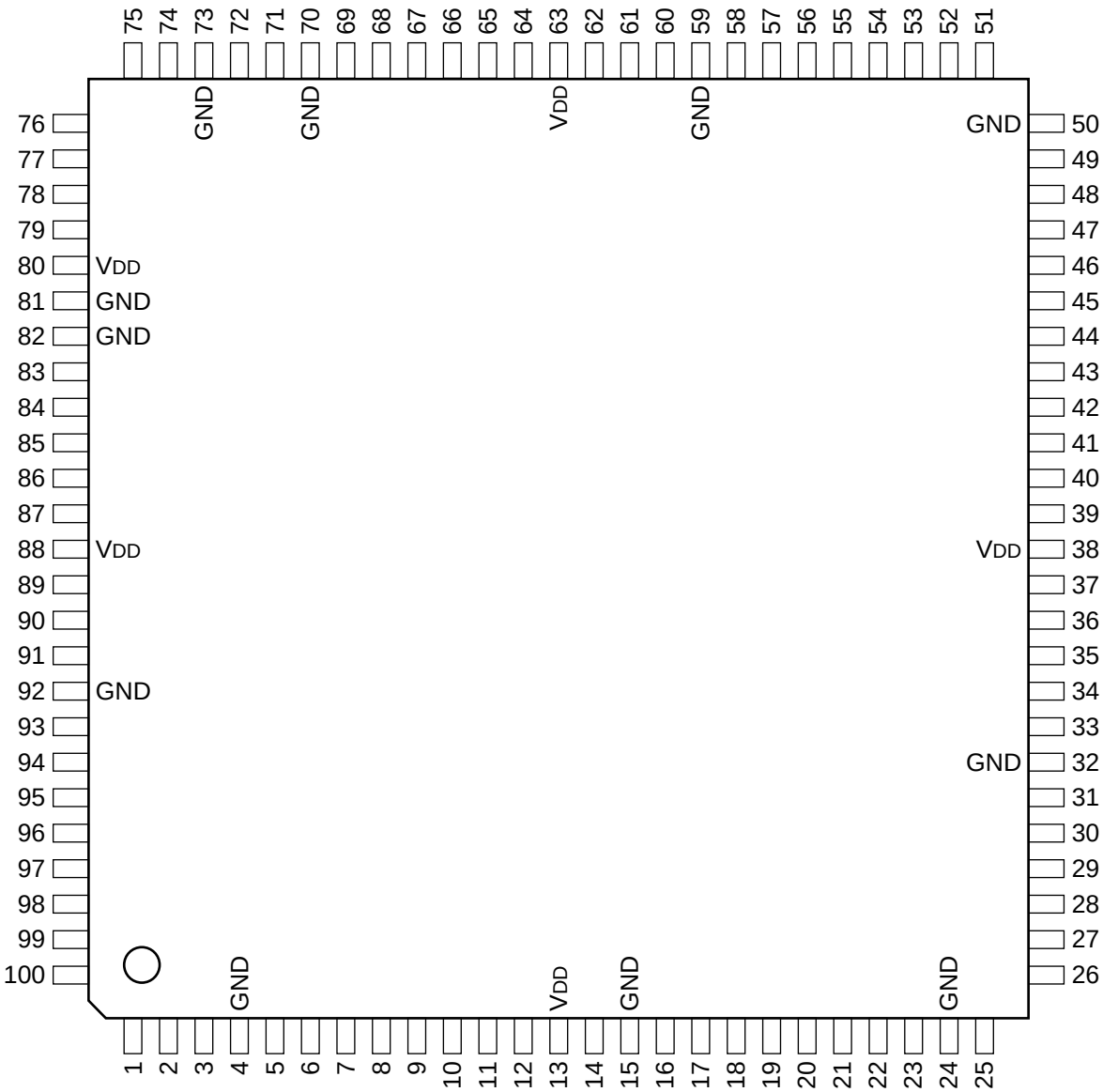
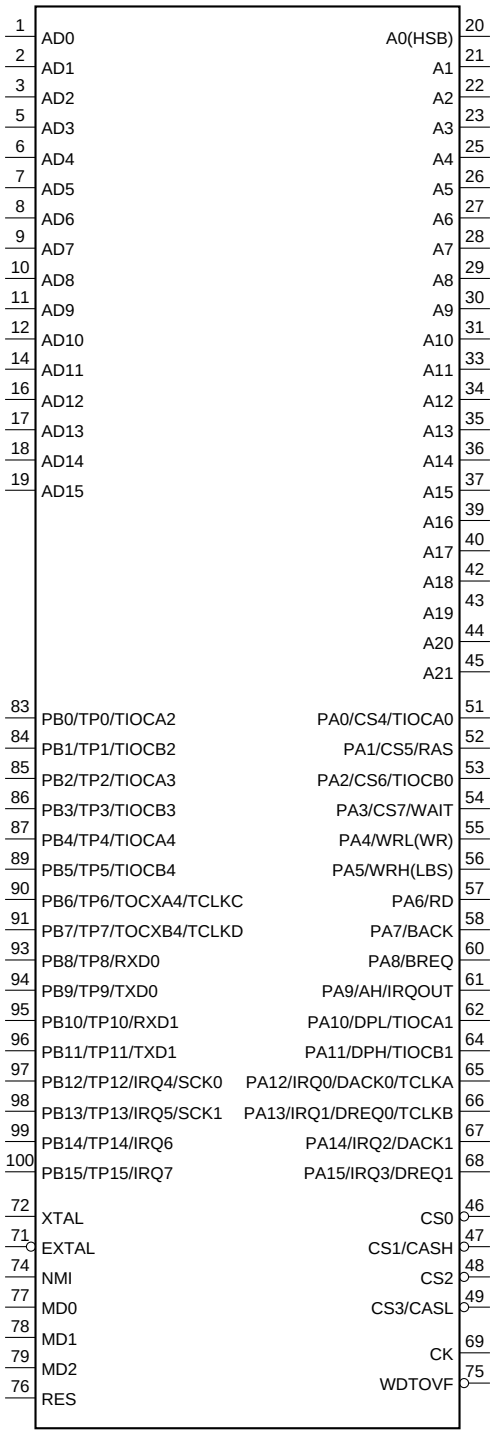
C-MOS 32-BIT MICROPROCESSOR

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	AD0	35	O	A13	69	O	CK
2	I/O	AD1	36	O	A14	70	—	GND
3	I/O	AD2	37	O	A15	71	I	EXTAL
4	—	GND	38	—	V_{DD}	72	I	XTAL
5	I/O	AD3	39	O	A16	73	—	GND
6	I/O	AD4	40	O	A17	74	I	NMI
7	I/O	AD5	41	—	GND	75	O	$\overline{\text{WDTOVF}}$
8	I/O	AD6	42	O	A18	76	I	$\overline{\text{RES}}$
9	I/O	AD7	43	O	A19	77	I	MD0
10	I/O	AD8	44	O	A20	78	I	MD1
11	I/O	AD9	45	O	A21	79	I	MD2
12	I/O	AD10	46	O	$\overline{\text{CS0}}$	80	—	V_{DD}
13	—	V_{DD}	47	O	$\overline{\text{CS1/CASH}}$	81	—	GND
14	I/O	AD11	48	O	$\overline{\text{CS2}}$	82	—	GND
15	—	GND	49	O	$\overline{\text{CS3/CASL}}$	83	I/O	PB0/TP0/TIOCA2
16	I/O	AD12	50	—	GND	84	I/O	PB1/TP1/TIOCB2
17	I/O	AD13	51	I/O	PA0/$\overline{\text{CS4}}$/TIOCA0	85	I/O	PB2/TP2/TIOCA3
18	I/O	AD14	52	I/O	PA1/$\overline{\text{CS5}}$/$\overline{\text{RAS}}$	86	I/O	PB3/TP3/TIOCB3
19	I/O	AD15	53	I/O	PA2/$\overline{\text{CS6}}$/TIOCB0	87	I/O	PB4/TP4/TIOCA4
20	O	A0 ($\overline{\text{HBS}}$)	54	I/O	PA3/$\overline{\text{CS7/WAIT}}$	88	—	V_{DD}
21	O	A1	55	I/O	PA4/$\overline{\text{WRL}}$/($\overline{\text{WR}}$)	89	I/O	PB5/TP5/TIOCB4
22	O	A2	56	I/O	PA5/$\overline{\text{WRH}}$/($\overline{\text{LBS}}$)	90	I/O	PB6/TP6/TOCXA4/TCLKC
23	O	A3	57	I/O	PA6/$\overline{\text{RD}}$	91	I/O	PB7/TP7/TOCXB4/TCLKD
24	—	GND	58	I/O	PA7/$\overline{\text{BACK}}$	92	—	GND
25	O	A4	59	—	GND	93	I/O	PB8/TP8/RXD0
26	O	A5	60	I/O	PA8/BREQ	94	I/O	PB9/TP9/TXD0
27	O	A6	61	I/O	PA9/$\overline{\text{AH/IRQOUT}}$	95	I/O	PB10/TP10/RXD1
28	O	A7	62	I/O	PA10/DPL/TIOCA1	96	I/O	PB11/TP11/TXD1
29	O	A8	63	—	V_{DD}	97	I/O	PB12/TP12/$\overline{\text{IRQ4}}$/SCK0
30	O	A9	64	I/O	PA11/DPH/TIOCB1	98	I/O	PB13/TP13/$\overline{\text{IRQ5}}$/SCK1
31	O	A10	65	I/O	PA12/$\overline{\text{IRQ0}}$/DACK0/TCLKA	99	I/O	PB14/TP14/$\overline{\text{IRQ6}}$
32	—	GND	66	I/O	PA13/$\overline{\text{IRQ1}}$/$\overline{\text{DREQ0}}$/TCLKB	100	I/O	PB15/TP15/$\overline{\text{IRQ7}}$
33	O	A11	67	I/O	PA14/$\overline{\text{IRQ2}}$/DACK1			
34	O	A12	68	I/O	PA15/$\overline{\text{IRQ3}}$/DREQ1			



INPUT

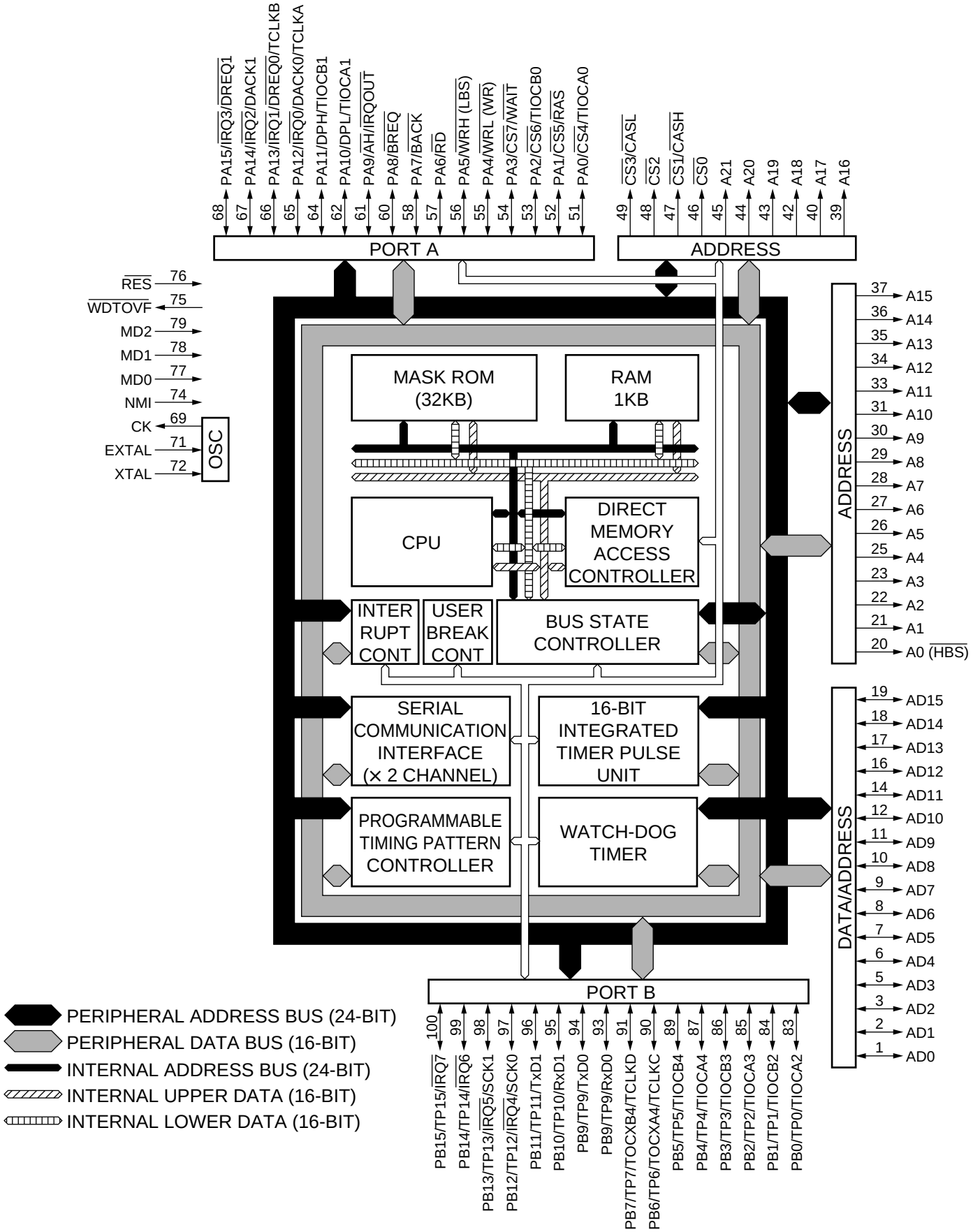
BREQ	;	BUS REQUEST
DREQ0, DREQ1	;	DMA REQUEST
EXTAL	;	CRYSTAL OSCILLATOR AND EXTERNAL CLOCK
IRQ0 - IRQ7	;	INTERRUPT REQUEST
MD0 - MD2	;	MODE SELECT
NMI	;	NON-MASKABLE INTERRUPT
RES	;	RESET
RXD0, RXD1	;	RECEIVE DATA
TCLKA - TCLKD	;	TIMER CLOCK
WAIT	;	WAIT
XTAL	;	EXTERNAL CRYSTAL OSCILLATOR

OUTPUT

AH	;	ADDRESS HOLD
A0 - A21	;	ADDRESS BUS
BACK	;	BUS REQUEST ACKNOWLEDGE
CASH	;	HIGH COLUMN ADDRESS STROBE
CASL	;	LOW COLUMN ADDRESS STROBE
CK	;	SYSTEM CLOCK
CS0 - CS7	;	CHIP SELECT
DACK0, DACK1	;	DMA REQUEST ACKNOWLEDGE
HBS	;	HIGH BYTE STROBE
LBS	;	LOW BYTE STROBE
RAS	;	ROW ADDRESS STROBE
RD	;	READ
RQOUT	;	REQUEST OUTPUT
TOCXA4	;	OUTPUT COMPARE XA4
TOCXB4	;	OUTPUT COMPARE XB4
TP0 - TP15	;	TIMING PATTERN CONTROLLER
TXD0, TXD1	;	TRANSMIT DATA
WDTOVF	;	WATCH-DOG TIMER OVERFLOW
WR	;	WRITE
WRH	;	HIGH WRITE
WRL	;	LOW WRITE

INPUT/OUTPUT

AD0 - AD15	;	DATA/ADDRESS BUS
DPH	;	HIGH DATA PARITY
DPL	;	LOW DATA PARITY
PA0 - PA15	;	I/O PORT A
PB0 - PB15	;	I/O PORT B
SCK0, SCK1	;	SERIAL CLOCK
TIOCA0 - TIOCA4	;	ITU INPUT CAPTURE/OUTPUT COMPARE
TIOB0 - TIOCB4	;	ITU INPUT CAPTURE/OUTPUT COMPARE


PA15/IRQ3/DREQ1
PA14/IRQ2/DACK1
PA13/IRQ1/DREQ0/TCLKB
PA12/IRQ0/DACK0/TCLKA
PA11/DPH/TIOCB1
PA10/DPL/TIOCA1
PA9/AH/IRQOUT
PA8/BREQ
PA7/BACK
PA6/RD
PA5/WRH (LBS)
PA4/WRL (WR)
PA3/CS7/WAIT
PA2/CS6/TIOCB0
PA1/CS5/RAS
PA0/CS4/TIOCA0
CS3/CASL
CS2
CS1/CASH
CS0
A21
A20
A19
A18
A17
A16
PORT A
ADDRESS
RES
WDTOVF
MD2
MD1
MD0
NMI
CK
EXTAL
XTAL
OSC
MASK ROM (32KB)
RAM 1KB
CPU
DIRECT MEMORY ACCESS CONTROLLER
INTER RUPT CONT
USER BREAK CONT
BUS STATE CONTROLLER
SERIAL COMMUNICATION INTERFACE (× 2 CHANNEL)
16-BIT INTEGRATED TIMER PULSE UNIT
PROGRAMMABLE TIMING PATTERN CONTROLLER
WATCH-DOG TIMER
ADDRESS
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0 (HBS)
DATA/ADDRESS
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PORT B
PB15/TP15/IRQ7
PB14/TP14/IRQ6
PB13/TP13/IRQ5/SCK1
PB12/TP12/IRQ4/SCK0
PB11/TP11/TxD1
PB10/TP10/RxD1
PB9/TP9/TxD0
PB9/TP9/RxD0
PB7/TP7/TOCXB4/TCLKD
PB6/TP6/TOCXA4/TCLKC
PB5/TP5/TIOCB4
PB4/TP4/TIOCA4
PB3/TP3/TIOCB3
PB2/TP2/TIOCA3
PB1/TP1/TIOCB2
PB0/TP0/TIOCA2
PERIPHERAL ADDRESS BUS (24-BIT)
PERIPHERAL DATA BUS (16-BIT)
INTERNAL ADDRESS BUS (24-BIT)
INTERNAL UPPER DATA (16-BIT)
INTERNAL LOWER DATA (16-BIT)