ESDALC6V1M3

Dual low capacitance TRANSIL™ array for ESD protection

Main product applications

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Features

- 2 unidirectional low capacitance TRANSIL diodes
- Breakdown Voltage V_{BR} = 6.1 V min
- Low diode capacitance (11 pF typ at 0 V)
- Low leakage current < 0.5 µA
- Very small PCB area: 0.6 mm²
- RoHS compliant

Description

The ESDALC6V1M3 is a monolithic array designed to protect 1 line or 2 lines against ESD transients.

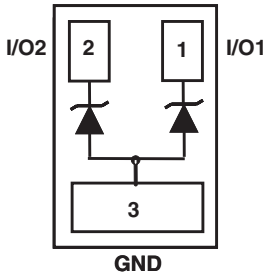
The device is ideal for applications where both reduced line capacitance and board space saving are required.

Benefits

- High ESD protection level
- High integration
- Suitable for high density boards

SOT 883
(JEDEC MO-236AA Compliant)

Configuration



Underside view

Order code

Part number	Marking
ESDALC6V1M3	K

Complies with the following standards

IEC61000-4-2 level 4:

15 kV (air discharge)
8 kV (contact discharge)

MIL STD 883E-Method 3015-7: class 3

HBM (Human Body Model)

TRANSIL is a trademark of STMicroelectronics

1 Characteristics

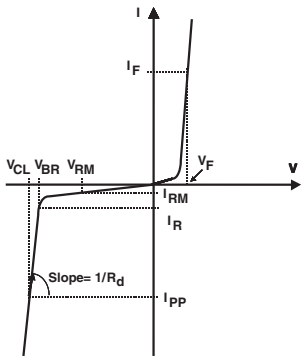
Table 1. Absolute ratings (T_{AMB} = 25° C - limiting values)

Symbol		Parameter		Value	Unit
V_{PP}	ESD discharge	IEC61000-4-2 air discharge IEC61000-4-2 contact discharge		± 15 ± 8	kV
P_{PP}	Peak pulse power dissipation (8/20 µs)(1)		T_j initial = T_{AMB}	30	W
I_{pp}	Repetitive peak pulse current (8/20 µs)			3	A
Tj	Junction temperature			125	° C
Tstg	Storage temperature range			-55 + 150	° C
T_L	Maximum lead temperature for soldering during 10 s			260	° C
T_{OP}	Operating temperature range			-40 + 125	° C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Table 2. Electrical characteristics (T_{AMB} = 25° C)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current @ V_{RM}
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
V_F	Forward voltage drop



Parameter	Test condition	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	6.1		7.2	V
I_{RM}	V_{RM} = 5 V			0.5	µA
R_d			1.1		Ω
αT	I_R = 1 mA			4.2	10^{-4}/°C
C	V_R = 0 V, F = 1 MHz, V_{OSC} = 30 mV		11		pF

Figure 1. S21 attenuation measurement results of each channel

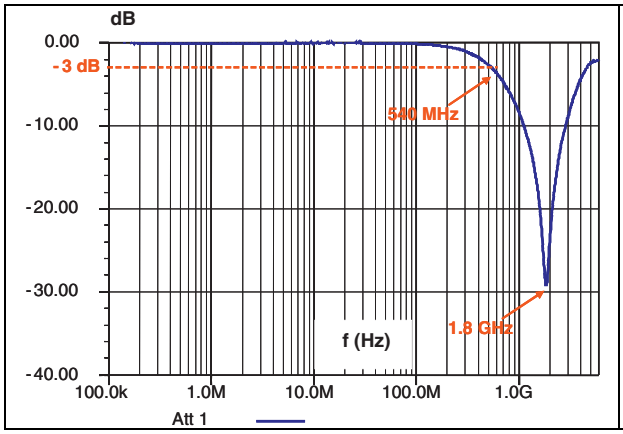


Figure 2. Analog crosstalk measurements between channels

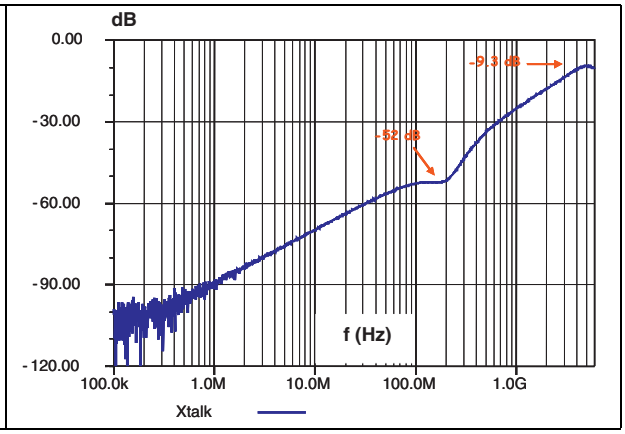


Figure 3. ESD response to IEC61000-4-2 (+15 kV air discharge) on each channel

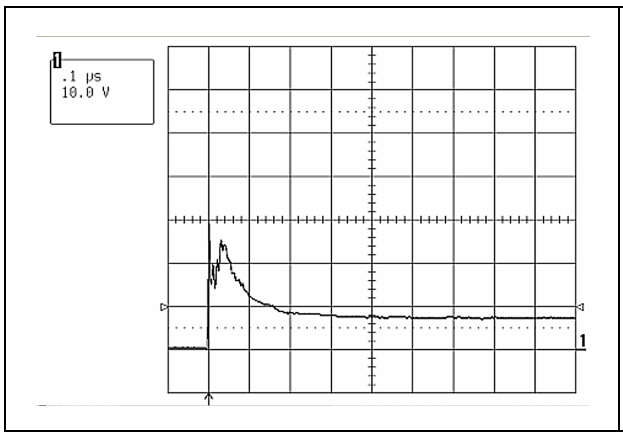


Figure 4. ESD response to IEC61000-4-2 (-15 kV air discharge) on each channel.

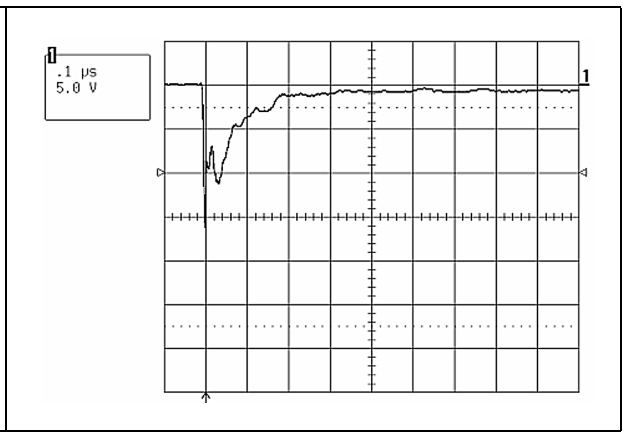


Figure 5. Relative variation of peak pulse power versus initial junction temperature

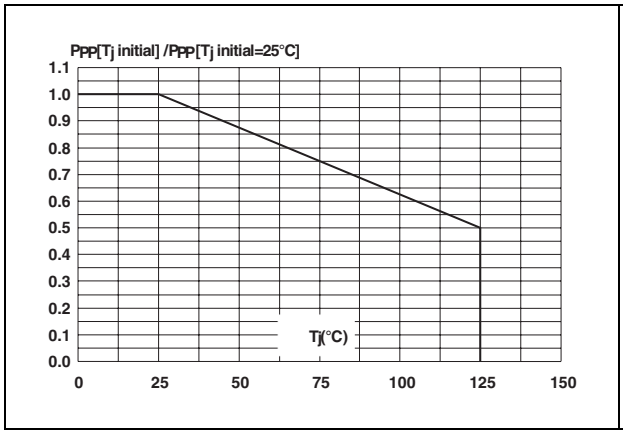


Figure 6. Peak pulse power versus exponential pulse duration

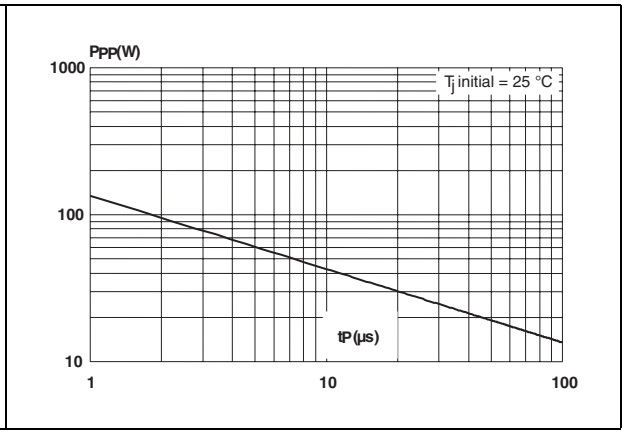


Figure 7. Clamping voltage versus peak pulse current (typical values)

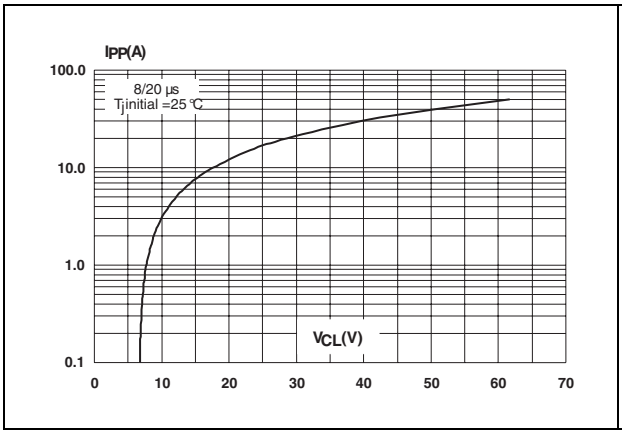


Figure 8. Forward voltage drop versus peak forward current (typical values)

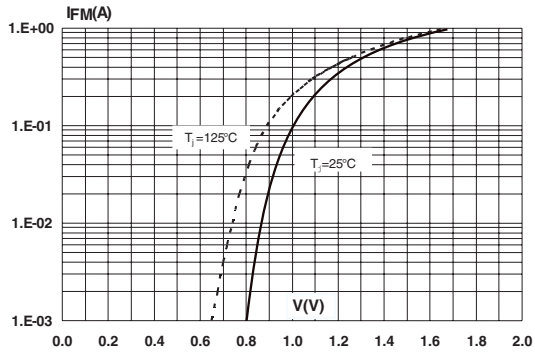


Figure 9. Junction capacitance versus reverse voltage applied (typical values)

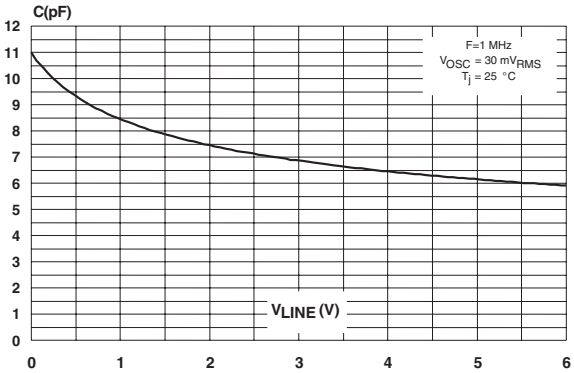
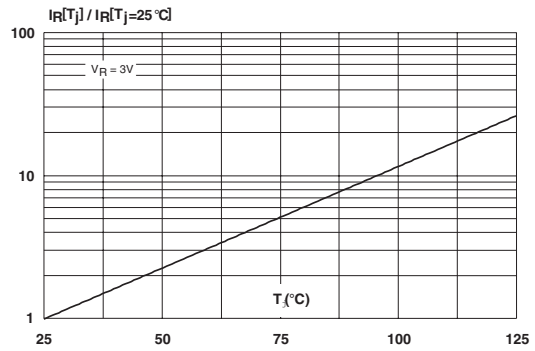


Figure 10. Relative variation of leakage current versus junction temperature (typical values)



2 Ordering information scheme

ESDA LC 6V1 M3

ESD Array

Low Capacitance

Breakdown Voltage

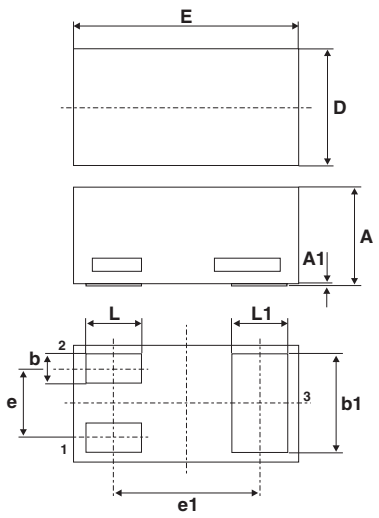
6V1 = 6.1 Volts min

Package

M3 = SOT883

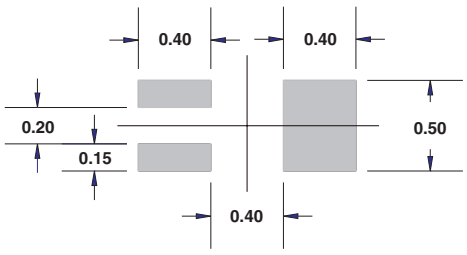
3 Package information

Table 3. SOT883 Dimensions



Ref.	Dimensions					
	Millimetres			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.45		0.52	0.18		0.2
A1	0.00		0.05	0.00		0.02
b	0.10	0.15	0.20	0.04	0.06	0.08
b1	0.45	0.50	0.55	0.18	0.20	0.22
D		0.60			0.24	
E		1.00			0.39	
e		0.35			0.14	
e1		0.65			0.26	
L	0.20	0.25	0.30	0.08	0.10	0.12
L1	0.20	0.25	0.30	0.08	0.10	0.12

Figure 11. Footprint



All dimensions in mm

Figure 12. Marking

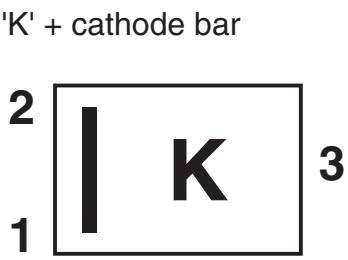


Figure 13. ST Ecopack® recommended soldering reflow profile for PCB mounting

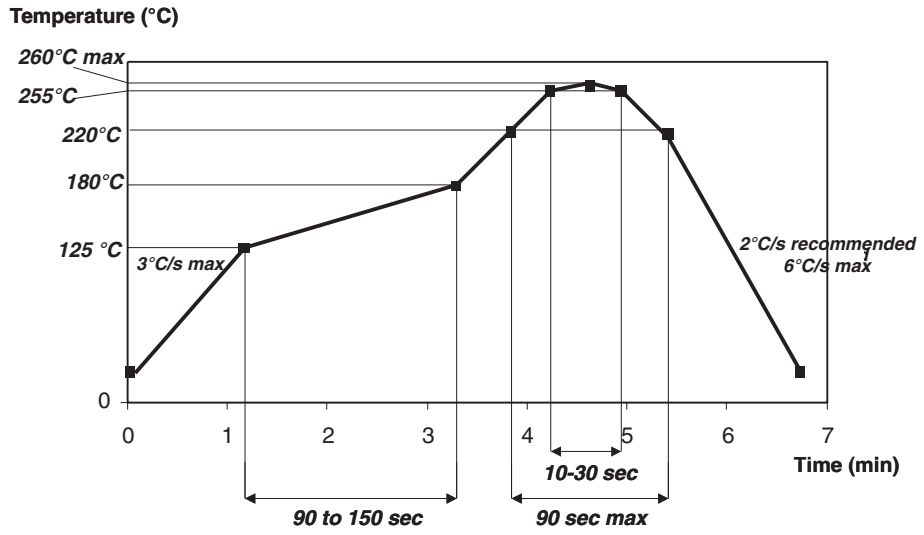
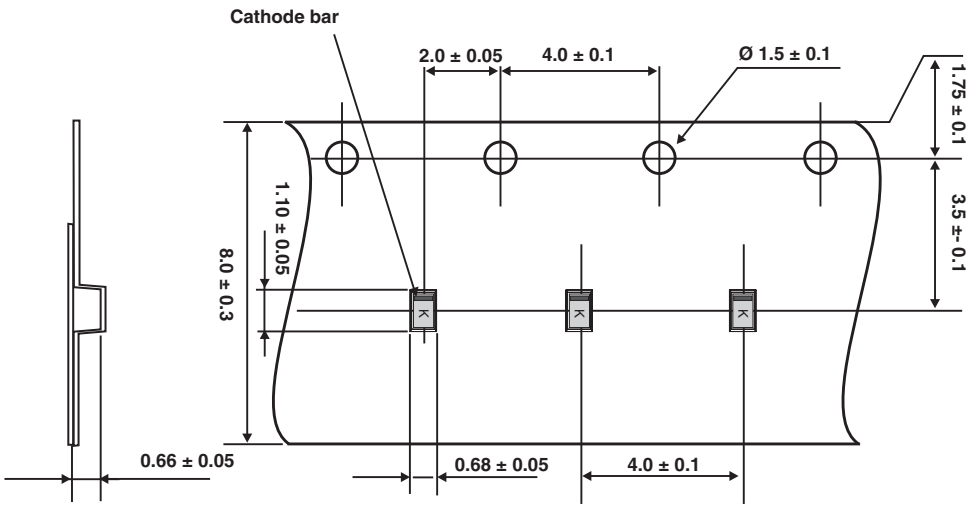


Figure 14. Packing information



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Part number	Marking	Package	Weight	Bulk qty	Delivery mode
ESDALC6V1M3	K	SOT883	0.96 mg	30 000	Tape and reel

5 Revision history

Date	Revision	Changes
04-Aug-2005	1	Initial release.
23-May-2006	2	Reformated to current standards. Added soldering reflow profile diagram.
16-Jun-2006	3	Updated tape and reel illustration (Figure 14).