

SONY

CXK5814P

2048-word $\times$ 8 bit High Speed CMOS Static RAM

Description

The CXK5814P is a 16,384 bits high speed CMOS static RAM organized as 2,048 words $\times$ 8 bits and operates from a single 5V supply.

The CXK5814P is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: 35 ns/45 ns/55 ns (Max.)
- Low power standby: 5 μ W (Typ.)—L-version
100 μ W (Typ.)—Standard version
- Low power operation: 300 mW (Typ.)
- Single +5V supply
- Fully static memory No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- High density: 300 mil 24 pin plastic package

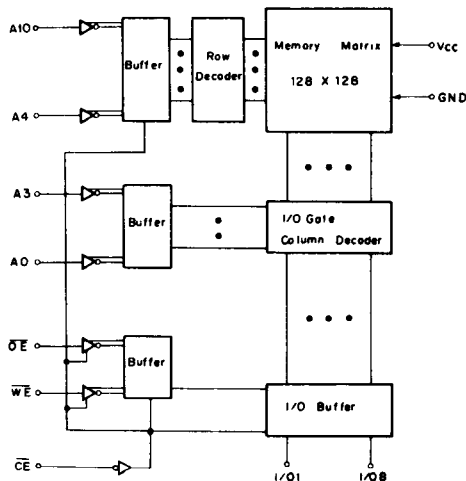
Function

2048-word $\times$ 8 bit static RAM

Structure

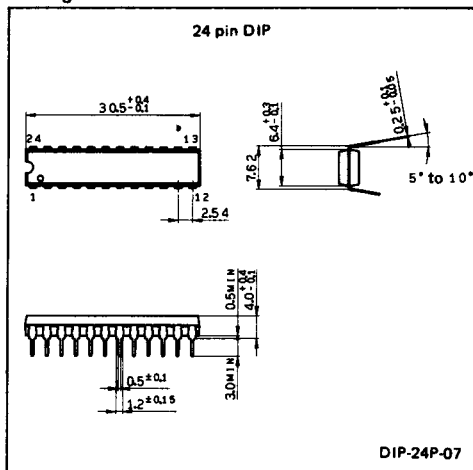
Silicon Gate CMOS IC

Block Diagram

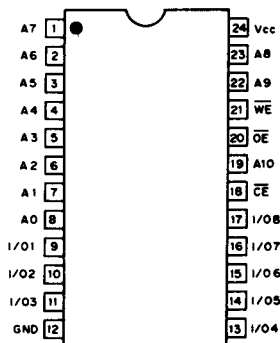


Package Outline

Unit: mm



Pin Configuration (Top View)



Symbol	Description
A0 to A10	Address Input
I/O1 to I/O8	Data Input Output
$\overline{CE}$	Chip Enable Input
WE	Write Enable Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	-0.5* to +7.0	V
Input Voltage	V _{IN}	-0.5* to V _{CC} +0.5	V
Input and Output Voltage	V _{I/O}	-0.5* to V _{CC} +0.5	V
Allowable Power Dissipation	P _D	1.0	W
Operating Temperature	T _{opr}	0 to +70	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Soldering Temperature	T _{solder}	260 ± 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} min=-3.5V for 20 ns pulse.**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O 1 to I/O 8	V _{CC} Current
H	X	X	Not Selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output Disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	D _{OUT}	I _{CC1} , I _{CC2}
L	X	L	Write	D _{IN}	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.*	Max.	Unit
Power Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Input High Voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input Low Voltage	V _{IL}	-0.3	—	0.8	V

* V_{CC}=5V, Ta=25°C

DC and Operating Characteristics

(V_{CC}=5V±10%, GND=0V, T_a=0 to +70°C)

Item	Symbol	Test condition	CXK5814P -35/45/55			CXK5814P -35L/45L/55L			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Input Leakage Current	I _{LI}	V _{IN} =GND to V _{CC}	-2	—	2	-2	—	2	μA	
Output Leakage Current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-2	—	2	-2	—	2	μA	
Operating Power Supply Current	I _{CC1}	$\overline{CE}=V_{IL}$	35/35L	—	60	85	—	60	85	mA
		I _{OUT} =0mA	45/45L	—	50	70	—	50	70	mA
		V _{IN} =V _{IH} /V _{IL}	55/55L	—	40	60	—	40	60	mA
Average Operating Current	I _{CC2}	Cycle=Min	35/35L	—	70	95	—	70	95	mA
		Duty=100%	45/45L	—	60	80	—	60	80	mA
		I _{OUT} =0mA	55/55L	—	50	70	—	50	70	mA
Standby Current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$, V _{IN} $\geq V_{CC}-0.2V$ or V _{IN} $\leq 0.2V$	—	0.02	1.0	—	0.001	0.05	mA	
	I _{SB2}	$\overline{CE}=V_{IH}$, V _{IN} =V _{IH} /V _{IL}	—	15	25	—	15	25	mA	
Output High Voltage	V _{OH}	I _{OH} =-4.0 mA	2.4	—	—	2.4	—	—	V	
Output Low Voltage	V _{OL}	I _{OL} =8.0 mA	—	—	0.4	—	—	0.4	V	

Capacitance

(T_a=25°C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C _{IN}	V _{IN} =0V	—	5	pF
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

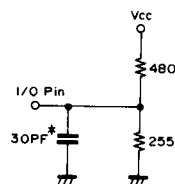
AC Operating Characteristics

• AC Test condition

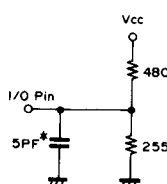
(V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Condition
Input Pulse High Level	V _{IH} =3.0V
Input Pulse Low Level	V _{IL} =0V
Input Rise Time	t _r =5 ns
Input Fall Time	t _f =5 ns
Input and Output Timing Reference Level	1.5V
Output Load	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

Read Cycle

Item	Symbol	CXK5814P -35/35L		CXK5814P -45/45L		CXK5814P -55/55L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	trc	35	—	45	—	55	—	ns
Address Access Time	tAA	—	35	—	45	—	55	ns
Chip Enable Access Time	tCO	—	35	—	45	—	55	ns
Output Enable to Output Valid	toE	—	20	—	20	—	25	ns
Output Hold from Address Change	toH	5	—	5	—	5	—	ns
Chip Enable to Output in Low Z ($\overline{CE}$)	tlZ*	5	—	5	—	5	—	ns
Output Enable to Output in Low Z ($\overline{OE}$)	tolZ*	0	—	0	—	0	—	ns
Chip Disable to Output in High Z ($\overline{CE}$)	thZ*	0	20	0	20	0	20	ns
Output Disable to Output in High Z ($\overline{OE}$)	toHZ*	0	15	0	15	0	20	ns
Chip Enable to Power Up Time	tpU	0	—	0	—	0	—	ns
Chip Disable to Power Down Time	tpD	—	30	—	30	—	30	ns

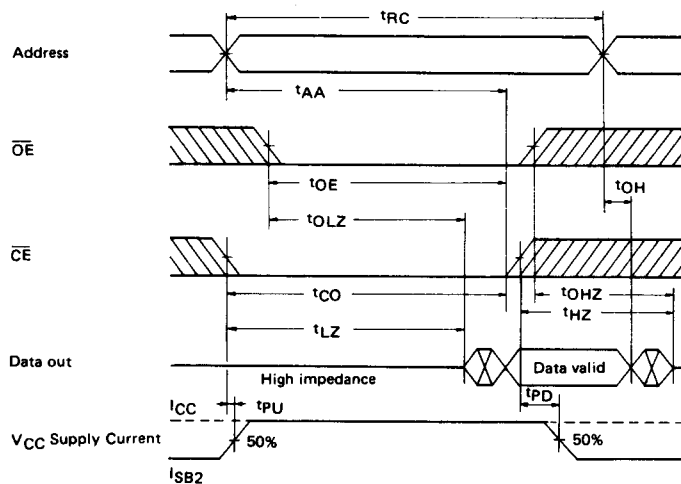
Write Cycle

Item	Symbol	CXK5814P -35/35L		CXK5814P -45/45L		CXK5814P -55/55L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	twc	35	—	45	—	55	—	ns
Address Valid to End of Write	tAW	30	—	40	—	50	—	ns
Chip Enable to End of Write	tcw	30	—	40	—	50	—	ns
Data to Write Time Overlap	tdw	15	—	20	—	25	—	ns
Data Hold from Write Time	tdH	0	—	0	—	0	—	ns
Write Pulse Width	tWP	30	—	35	—	40	—	ns
Address Setup Time	tAS	0	—	0	—	0	—	ns
Write Recovery Time	tWR	0	—	0	—	0	—	ns
Output Active from End of Write	tOW*	5	—	5	—	5	—	ns
Write to Output in High Z	twHZ*	0	20	0	20	0	20	ns

*Note) Transition is measured ± 500 mV from steady state voltage with specified loading in Fig. 1. These parameters are sampled and not 100% tested.

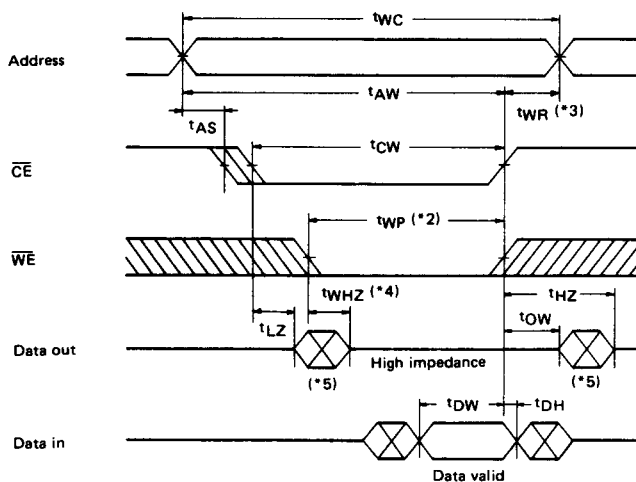
Timing Waveform

(1) Read Cycle [$\overline{WE}=V_{IH}$]

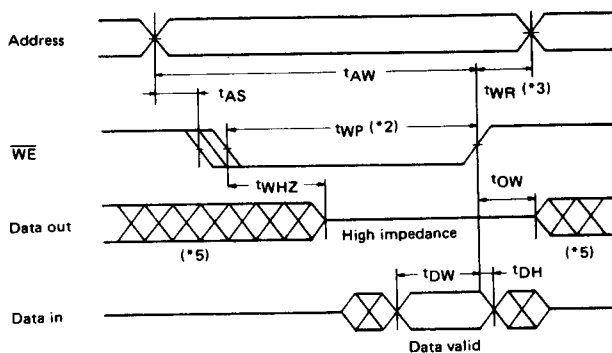


(2) Write Cycle

- Write Cycle No.1: [$\overline{OE}=V_{IL}$ or V_{IH}] (*1)



- Write Cycle No.2: [$\overline{OE}=V_{IL}$ or V_{IH} , $\overline{CE}=V_{IL}$] (*1)



* Notes

1. If $\overline{OE}$ is high, output remains in a high impedance state.
2. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

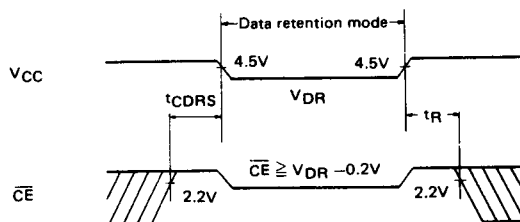
Data Retention Characteristics

($T_a=0$ to $+70^\circ\text{C}$)

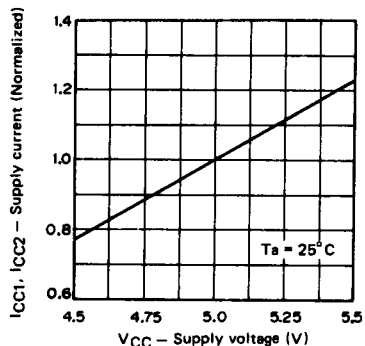
Item	Symbol	Test condition	CXK5814P -35/45/55			CXK5814P -35L/45L/55L			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data Retention Voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2\text{V}$	2.0	5.0	5.5	2.0	5.0	5.5	V
Data Retention Current	I_{CCDR1}	$\overline{CE} \geq V_{CC} - 0.2\text{V}$, $V_{CC}=3.0\text{V}$		12	600		0.6	30	μA
	I_{CCDR2}	$V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$, $V_{CC}=2.0$ to 5.5V		20	1000		1.0	50	μA
Data Retention Set up Time	t_{CDRS}	Chip disable to data retention mode	0			0			ns
Recovery Time	t_R		t_{RC}^*			t_{RC}^*			ns

* t_{RC} : Read Cycle Time

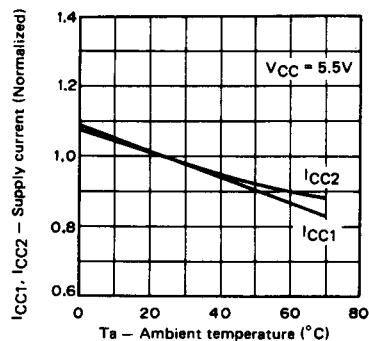
Data Retention Waveform



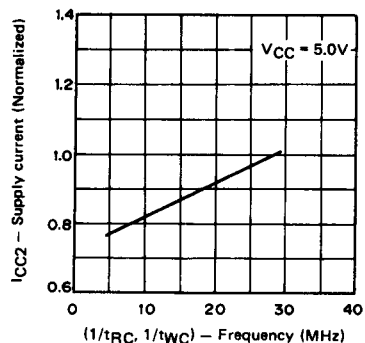
**Supply current vs.
Supply voltage**



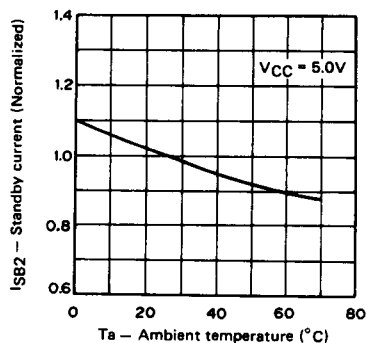
**Supply current vs.
Ambient temperature**



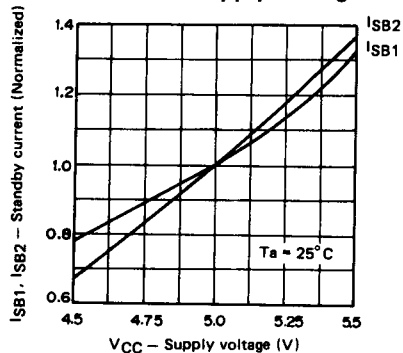
Supply current vs. Frequency



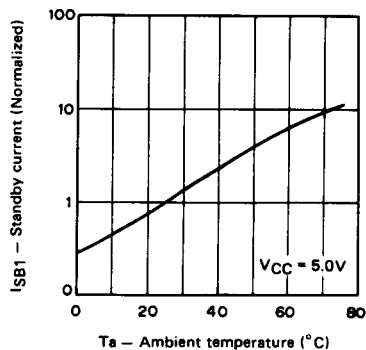
**Standby current vs.
Ambient temperature**



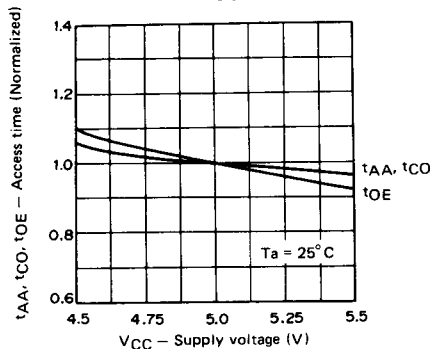
**Standby current vs.
Supply voltage**



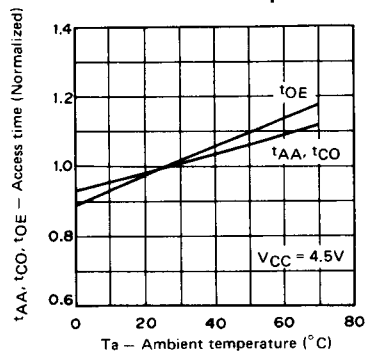
**Standby current vs.
Ambient temperature**



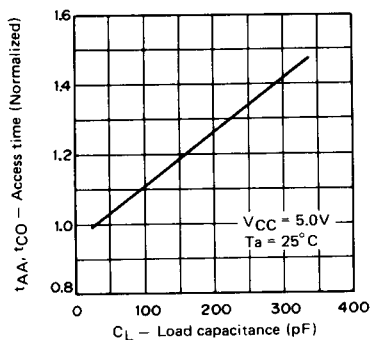
**Access time vs.
Supply voltage**



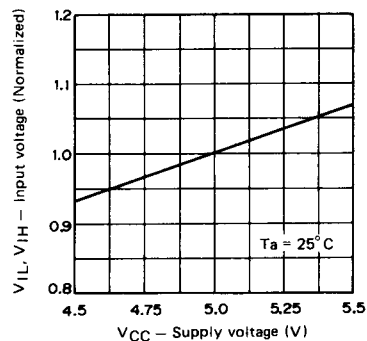
**Access time vs.
Ambient temperature**



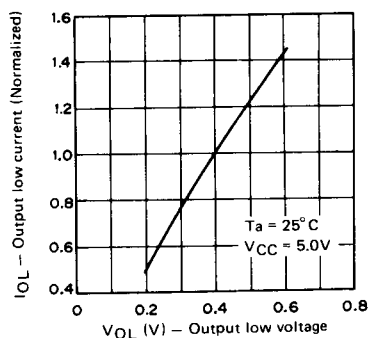
**Access time vs.
Load capacitance**



**Input voltage vs.
Supply voltage**



**Output current vs.
Output voltage**



**Output current vs.
Output voltage**

