M5M44400CJ,TP-5,-6,-7, -5S,-6S,-7S

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 4-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer metalization process technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities. Self or extended refresh current is low enough for battery back-up application.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M44400CXX-5,-5S	50	13	25	13	90	500
M5M44400CXX-6,-6S	60	15	30	15	110	400
M5M44400CXX-7,-7S	70	20	35	20	130	350

XX=J,TP

- Standard 26pin SOJ, 26pin TSOP (II)
- Single 5V±10% supply
- Low stand-by power dissipation
  CMOS Input level ---------------------------5.5mW (Max)
  CMOS Input level -----------------------550 μ W (Max) *
- Operating power dissipation
  M5M44400Cxx-5,-5S --------------------- 687.5mW (Max)
  M5M44400Cxx-6,-6S --------------------- 550.0mW (Max)
  M5M44400Cxx-7,-7S --------------------- 467.5mW (Max)
- Self refresh capability *
  Self refresh current ------------------------- 120 μ A(Max)
- Extended refresh capability
  Extended refresh current ------------------- 120 μ A(Max)
- Fast-page mode(1024-column random access),Read-modify-write, $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities.
- Early-write mode, $\overline{CAS}$ and $\overline{OE}$ to control output buffer impedance
- 1024 refresh cycles every 16.4ms (A$_0$ ~A$_9$)
- 1024 refresh cycles every 128ms (A$_0$ ~A$_9$) *
- 4-bit parallel test mode capability
 * :Applicable to self refresh version (M5M44400CJ,TP-5S,-6S,-7S :option) only

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A$_0$~A$_9$	Address inputs
DQ$_1$~DQ$_4$	Data inputs/outputs
$\overline{RAS}$	Row address strobe input
$\overline{CAS}$	Column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+5V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)
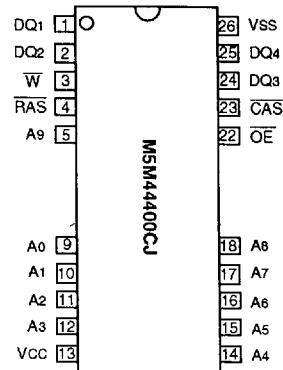
Outline 26P0J(300mil SOJ)
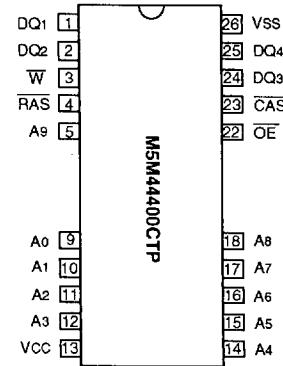
Outline 26P3Z-E(300mil TSOP)

M5M44400CJ,TP-5,-5S:Under development

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FUNCTION

In addition to normal read, write, and read-modify-write operations the M5M44400CJ, TP provides a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	NAC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ (Extended*) refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Self refresh*	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM

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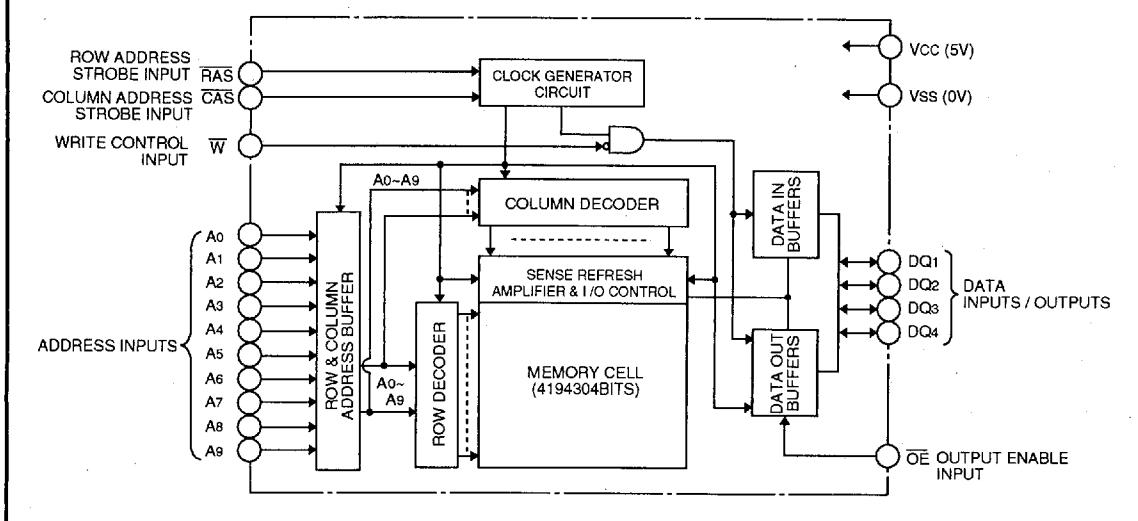
FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	-1 ~ 7	V
V_I	Input voltage		-1 ~ 7	V
V_O	Output voltage		-1 ~ 7	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25°C	1000	mW
T_{opr}	Operating temperature		0 ~ 70	°C
T_{stg}	Storage temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter		Min	Nom	Max	Unit
				Limits		
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	High-level input voltage, all inputs		2.4		6.5	V
V_{IL}	Low-level input voltage	DQ_1~DQ_4	-1.0		0.8	V
		Others	-2.0		0.8	

Note 1 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
					Limits		
V_{OH}	High-level output voltage		IOH=-5mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		IOL=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating, 0V≦VOUT≦5.5V	-10		10	μA
I_I	Input current		0V≦VIN≦+6.5V, Other inputs pins=0V	-10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC=twc=min. output open			125	mA
		M5M44400C-6,-6S				100	
		M5M44400C-7,-7S				85	
I_{CC2} (AV)	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =VIH, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.5V			1.0	
			output open			0.1*	
I_{CC3} (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$= VIH tRC=min. output open			125	mA
		M5M44400C-6,-6S				100	
		M5M44400C-7,-7S				85	
I_{CC4} (AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open			105	mA
		M5M44400C-6,-6S				85	
		M5M44400C-7,-7S				75	
I_{CC6}(AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open			105	mA
		M5M44400C-6,-6S				85	
		M5M44400C-7,-7S				75	
I_{CC8}(AV)*	Average supply current from Vcc, Extended-Refresh mode (Note 6)		$\overline{RAS}$ cycling $\overline{CAS}$ ≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling $\overline{RAS}$≦0.2V or ≧Vcc-0.2V $\overline{CAS}$≦0.2V or ≧Vcc-0.2V $\overline{W}$≦0.2V(Except for $\overline{RAS}$ falling edge) or ≧Vcc-0.2V $\overline{OE}$≦0.2V or ≧Vcc-0.2V Ao~A9≦0.2V or ≧Vcc-0.2V, DQ=open tRC=125 μs, tRAS=tRASmin~1 μs			120	μA
I_{CC9}(AV)*	Average supply current from Vcc, Self-Refresh mode (Note 6)		$\overline{RAS}$=$\overline{CAS}$≦0.2V output open			120	μA

Note 2: Current flowing into an IC is positive, out is negative.

3: ICC1 (AV), ICC3 (AV), ICC4 (AV) and ICC6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: ICC1 (AV) and ICC4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while $\overline{RAS}$=VIL and $\overline{CAS}$=VIH

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CAPACITANCE (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_I(A)$	Input capacitance, address inputs	$V_I=V_{ss}$			5	pF
$C_I(CLK)$	Input capacitance, clock inputs	f=1MHz			7	pF
$C_{I/O}$	Input/Output capacitance, data ports	$V_I=25mV_{rms}$			7	pF

SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 7,8)		13		15		20	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 7,9)		50		60		70	ns
t_{AA}	Column address access time	(Note 7,10)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 7,11)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$	(Note 7)		13		15		20	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 12)		13		15		20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 12)		13		15		20	ns

Note 6:An initial pause of 200 μ s is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$- only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh cycles).

Note the $\overline{RAS}$ may be cycled during the initial pause. And 8 initialization cycles are required after prolonged periods (greater than t_{REF}(max)) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7:Measured with a load circuit equivalent to 2TTL loads and 100pF.

8:Assumes that $t_{RCD} \geqq t_{RCD}$(max) and $t_{ASC} \geqq t_{ASC}$(max).

9:Assumes that $t_{RCD} \leqq t_{RCD}$(max) and $t_{RAD} \leqq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} or t_{RCD} exceeds the value shown.

10:Assumes that $t_{RAD} \geqq t_{RAD}$(max) and $t_{ASC} \leqq t_{ASC}$(max).

11:Assumes that $t_{CP} \leqq t_{CP}$(max) and $t_{ASC} \geqq t_{ASC}$(max).

12:t_{OFF}(max), t_{OEZ}(max) defines the time at which the output achieves the high impedance state ($I_{OUT} \leqq |\pm 10 \mu A|$) and is not reference to V_{OH}(min) or V_{OL}(max).

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FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~70°C , Vcc = 5V±10%, Vss=0V, unless otherwise noted, see notes 6,13,14)

Symbol	Parameter		Limits					Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S	
			Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time			16.4		16.4		16.4	ms
tREF	Refresh cycle time*			128		128		128	ms
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 15)	18	37	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 16)	13	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	7	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		8		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		13		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note 18)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note 18)	0		0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note 19)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note 19)	13		15		20		ns
tT	Transition time	(Note 20)	1	50	1	50	1	50	ns

Note 13: The timing requirements are assumed tT=5ns.
14: VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
15: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.
16: tRAD(max) is specified as a reference point only. If tRAD≧tRAD(max) and tASC≦tASC(max), access time is controlled exclusively by tAA.
17: tASC(max) is specified as a reference point only. If tRCD≧tRCD(max) and tASC≧tASC(max), access time is controlled exclusively by tCAC.
18: Either tDZC or tDZO must be satisfied.
19: Either tCDD or tODD must be satisfied.
20: tT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

Symbol	Parameter		Limits					Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S	
			Min	Max	Min	Max	Min	Max	
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		13	10000	15	10000	20	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		50		60		70		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		13		15		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low		0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 21)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 21)	0		0		0		ns
tRAL	Column address to $\overline{RAS}$ hold time		25		30		35		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns

Note 21: Either tRCH or tRRH must be satisfied for a read cycle.

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Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tWC	Write cycle time		90		110		130		ns
tRAS	RAS low pulse width		50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width		13	10000	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low		50		60		70		ns
tRSH	RAS hold time after CAS low		13		15		20		ns
tWCS	Write setup time before CAS low	(Note 23)	0		0		0		ns
tWCH	Write hold time after CAS low		8		10		15		ns
tCWL	CAS hold time after W low		13		15		20		ns
tRWL	RAS hold time after W low		13		15		20		ns
tWP	Write pulse width		8		10		15		ns
tDS	Data setup time before CAS low or W low		0		0		0		ns
tDH	Data hold time after CAS low or W low		8		10		15		ns
tOEH	OE hold time after W low		13		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	126		150		180		ns
tRAS	RAS low pulse width		86	10000	100	10000	120	10000	ns
tCAS	CAS low pulse width		49	10000	55	10000	70	10000	ns
tCSH	CAS hold time after RAS low		86		100		120		ns
tRSH	RAS hold time after CAS low		49		55		70		ns
tRCS	Read setup time before CAS low		0		0		0		ns
tCWD	Delay time, CAS low to W low	(Note 23)	31		35		45		ns
tRWD	Delay time, RAS low to W low	(Note 23)	68		80		95		ns
tAWD	Delay time, address to W low	(Note 23)	43		50		60		ns
tCWL	CAS hold time after W low		13		15		20		ns
tRWL	RAS hold time after W low		13		15		20		ns
tWP	Write pulse width		8		10		15		ns
tDS	Data setup time before CAS low or W low		0		0		0		ns
tDH	Data hold time after CAS low or W low		8		10		15		ns
tOEH	OE hold time after W low		13		15		20		ns

Note 22: tRWC is specified as tRWC(min)=tRAC(max)+tODD(min)+tRWL(min)+tRP(min)+4tT.

23: tWCS, tCWD, tRWD, tAWD and tCPWD are specified as reference points only. If tWCS≧tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD(min), tAWD≧tAWD(min) and tCPWD≧tCPWD(min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) is satisfied, the condition of the DQ (at access time and until CAS or OE goes back to V IH) is indeterminate.

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Fast Page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		35		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		71		80		95		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle	(Note 25)	85	100000	100	100000	115	100000	ns
tCP	$\overline{CAS}$ high pulse width	(Note 26)	8	12	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		30		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	48		55		65		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
25: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.
'26: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle * (Note 27)

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	5		5		5		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		10		15		ns
tCAS	$\overline{CAS}$ low pulse width	20		20		25		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Self Refresh Cycle * (Note 28)

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRASS	CBR self refresh $\overline{RAS}$ low pulse width	100		100		100		μs
tRPS	CBR self refresh $\overline{RAS}$ high precharge time	90		110		130		ns
tCHS	CBR self refresh $\overline{CAS}$ hold time	-50		-50		-50		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		10		ns
tRSR	Read hold time after $\overline{RAS}$ low	10		10		15		ns

Test Mode Specification (Note 29)
ELECTRICAL CHARACTERISTICS (Ta=0~70°C , Vcc=5V±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
ICC1 (AV)	Average supply current from Vcc, operating (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC≈twc=min. output open			145	mA
		M5M44400C-6,-6S				115	
		M5M44400C-7,-7S				100	
ICC3 (AV)	Average supply current from Vcc, $\overline{RAS}$ only refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=VIH tRC=min. output open			145	mA
		M5M44400C-6,-6S				115	
		M5M44400C-7,-7S				100	
ICC4 (AV)	Average supply current from Vcc, Fast Page Mode (Note 3,4,5)	M5M44400C-5,-5S	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open			120	mA
		M5M44400C-6,-6S				100	
		M5M44400C-7,-7S				85	
ICC6 (AV)	Average supply current from Vcc, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3,5)	M5M44400C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open			120	mA
		M5M44400C-6,-6S				100	
		M5M44400C-7,-7S				85	

Note 29: All previously specified electrical characteristics, switching characteristics, and timing requirements are applicable to that of test mode.

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

SWITCHING CHARATERISTICS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 6, 13, 14)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7, 8)		18		20		25	ns
tRAC	Access time from $\overline{RAS}$	(Note 7, 9)		55		65		75	ns
tAA	Column address access time	(Note 7, 10)		30		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7, 11)		35		40		45	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		18		20		25	ns

TIMING REQUIREMENTS (Ta=0~70°C, Vcc=5V±10%, Vss=0V, unless otherwise noted, see notes 13, 14)

Read and Refresh Cfycle

Symbol	Parameter		Limits					Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	95		115		135		ns
tRAS	$\overline{RAS}$ low pulse width	55	10000	65	10000	75	10000	ns
tCAS	$\overline{CAS}$ low pulse width	18	10000	20	10000	25	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	55		65		75		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	18		20		25		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		40		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	18		20		25		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	18		20		25		ns

Read Write and Read-Modify-Write Cfycle

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note 22)	131		155		185		ns
tRAS	$\overline{RAS}$ low pulse width		91	10000	105	10000	125	10000	ns
tCAS	$\overline{CAS}$ low pulse width		54	10000	60	10000	75	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		91		105		125		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		54		60		75		ns
tCWD	Delay time, $\overline{CAS}$ low $\overline{W}$ low	(Note 23)	36		40		50		ns
tRWD	Delay time, $\overline{RAS}$ low $\overline{W}$ low	(Note 23)	73		85		100		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note 23)	48		55		65		ns

Fast page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle) (Note 24)

Symbol	Parameter		Limits						Unit
			M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		40		45		50		ns
tPRWC	Fast page mode read write/read modify write cycle time		76		85		100		ns
tRAS	$\overline{RAS}$ low pulse width for read or write cycle	(Note 25)	95	100000	110	100000	125	100000	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		45		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note 23)	53		60		70		ns

Test Mode Set Cycle

Symbol	Parameter	Limits						Unit
		M5M44400C-5,-5S		M5M44400C-6,-6S		M5M44400C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tWSR	Write setup time before $\overline{RAS}$ low	10		10		10		ns
tWHR	Write hold time after $\overline{RAS}$ low	10		10		15		ns

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FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Timing Diagrams (Note 30)
Read Cycle
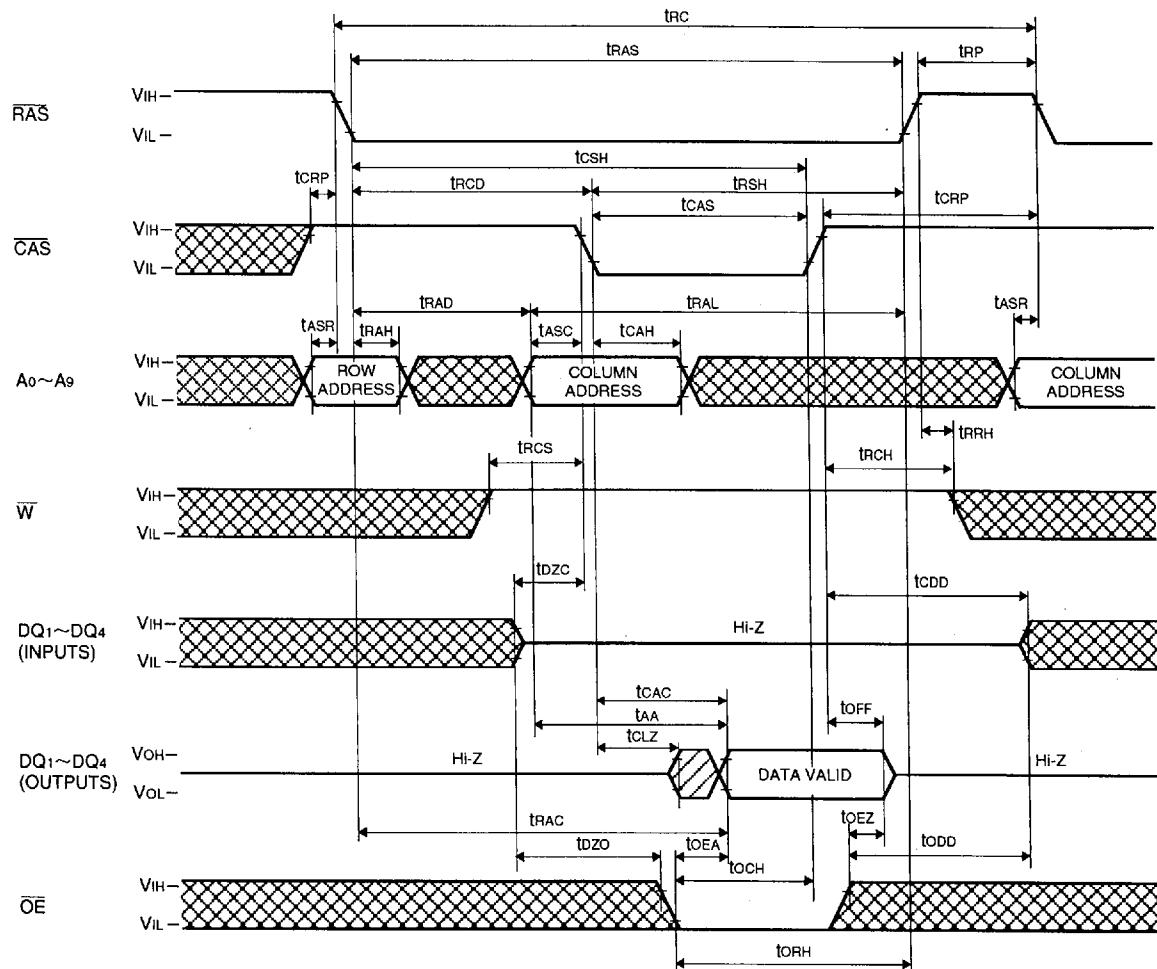
Note 30

Indicates the don't care input.
$V_{IH}(min) \leq V_{IN} \leq V_{IH}(max)$ or $V_{IL}(min) \leq V_{IN} \leq V_{IL}(max)$
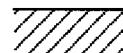
Indicates the invalid output.

6249825 0028246 836

### FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM
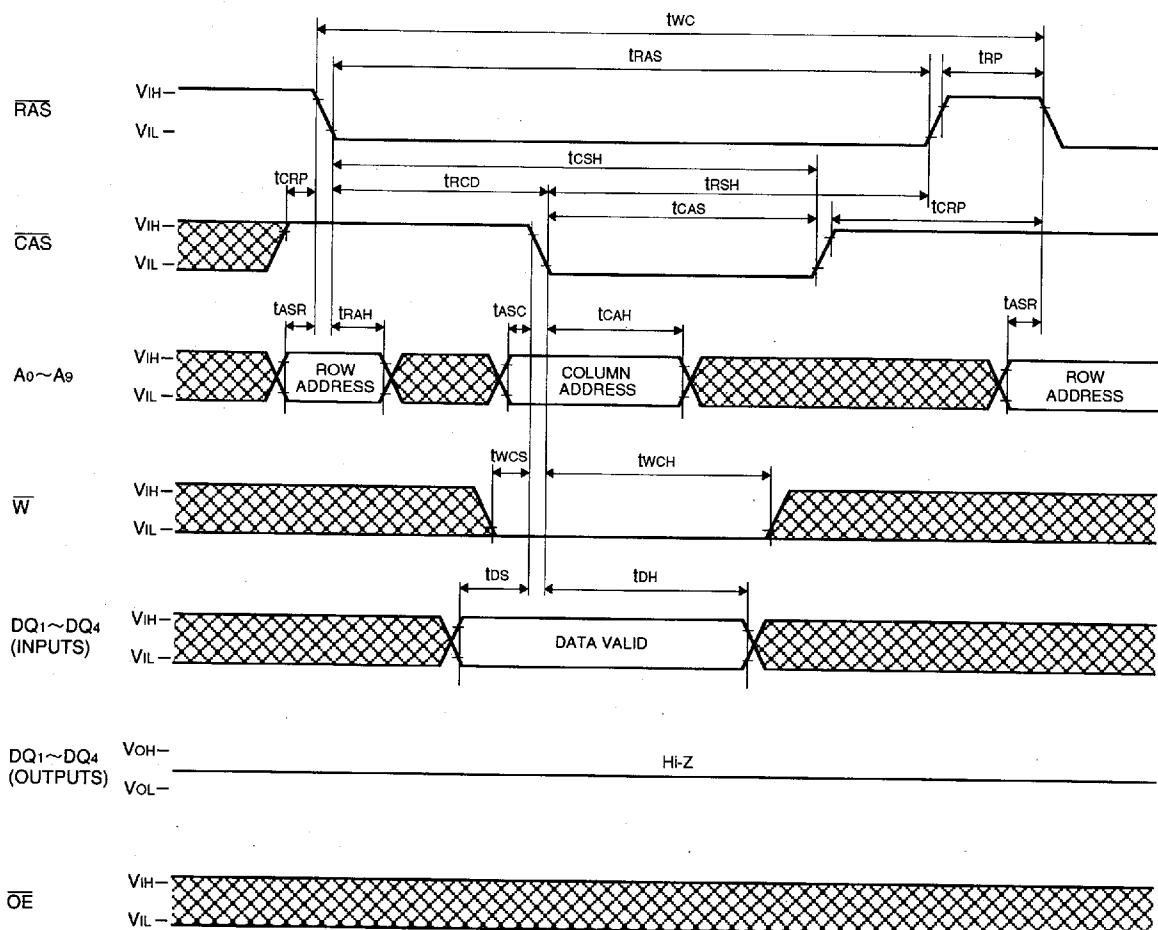
Write Cycle (Early write)

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Write Cycle (Delayed write)
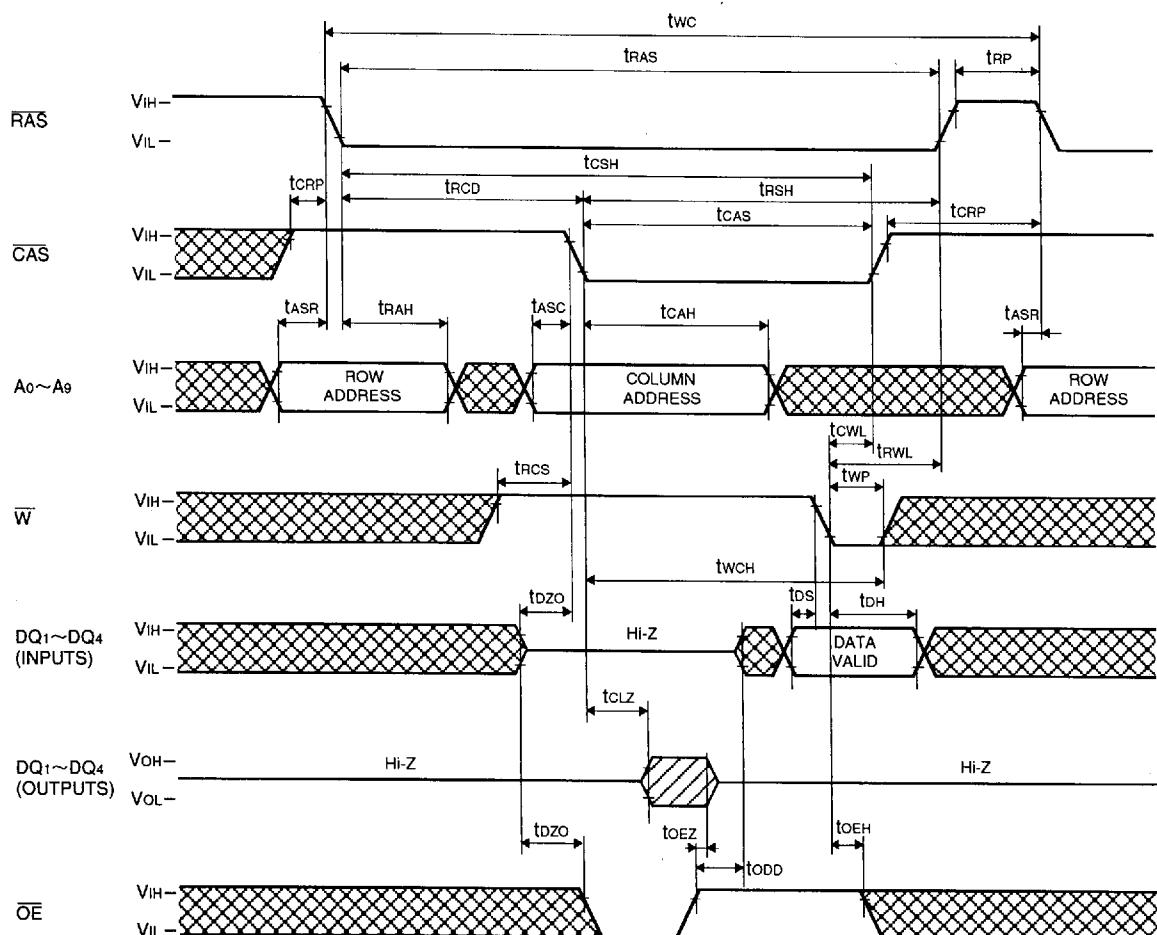
6249825 0028248 609

Read-Write, Read-Modify-Write Cycle

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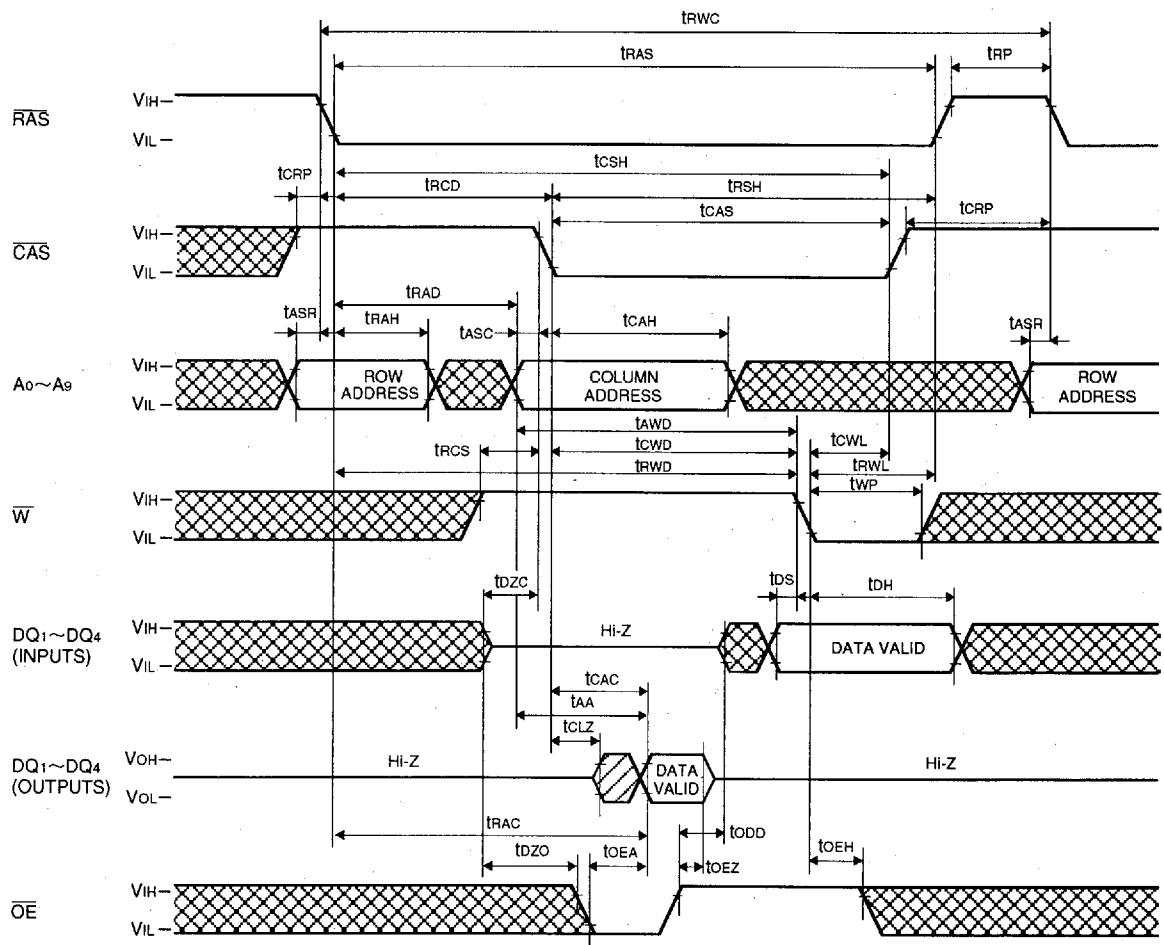
$\overline{\text{RAS}}$-only Refresh Cycle
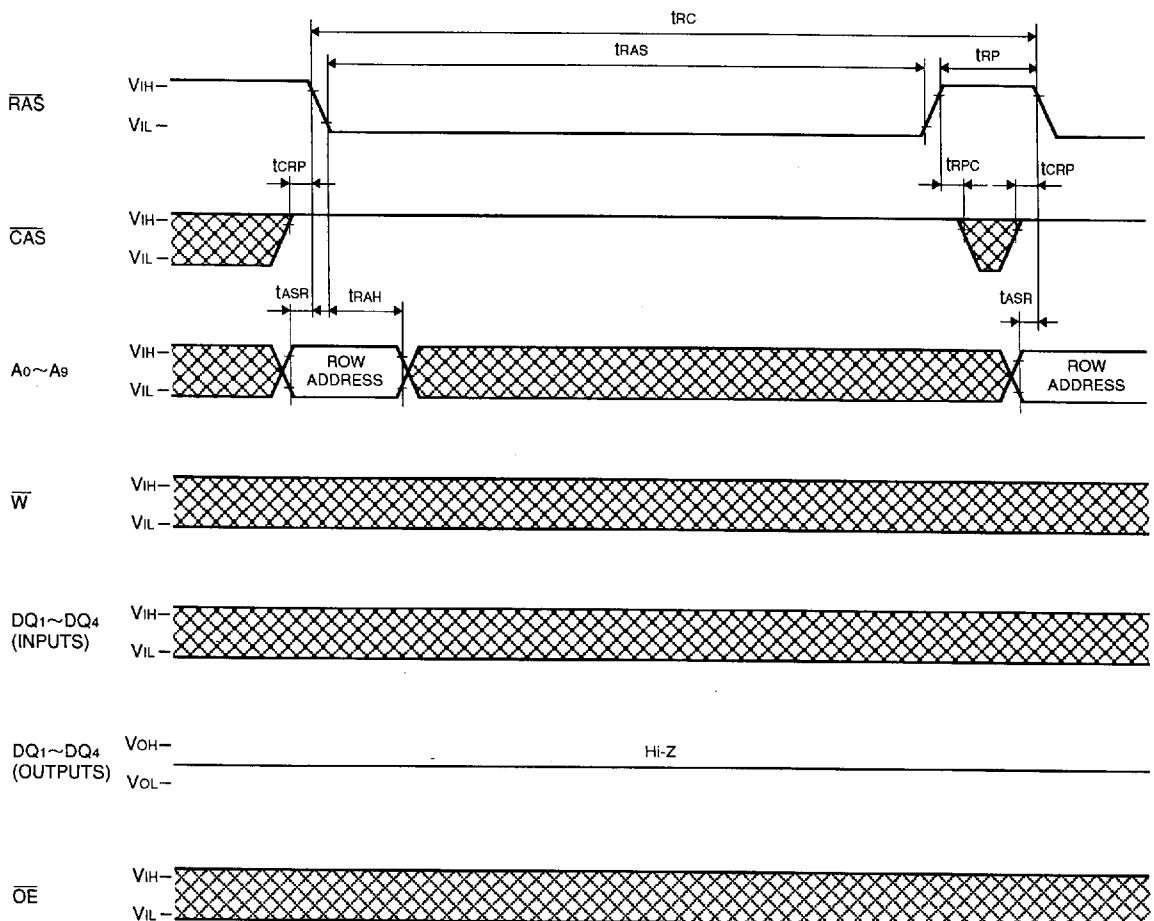
FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *
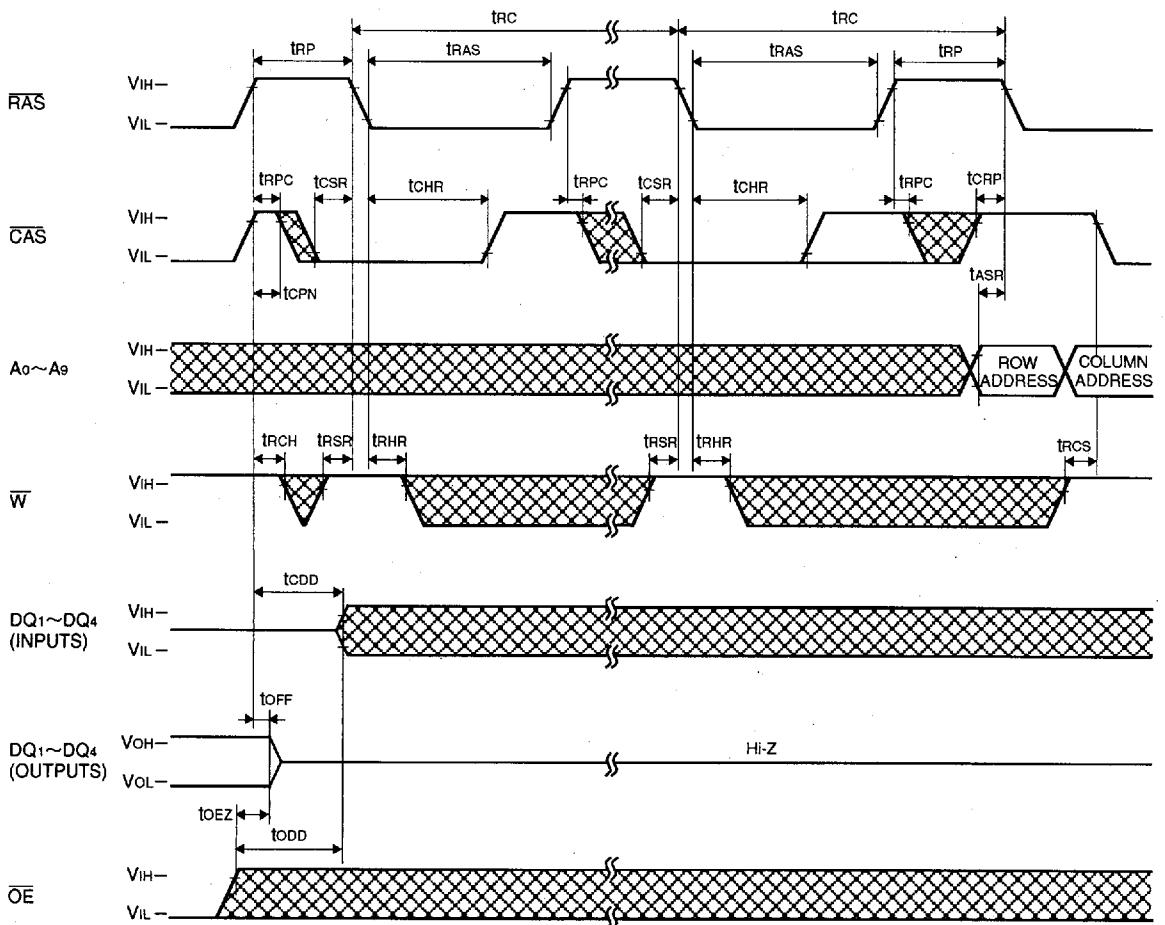
FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Hidden Refresh Cycle (Read) (Note 31)
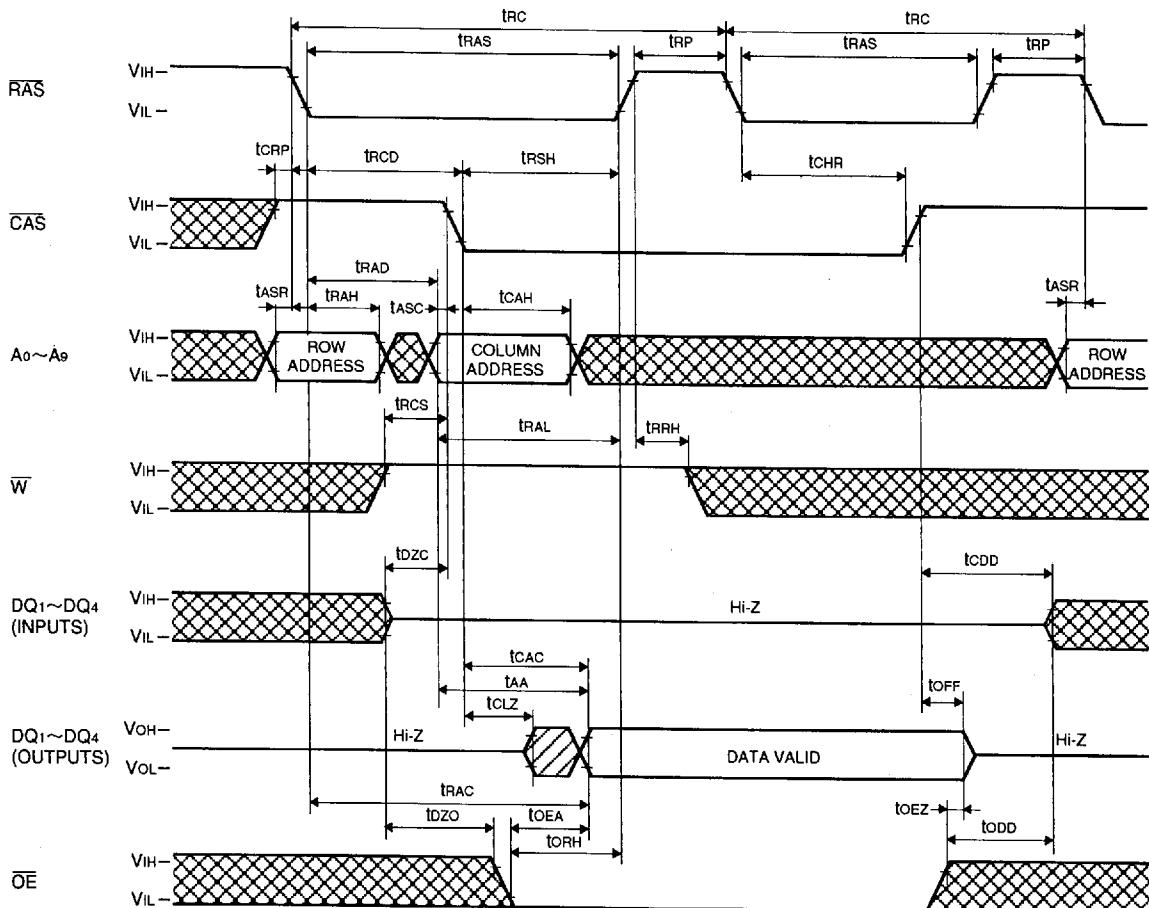
Note 31: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle described above.

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Fast Page Mode Read Cycle
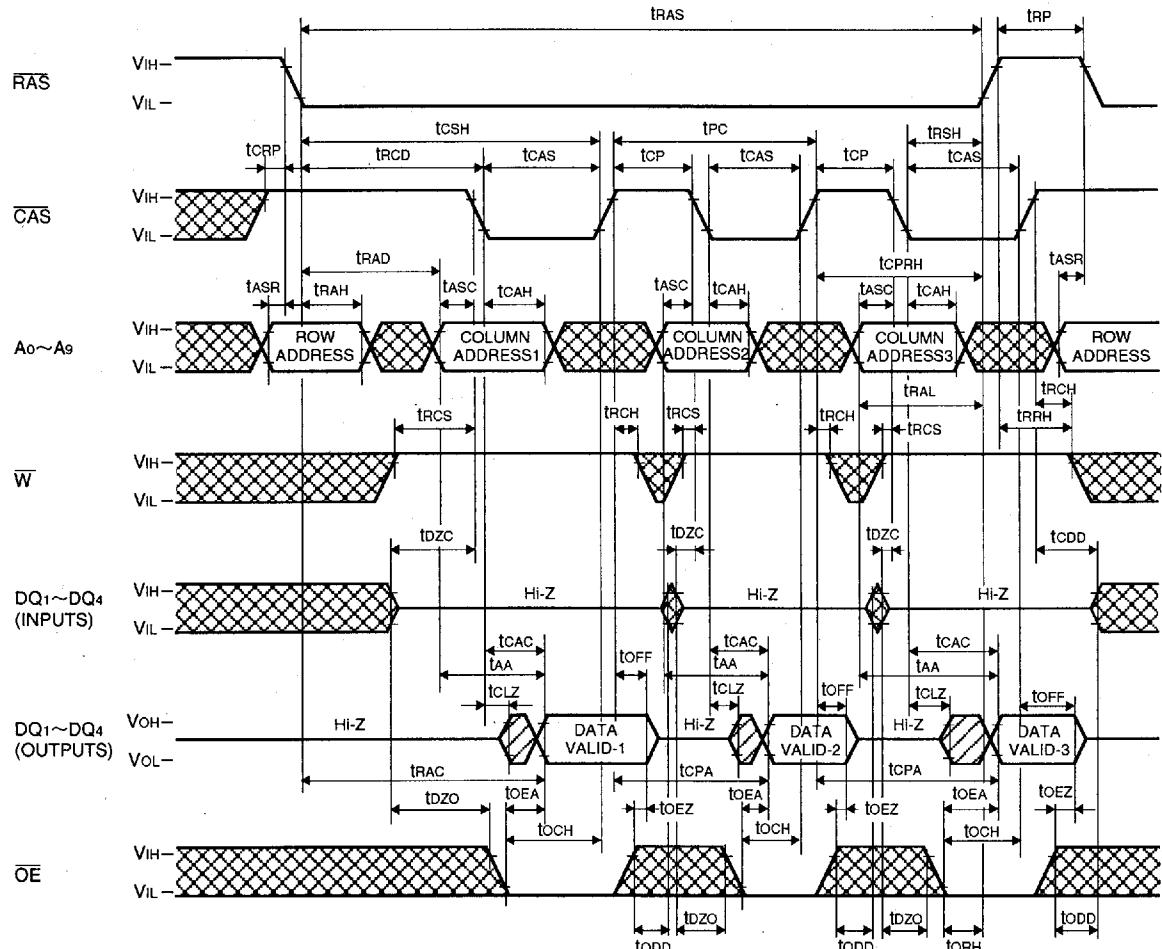
FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Fast Page Mode Write Cycle (Early Write)

Fast-Page Mode Write Cycle (Delayed Write)

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Fast Page Mode Read-Write, Read-Modify-Write Cycle

Self Refresh Cycle* (Note 28)

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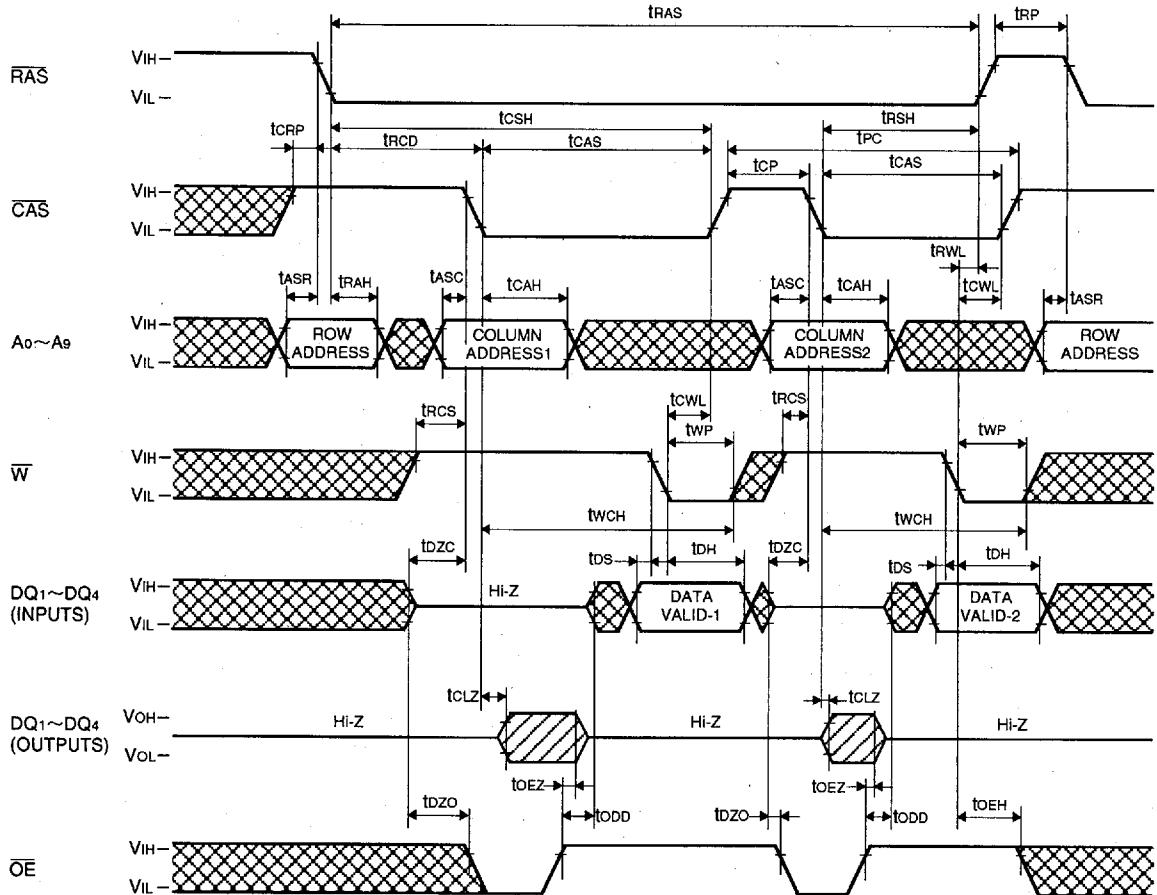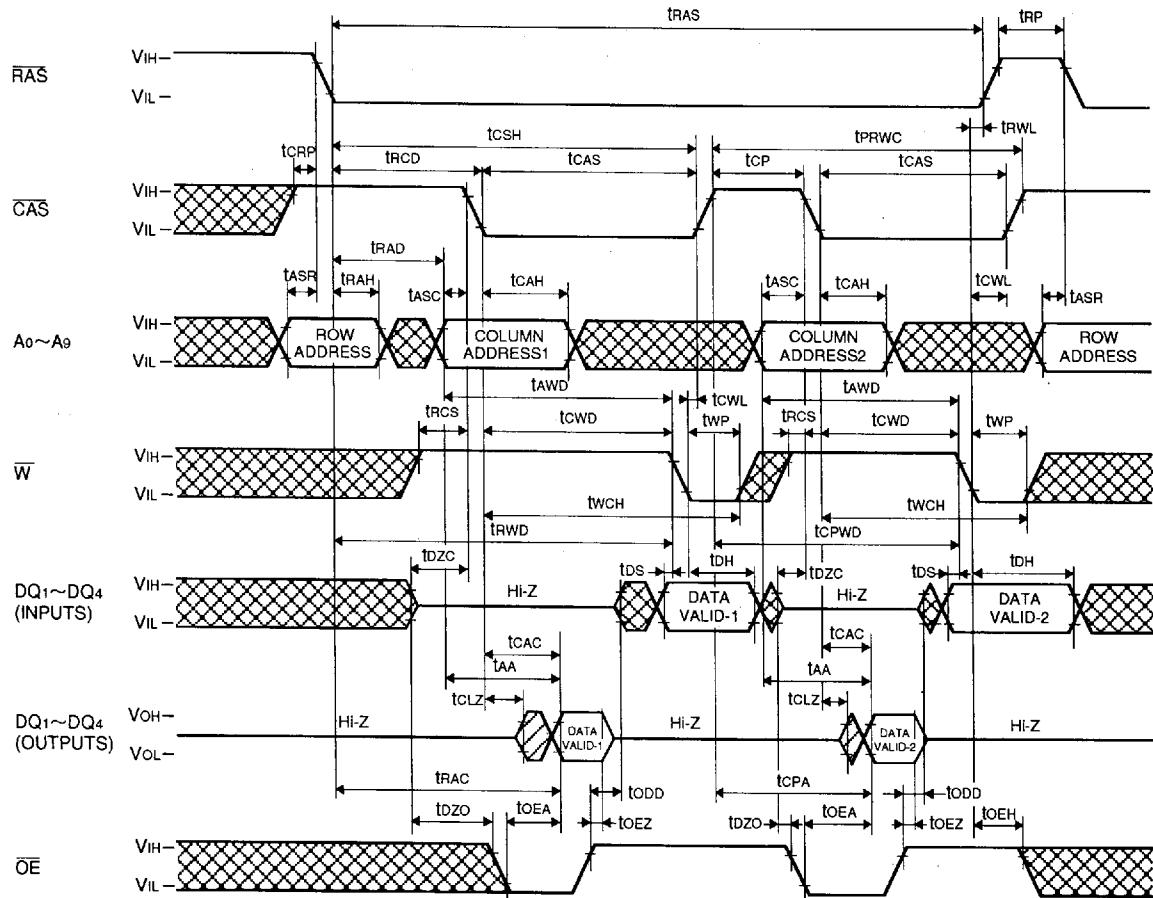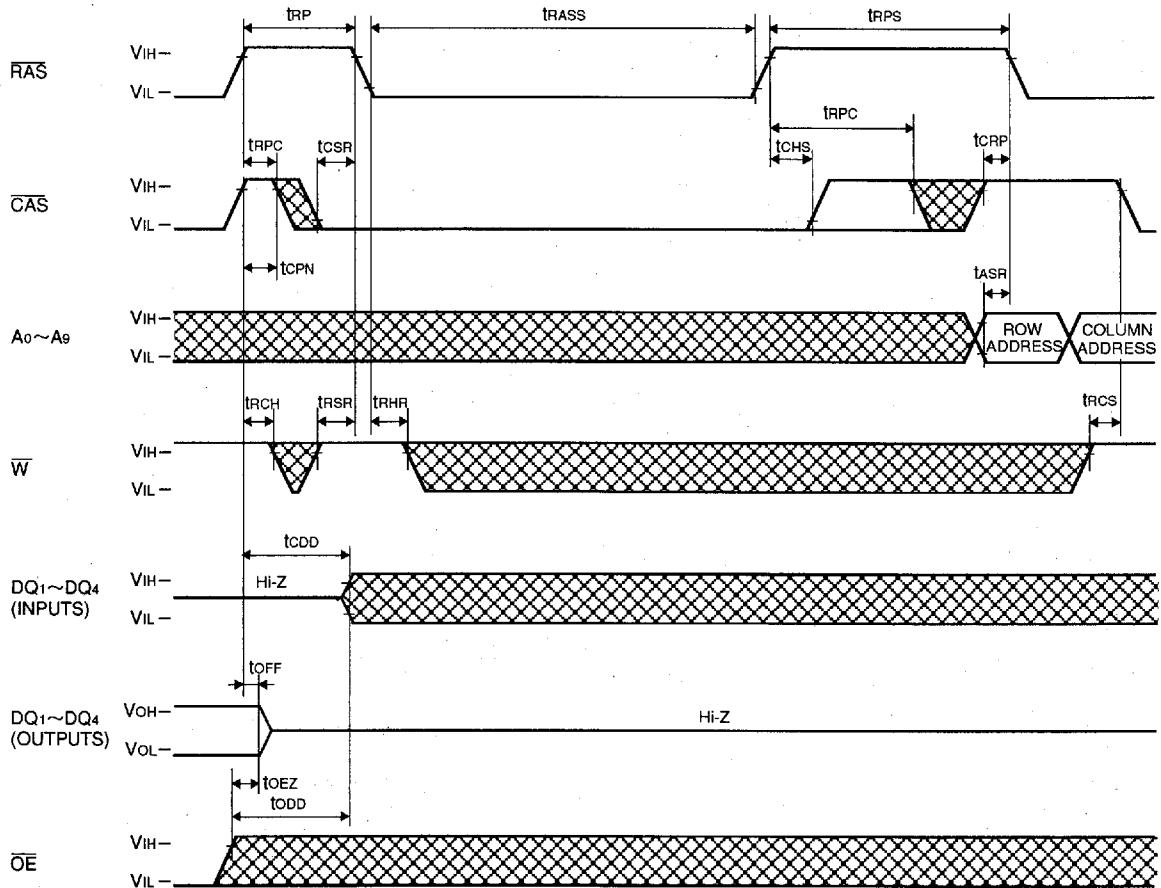
FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

Test Mode Set Cycle (Note 32)
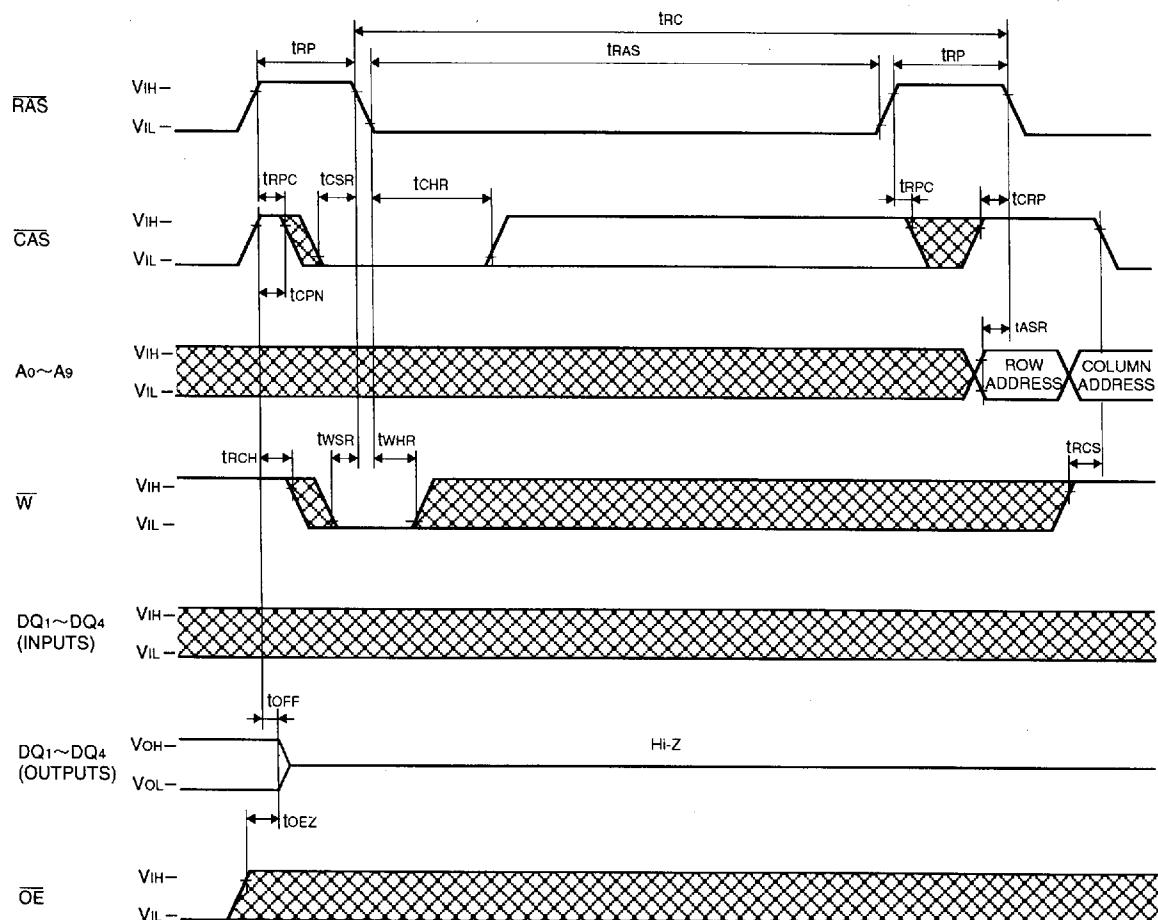
Note : 32 The cycle is also avaiilable for initialization cycle, but in this case device enters test mode.
The test mode function is initiated with a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle(WCBR cycle) as specified above timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$(CBR) refresh or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 4-bits wide (256k-bytes deep) for each DQ (input/output) port.
No addressing of A0,A1(column only) is required.
During a write cycle, data on the each DQ (input) pin is written in parallel into all 4-bits for each DQ port and can be written independently for each DQ port.
During a read cycle, the each DQ (output) pin indicates independently a HIGH state if all 4-bits are equal, and a LOW state if any bits differ.
During the test mode operation, a WCBR cycle is used to perform refresh.

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Note 28:Self refresh sequence

Two refreshing methods should be used properly depending on the low pulse width(t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

### 1. Distributed refresh during Read/Write operation

(A) Timing diagram
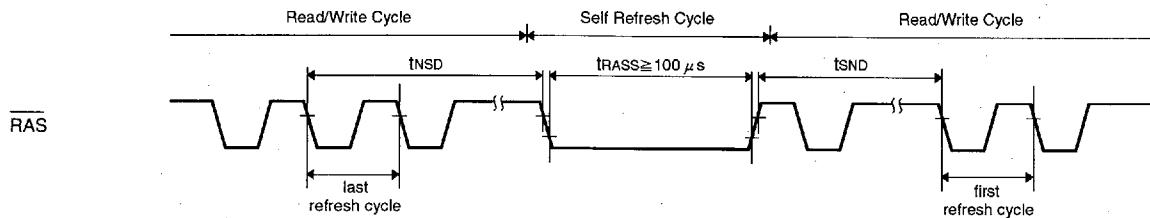
Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} \leqq 125 \mu s$	$t_{SND} \leqq 125 \mu s$
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16 \mu s$	$t_{SND} \leqq 16 \mu s$

(B) Definition of distributed refresh
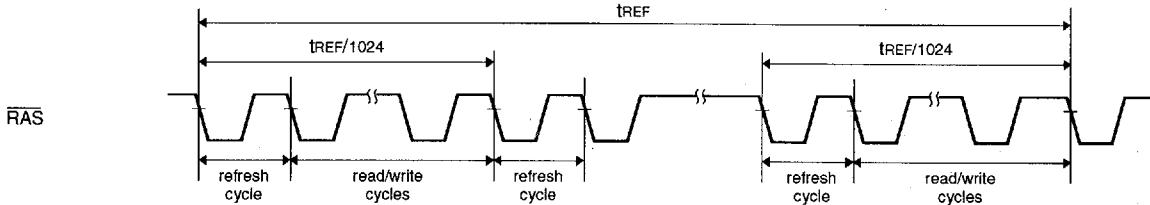
Definition of CBR distributed refresh
(Including extended refresh)

The CBR distributed refresh performs more than 1024 constant period (125 μs max.) CBR cycles within 128ms.

Definition of $\overline{RAS}$ only distributed refresh

All combinations of row address signals ($A_0 \sim A_9$) are selected during 1024 constant period (16 μs max.) $\overline{RAS}$ only refresh cycles within 16.4ms.

Note:
Hidden refresh may be used instead of CBR refresh.
$\overline{RAS}/\overline{CAS}$ refresh may be used instead of $\overline{RAS}$ only refresh.

1.1 CBR distributed refresh

● Switching from read/write operation to self refresh operation.
The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).

● Switching from self refresh operation to read/write operation.
The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2)

1.2 $\overline{RAS}$ only distributed refresh

● Switching from read/write operation to self refresh operation.
The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.

● Switching from self refresh operation to read/write operation.
The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

FAST PAGE MODE 4194304-BIT (1048576-WORD BY 4-BIT) DYNAMIC RAM

2. Burst refresh during Read/Write operation

(A) Timing diagram
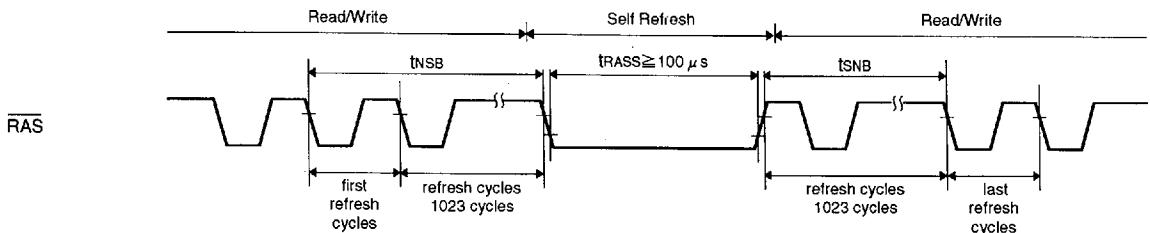
Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh
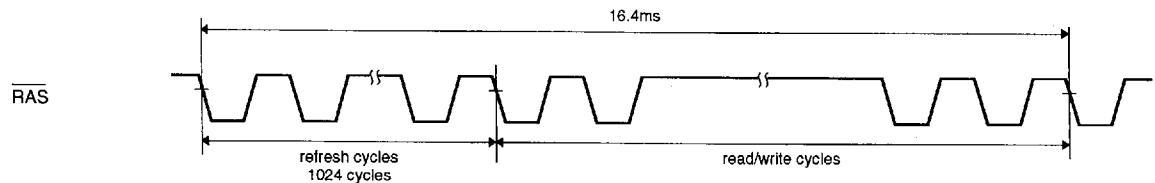
Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of row address signals ($A_0 \sim A_9$) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4ms.

2.1 CBR burst refresh

● Switching from read/write operation to self refresh operation.
The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4ms.

● Switching from self refresh operation to read/write operation.
The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

2.2 $\overline{RAS}$ only burst refresh

● Switching from read/write operation to self refresh operation.
The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).

● Switching from self refresh operation to read / write operation.
The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period should be set within t_{SNB} (shown in table 3).